



### Data Sheet

### $\pi$ 220N61/ $\pi$ 221N61

#### FEATURES

- Bidirectional I<sup>2</sup>C communication
- Ultra-low power consumption
- Supports up to 2 MHz operation
- Open-drain interfaces
  - Side 1 outputs with 3.5 mA sink current
  - Side 2 outputs with 35 mA sink current
- 3.0V to 5.5V supply/logic levels
- High common-mode transient immunity: 120 kV/ $\mu$ s typical
- Safety and regulatory approvals:
  - UL certificate number: E494497
    - 5000Vrms for 1 minute per UL 1577
  - CSA Component Acceptance Notice 5A
  - VDE certificate number: 40052896
    - DIN VDE V 0884-11:2017-01
    - V<sub>IORM</sub> = 1200V peak
  - CQC certification per GB4943.1-2011
  - AEC-Q100 (Pending)
- Wide temperature range: -40°C to 125°C
- RoHS-compliant, WB SOIC-16 package
- APPLICATIONS**
  - Isolated I<sup>2</sup>C, SMBus, PMBus interfaces
  - Multilevel I<sup>2</sup>C interfaces
  - Electric and Hybrid-Electric Vehicles
  - Open-Drain Networks
  - I<sup>2</sup>C Level Shifting
  - Power supplies
- GENERAL DESCRIPTION**

tions where a bidirectional clock is not required. The  $\pi$ 221N61 is used in applications that have a single master while the  $\pi$ 220N61 is suitable for multi-master applications.

These devices feature independent 3.0V to 5.5V supplies on each side of the isolator. These devices operate from DC to 2MHz at ambient temperatures of -40°C to +125°C.

#### FUNCTIONAL BLOCK DIAGRAMS

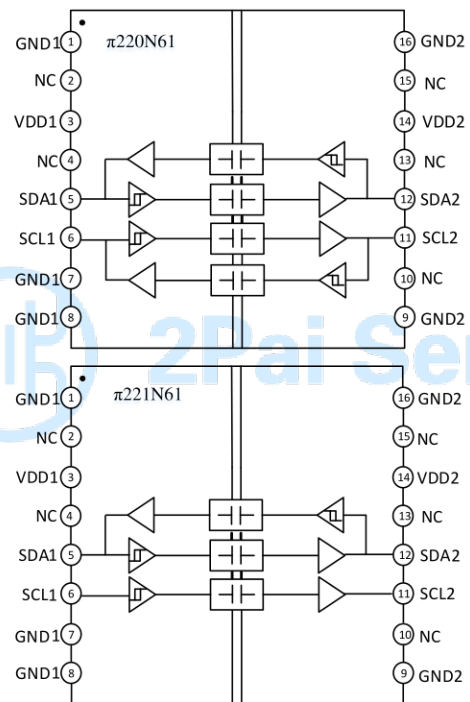


Figure1.  $\pi$ 220N61/ $\pi$ 221N61 functional Block Diagram

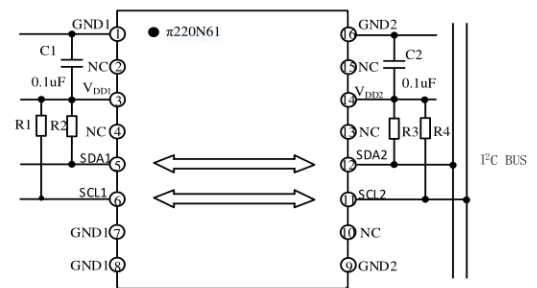


Figure2.  $\pi$ 220N61 Typical Application Circuit

The  $\pi$ 220N61/ $\pi$ 221N61 devices are low-power bidirectional isolators compatible with the I<sup>2</sup>C interface and are based on iDivider® technology from 2PaiSemi. These devices have logic input and output buffers that are separated by using a silicon dioxide (SiO<sub>2</sub>) barrier. These devices block high voltages and prevent noise currents from entering the control side ground, avoiding circuit interference and damaging sensitive components.

The  $\pi$ 220N61/ $\pi$ 221N61 devices are based on iDivider® technology with functional, performance, size, and power consumption advantages as compared to optocouplers.

The  $\pi$ 220N61 provides two bidirectional channels, supporting a complete isolated I<sup>2</sup>C interface. The  $\pi$ 221N61 provides one bidirectional channel and one unidirectional channel for applica-

## PIN CONFIGURATIONS AND FUNCTIONS

### $\pi 220N61/\pi 221N61$ Pin Function Descriptions

Pin No.	Name	Description
1	GND1	Ground 1. This pin is the ground reference for Isolator Side 1.
2	NC	No connect.
3	VDD1	Supply Voltage for Isolator Side 1.
4	NC	No connect.
5	SDA1	Serial data input / output, side 1.
6	SCL1	Serial clock input / output, side 1.
7	GND1	Ground 1. This pin is the ground reference for Isolator Side 1.
8	GND1	Ground 1. This pin is the ground reference for Isolator Side 1.
9	GND2	Ground 2. This pin is the ground reference for Isolator Side 2.
10	NC	No connect.
11	SCL2	Serial clock input / output, side 2.
12	SDA2	Serial data input / output, side 2.
13	NC	No connect.
14	VDD2	Supply Voltage for Isolator Side 2.
15	NC	No connect.
16	GND2	Ground 2. This pin is the ground reference for Isolator Side 2.

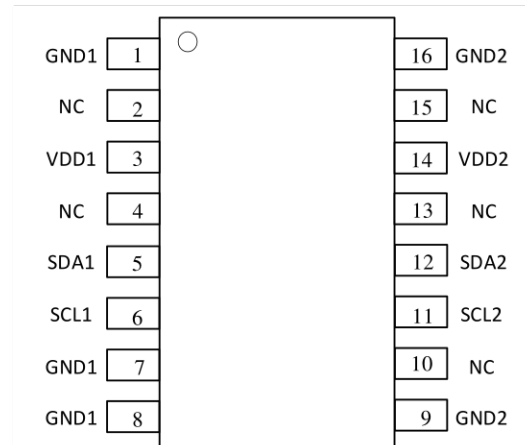


Figure3.  $\pi 220N61/\pi 221N61$  Pin Configuration

## ABSOLUTE MAXIMUM RATINGS

Table 1. Absolute Maximum Ratings<sup>1,2</sup>

Parameter	Rating
Supply Voltages ( $V_{DD1-GND1}$ , $V_{DD2-GND2}$ )	-0.5 V to +7.0 V
Signal Voltage SDA1/SCL1	-0.5 V to $V_{DDx} + 0.5$ V
Signal Voltage SDA2/SCL2	-0.5 V to $V_{DDx} + 0.5$ V
Average Output Current SDA1/SCL1 ( $I_{O1}$ )	-20 mA to +20 mA
Average Output Current SDA2/SCL2 ( $I_{O2}$ )	-100 mA to +100 mA
Storage Temperature ( $T_{ST}$ ) Range	-55°C to +150°C
Maximum junction temperature $T_{J(MAX)}$	+150°C

Notes:

<sup>1</sup> All voltage values here within are with respect to the local ground pin (GND1 or GND2) and are peak voltage values.

<sup>2</sup> Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## RECOMMENDED OPERATING CONDITIONS

Table 2. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	$V_{DDx}^1$	3		5.5	V
Input/Output Signal Voltage ( $V_{SDA1}$ , $V_{SCL1}$ , $V_{SDA2}$ , $V_{SCL2}$ )		0		$V_{DDx}^1$	V
Low-level input voltage, side 1	$V_{IL1}$	0		0.45	V
High-level input voltage, side 1	$V_{IH1}$	$0.7 * V_{DD1}$		$V_{DD1}$	V
Low-level input voltage, side 2	$V_{IL2}$	0		$0.3 * V_{DD2}$	V

High-level input voltage, side 2	$V_{IH2}$	$0.7 \cdot V_{DD2}$	$V_{DD2}$	V
Output current, side 1	$I_{OL1}$	0.5	3.5	mA
Output current, side 2	$I_{OL2}$	0.5	35	mA
Capacitive load, side 1	C1		40	pF
Capacitive load, side 2	C2		400	pF
Operating frequency	$f_{MAX}$		2	MHz
Ambient Operating Temperature	$T_A$	-40	125	°C

Notes:

<sup>1</sup>  $V_{DDx}$  is the side voltage power supply  $V_{DD}$ , where x = 1 or 2.**Truth Tables****Table 3.  $\pi 220N61/\pi 221N61$  Truth Table**

$V_{Ix}$ Input <sup>1</sup>	$V_{DD1}$ State <sup>1</sup>	$V_{DD0}$ State <sup>1</sup>	$V_{Ox}$ Output <sup>1</sup>
Low	Powered <sup>2</sup>	Powered <sup>2</sup>	Low
High	Powered <sup>2</sup>	Powered <sup>2</sup>	High Impedance
Open <sup>4</sup>	Powered <sup>2</sup>	Powered <sup>2</sup>	High Impedance
Don't Care	Unpowered <sup>3</sup>	Powered <sup>2</sup>	High Impedance
Don't Care	Powered <sup>2</sup>	Unpowered <sup>3</sup>	High Impedance

Notes:

<sup>1</sup>  $V_{Ix}/V_{Ox}$  are the input/output signals of a given channel (SDA or SCL).  $V_{DD1}/V_{DD0}$  are the supply voltages on the input/output signal sides of this given channel.<sup>2</sup> Powered means  $V_{DDx} \geq 2.95$  V<sup>3</sup> Unpowered means  $V_{DDx} < 2.30$  V<sup>4</sup> Invalid input condition as an I<sup>2</sup>C system requires that a pullup resistor to  $V_{DD}$  is connected.**SPECIFICATIONS****ELECTRICAL CHARACTERISTICS****Table 4. DC Specifications** $V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC} \pm 10\%$  or  $5V_{DC} \pm 10\%$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
<b>SIDE 1 LOGIC LEVELS</b>						
Voltage input threshold low, SDA1 and SCL1	$V_{ILT1}$	470	510	570	mV	
Voltage input threshold high, SDA1 and SCL1	$V_{IHT1}$	540	580	630	mV	
Voltage input hysteresis	$V_{HYST1}$	50	70		mV	$V_{IHT1} - V_{ILT1}$
Low-level output voltage, SDA1 and SCL1	$V_{OL1}$	650	700	800	mV	$0.5 \text{ mA} \leq (I_{SDA1} \text{ and } I_{SCL1}) \leq 3.5 \text{ mA}$
Low-level output voltage to high-level input voltage threshold difference, SDA1 and SCL1	$\Delta V_{OIT1}^1$	60	120		mV	$0.5 \text{ mA} \leq (I_{SDA1} \text{ and } I_{SCL1}) \leq 3.5 \text{ mA}$
<b>SIDE 2 LOGIC LEVELS</b>						
Voltage input threshold low, SDA2 and SCL2	$V_{ILT2}$	$0.30 \cdot V_{DD2}$		$0.42 \cdot V_{DD2}$	V	
Voltage input threshold high, SDA2 and SCL2	$V_{IHT2}$	$0.60 \cdot V_{DD2}$		$0.66 \cdot V_{DD2}$	V	
Voltage input hysteresis	$V_{HYST2}$	$0.20 \cdot V_{DD2}$	$0.28 \cdot V_{DD2}$		V	$V_{IHT2} - V_{ILT2}$
Low-level output voltage, SDA2 and SCL2	$V_{OL2}$			0.4	V	$0.5 \text{ mA} \leq (I_{SDA2} \text{ and } I_{SCL2}) \leq 35 \text{ mA}$
<b>BOTH SIDES</b>						
Input leakage currents, SDA1, SCL1, SDA2, and SCL2	$ I_{IN} $		0.01	10	$\mu\text{A}$	$V_{SDA1}, V_{SCL1} = V_{DD1}; V_{SDA2}, V_{SCL2} = V_{DD2}$

$V_{DDx}^3$ Undervoltage Rising Threshold	$V_{DDxUV+}$	2.45	2.75	2.95	V
$V_{DDx}^3$ Undervoltage Falling Threshold	$V_{DDxUV-}$	2.30	2.60	2.80	V
$V_{DDx}^3$ Hysteresis	$V_{DDxUVH}$		0.15		V

Notes:

<sup>1</sup>  $\Delta VOIT1 = VOL1 - VIHT1$ . This is the minimum difference between the output logic low level and the input logic threshold within a given component. This ensures that there is no possibility of the part latching up the bus to which it is connected.

<sup>2</sup>  $V_{DDx}$  is the side voltage power supply  $V_{DD}$ , where  $x = 1$  or  $2$ .

**Table 5. Quiescent Supply Current**

$V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC} \pm 10\%$  or  $5V_{DC} \pm 10\%$ ,  $T_A = 25^\circ C$ ,  $R1, R2 = \text{Open}$ ;  $C1, C2 = \text{Open}$  (figure 17), unless otherwise noted. Test method refer to Figure 17.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
$\pi 220N61$ Quiescent Supply Current @ $5V_{DC}$ Supply	$I_{DD1(Q)}$		1.7	2.4	mA	$V_{SDA1}, V_{SCL1} = GND1$ ; $V_{SDA2}, V_{SCL2} = GND2$
	$I_{DD2(Q)}$		1.4	2.1	mA	
	$I_{DD1(Q)}$		1.5	2.3	mA	$V_{SDA1}, V_{SCL1} = V_{DD1}$ ; $V_{SDA2}, V_{SCL2} = V_{DD2}$
	$I_{DD2(Q)}$		1.2	1.8	mA	
$\pi 220N61$ Quiescent Supply Current @ $3.3V_{DC}$ Supply	$I_{DD1(Q)}$		1.5	2.3	mA	$V_{SDA1}, V_{SCL1} = GND1$ ; $V_{SDA2}, V_{SCL2} = GND2$
	$I_{DD2(Q)}$		1.2	1.8	mA	
	$I_{DD1(Q)}$		1.5	2.3	mA	$V_{SDA1}, V_{SCL1} = V_{DD1}$ ; $V_{SDA2}, V_{SCL2} = V_{DD2}$
	$I_{DD2(Q)}$		1.2	1.8	mA	
$\pi 221N61$ Quiescent Supply Current @ $5V_{DC}$ Supply	$I_{DD1(Q)}$		1.1	1.7	mA	$V_{SDA1}, V_{SCL1} = GND1$ ; $V_{SDA2}, V_{SCL2} = GND2$
	$I_{DD2(Q)}$		1.2	1.8	mA	
	$I_{DD1(Q)}$		1.2	1.8	mA	$V_{SDA1}, V_{SCL1} = V_{DD1}$ ; $V_{SDA2}, V_{SCL2} = V_{DD2}$
	$I_{DD2(Q)}$		1.2	1.8	mA	
$\pi 221N61$ Quiescent Supply Current @ $3.3V_{DC}$ Supply	$I_{DD1(Q)}$		1.0	1.5	mA	$V_{SDA1}, V_{SCL1} = GND1$ ; $V_{SDA2}, V_{SCL2} = GND2$
	$I_{DD2(Q)}$		1.1	1.7	mA	
	$I_{DD1(Q)}$		1.1	1.7	mA	$V_{SDA1}, V_{SCL1} = V_{DD1}$ ; $V_{SDA2}, V_{SCL2} = V_{DD2}$
	$I_{DD2(Q)}$		1.1	1.7	mA	

**Table 6. Switching Specifications**

$V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC} \pm 10\%$  or  $5V_{DC} \pm 10\%$ ,  $T_A = 25^\circ C$ , unless otherwise noted. Test method refer to Figure 17.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Output Signal Fall Time SDA1, SCL1	$t_{f1}$	10	18	30	ns	$0.9 V_{DD1}$ to $0.9 V$ ; $R1 = 1430 \Omega, C1 = 40 \text{ pF}$ , @ $5V_{DC}$ supply
		9	16	28	ns	$R1 = 953 \Omega, C1 = 40 \text{ pF}$ ; @ $3.3V_{DC}$ supply
		6	11	18	ns	$0.7 V_{DD1}$ to $0.3 V_{DD1}$ ; $R1 = 1430 \Omega, C1 = 40$ $\text{pF}$ , @ $5V_{DC}$ supply
		6	10	16	ns	$R1 = 953 \Omega, C1 = 40 \text{ pF}$ ; @ $3.3V_{DC}$ supply
Output Signal Fall Time (SDA2, SCL2)	$t_{f2}$	22	36	45	ns	$0.9V_{DD2}$ to $0.4V$ ; $R2 = 143 \Omega, C2 = 400 \text{ pF}$ , @ $5V_{DC}$ supply
		20	31	42	ns	$R2 = 95.3 \Omega, C2 = 400 \text{ pF}$ ; @ $3.3V_{DC}$ supply
		9	16	26	ns	$0.7 V_{DD2}$ to $0.3 V_{DD2}$ ; $R2 = 143 \Omega, C2 = 400 \text{ pF}$ , @ $5V_{DC}$ supply
		8	14	23	ns	$R2 = 95.3 \Omega, C2 = 400 \text{ pF}$ ; @ $3.3V_{DC}$ supply
Low-to-High Propagation Delay, Side 1 to Side 2	$t_{pLH1-2}$		45	68	ns	$0.55 V$ to $0.7 \times V_{DD2}$ ; $R1 = 1430 \Omega, R2 = 143 \Omega$ ,

			38	57	ns	C1, C2 = 10 pF; @ 5V <sub>DC</sub> supply
High-to-Low Propagation Delay, Side 1 to Side 2	t <sub>PHL1-2</sub>		67	100	ns	R1 = 953 $\Omega$ , R2 = 95.3 $\Omega$ , C1, C2 = 10 pF; @ 3.3V <sub>DC</sub> supply
			64	96	ns	0.7 V to 0.4 V; R1 = 1430 $\Omega$ , R2 = 143 $\Omega$ , C1, C2 = 10 pF; @ 5V <sub>DC</sub> supply
Pulse Width Distortion  t <sub>PHL1-2</sub> – t <sub>PLH1-2</sub>	PWD <sub>1-2</sub>		22	32	ns	R1 = 953 $\Omega$ , R2 = 95.3 $\Omega$ , C1, C2 = 10 pF; @ 3.3V <sub>DC</sub> supply
			26	39	ns	R1 = 1430 $\Omega$ , R2 = 143 $\Omega$ , C1, C2 = 10 pF; @ 5V <sub>DC</sub> supply
Low-to-High Propagation Delay, Side 2 to Side 1	t <sub>PLH2-1</sub>		44	62	ns	R1 = 953 $\Omega$ , R2 = 95.3 $\Omega$ , C1, C2 = 10 pF; @ 3.3V <sub>DC</sub> supply
			42	56	ns	0.4 $\times$ V <sub>DD2</sub> to 0.7 $\times$ V <sub>DD1</sub> ; R1 = 1430 $\Omega$ , R2 = 143 $\Omega$ , C1, C2 = 10 pF; @ 5V <sub>DC</sub> supply
High-to-Low Propagation Delay, Side 2 to Side 1	t <sub>PHL2-1</sub>		52	78	ns	R1 = 953 $\Omega$ , R2 = 95.3 $\Omega$ , C1, C2 = 10 pF; @ 3.3V <sub>DC</sub> supply
			57	86	ns	0.4 $\times$ V <sub>DD2</sub> to 0.9 V; R1 = 1430 $\Omega$ , R2 = 143 $\Omega$ , C1, C2 = 10 pF; @ 5V <sub>DC</sub> supply
Pulse Width Distortion  t <sub>PHL2-1</sub> – t <sub>PLH2-1</sub>	PWD <sub>2-1</sub>		8	16	ns	R1 = 953 $\Omega$ , R2 = 95.3 $\Omega$ , C1, C2 = 10 pF; @ 3.3V <sub>DC</sub> supply
			15	30	ns	R1 = 1430 $\Omega$ , R2 = 143 $\Omega$ , C1, C2 = 10 pF; @ 5V <sub>DC</sub> supply
Round-trip propagation delay on Side 1	t <sub>LOOP1</sub>		104	156	ns	R1 = 953 $\Omega$ , R2 = 95.3 $\Omega$ , C1, C2 = 10 pF; @ 3.3V <sub>DC</sub> supply
			88	132	ns	0.4 V to 0.3 $\times$ V <sub>DD1</sub> ; R1 = 1430 $\Omega$ , R2 = 143 $\Omega$ , C1, C2 = 10 pF; @ 5V <sub>DC</sub> supply
Common-Mode Transient Immunity <sup>2</sup>	CMTI	120			kV/ $\mu$ s	R1 = 953 $\Omega$ , R2 = 95.3 $\Omega$ , C1, C2 = 10 pF; @ 3.3V <sub>DC</sub> supply
ESD (HBM - Human body model)	ESD	$\pm 6$			kV	0.4 V to 0.3 $\times$ V <sub>DD1</sub> ; R1 = 1430 $\Omega$ , R2 = 143 $\Omega$ , C1, C2 = 10 pF; @ 5V <sub>DC</sub> supply

Notes:

<sup>1</sup> V<sub>DDx</sub> is the side voltage power supply V<sub>DD</sub>, where x = 1 or 2.<sup>2</sup> See Figure 21 for Common-mode transient immunity (CMTI) measurement.**INSULATION AND SAFETY RELATED SPECIFICATIONS****Table 7. Insulation Specifications**

Parameter	Symbol	Value	Unit	Test Conditions/Comments
		$\pi 220N61/\pi 221N61$		
Rated Dielectric Insulation Voltage		5000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L (CLR)	8	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (CRP)	8	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	8.5	mm min	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		21	$\mu$ m min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Material Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

**PACKAGE CHARACTERISTICS****Table 8. Package Characteristics**

Parameter	Symbol	Typical Value	Unit	Test Conditions/Comments
		$\pi 220N61/\pi 221N61$		
Resistance (Input to Output) <sup>1</sup>	R <sub>I-O</sub>	10 <sup>11</sup>	$\Omega$	
Capacitance (Input to Output) <sup>1</sup>	C <sub>I-O</sub>	1.5	pF	@1MHz
Input Capacitance <sup>2</sup>	C <sub>I</sub>	7	pF	@1MHz
IC Junction to Ambient Thermal Resistance	$\theta_{JA}$	45	$^{\circ}\text{C}/\text{W}$	Thermocouple located at center of package underside

Notes:

<sup>1</sup>The device is considered a 2-terminal device; WSOIC-16 Pin 1 – Pin 8 are shorted together as the one terminal, and WSOIC-16 Pin 9 - Pin 16 are shorted together as the other terminal.

<sup>2</sup>Testing from the input signal pin to ground.

**REGULATORY INFORMATION**

See Table 9 for details regarding recommended maximum working voltages for specific cross isolation waveforms and insulation levels.

**Table 9. Regulatory**

UL	VDE	CQC
Recognized under UL 1577 Component Recognition Program <sup>1</sup>	DIN VDE V 0884-11:2017-01 <sup>2</sup>	Certified under CQC11-471543-2012
Single Protection, 5000 V rms Isolation Voltage	Basic insulation, V <sub>IORM</sub> = 1200 V peak, V <sub>IOSM</sub> = 5000 V peak	GB4943.1-2011
		Basic insulation at 845 V rms (1200 V peak) working voltage Reinforced insulation at 422 V rms (600 V peak)
File (E494497)	File (40052896)	File (CQC20001260258)

Notes:

<sup>1</sup>In accordance with UL 1577, each  $\pi 220N61/\pi 221N61$  is proof tested by applying an insulation test voltage  $\geq 6000$  V rms for 1 sec.

<sup>2</sup>In accordance with DIN V VDE V 0884-11, each  $\pi 220N61/\pi 221N61$  is proof tested by applying an insulation test voltage  $\geq 1800$  V peak for 1 sec (partial discharge detection limit = 5 pC). The \* marking branded on the component designates DIN V VDE V 0884-11 approval.

**DIN V VDE V 0884-11 (VDE V 0884-11) INSULATION CHARACTERISTICS**

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Protective circuits ensure the maintenance of the safety data. The \* marking on packages denotes DIN V VDE V 0884-11 approval.

**Table 10. VDE Insulation Characteristics**

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
			$\pi 220N61/\pi 221N61$	
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage $\leq 150$ V rms			I to IV	
For Rated Mains Voltage $\leq 300$ V rms			I to III	
For Rated Mains Voltage $\leq 400$ V rms			I to III	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum repetitive peak isolation voltage		V <sub>IORM</sub>	1200	V peak

Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.5 = V_{pd(m)}$ , 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1800	V peak
Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.2 = V_{pd(m)}$ , $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1440	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$ , $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC		1440	V peak
Highest Allowable Overvoltage		$V_{IOTM}$	7071	V peak
Surge Isolation Voltage Basic	Basic insulation, 1.2 $\mu$ s rise time, 50 $\mu$ s, 50% fall time	$V_{IOSM}$	5000	V peak
Surge Isolation Voltage Reinforced	Reinforced insulation, 1.2 $\mu$ s rise time, 50 $\mu$ s, 50% fall time, $V_{TEST} = 1.3 \times V_{IOSM}$ (qualification) <sup>1</sup>	$V_{IOSM}$		V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 3)			
Maximum Junction Temperature		$T_S$	150	$^{\circ}C$
Maximum Power Dissipation at 25 $^{\circ}C$		$P_S$	2.78	W
Insulation Resistance at $T_S$	$V_{IO} = 800$ V	$R_S$	>10 <sup>9</sup>	$\Omega$

Notes:

<sup>1</sup>In accordance with DIN V VDE V 0884-11,  $\pi 220N61/\pi 221N61$  is proof tested by applying a surge isolation voltage 6500 V.

Typical Thermal Characteristic

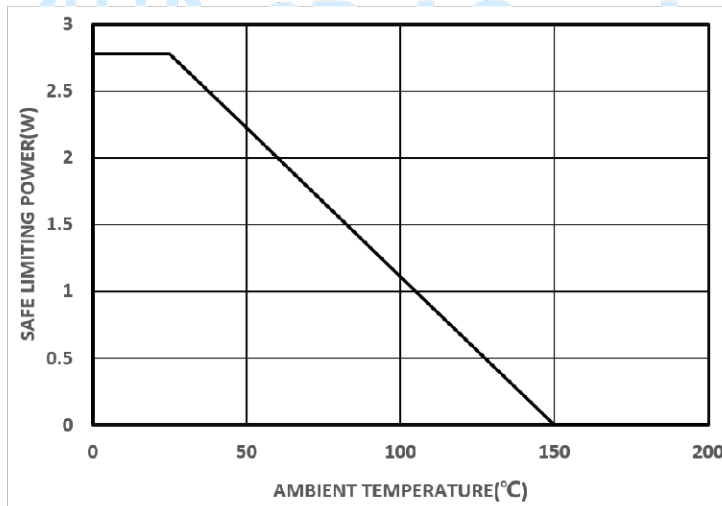


Figure 4. Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per VDE

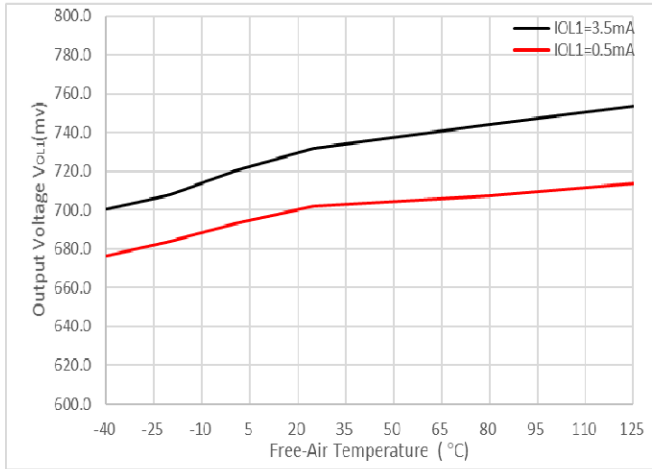


Figure 5. Side 1: Output Low Voltage vs Free-Air Temperature

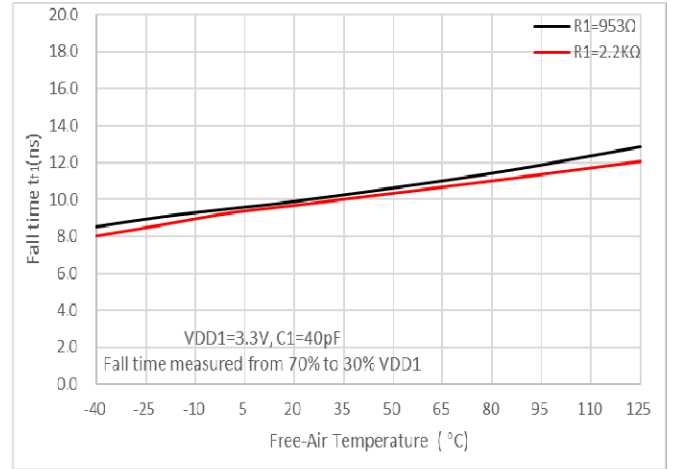


Figure 6. Side 1: Output Fall Time vs Free-Air Temperature

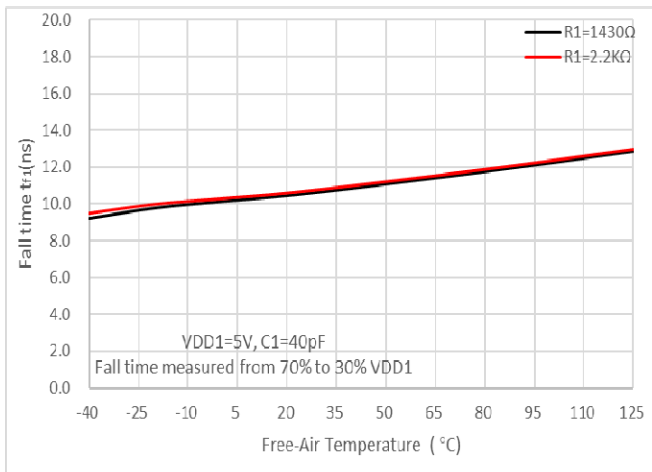


Figure 7. Side 1: Output Fall Time vs Free-Air Temperature

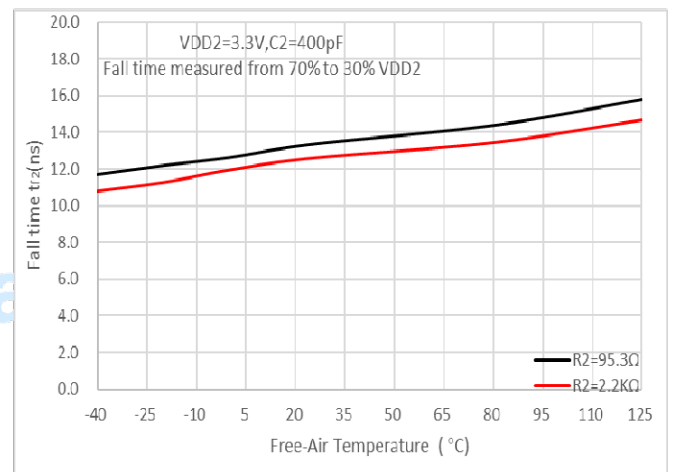


Figure 8. Side 2: Output Fall Time vs Free-Air Temperature

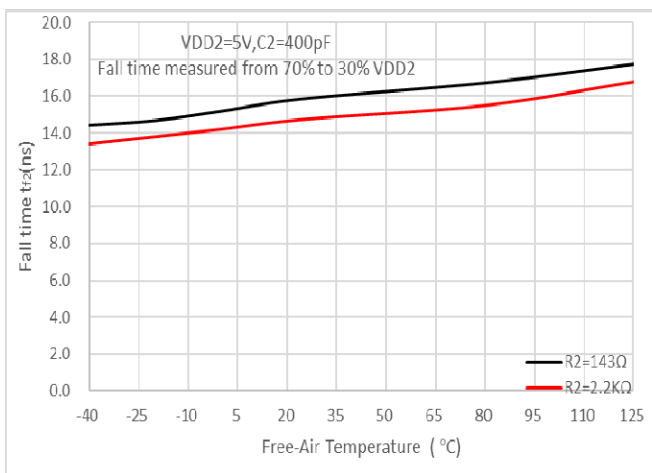


Figure 9. Side 2: Output Fall Time vs Free-Air Temperature

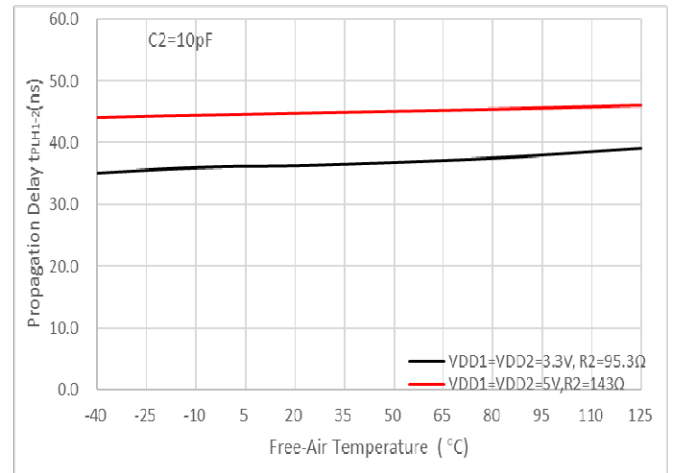


Figure 10.  $t_{PLH1-2}$  Propagation Delay vs Free-Air Temperature



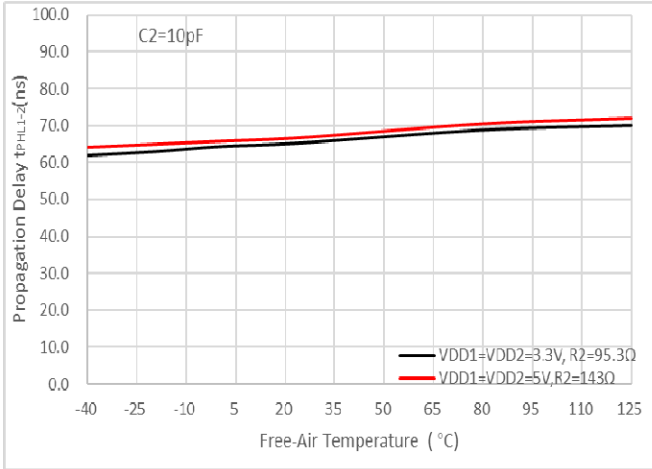


Figure 11.  $t_{PHL1-2}$  Propagation Delay vs Free-Air Temperature

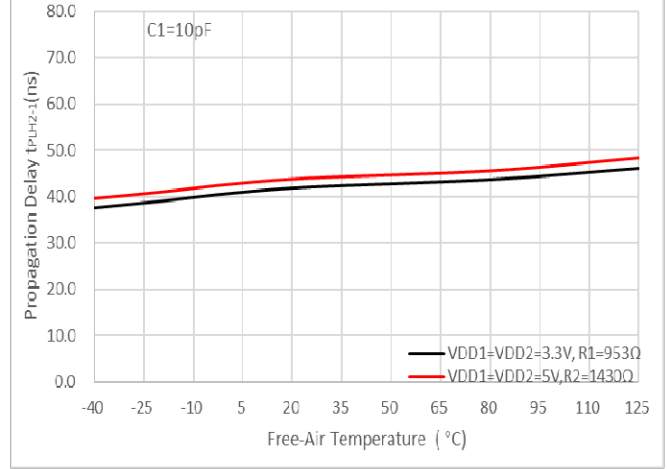


Figure 12.  $t_{PLH1-2}$  Propagation Delay vs Free-Air Temperature

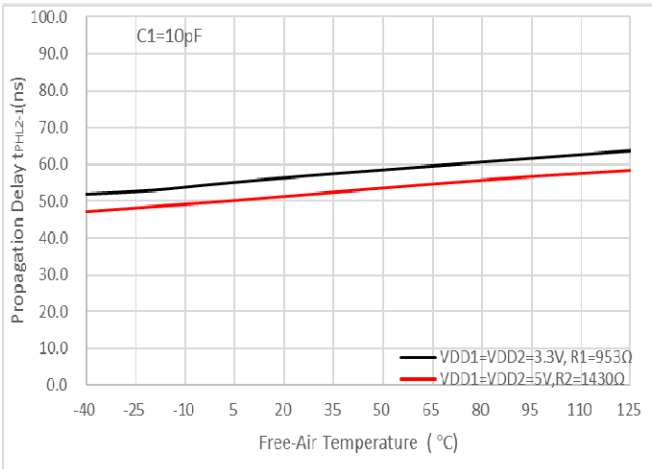


Figure 13.  $t_{PHL2-1}$  Propagation Delay vs Free-Air Temperature

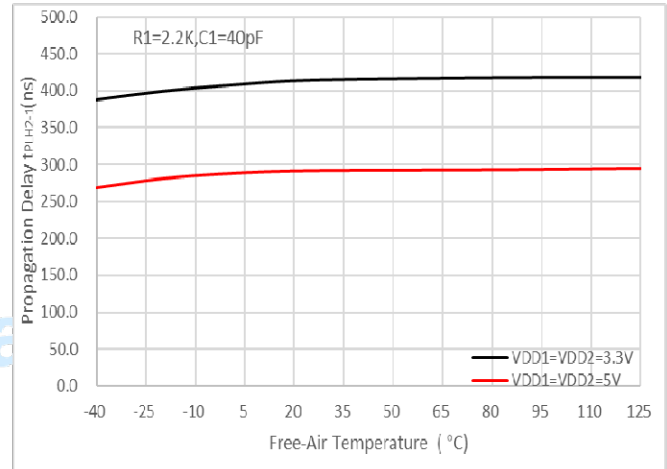


Figure 14.  $t_{PLH2-1}$  Propagation Delay vs Free-Air Temperature

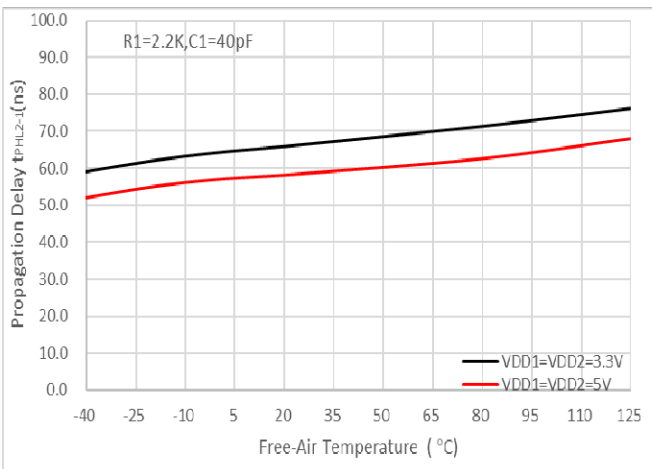


Figure 15.  $t_{PHL2-1}$  Propagation Delay vs Free-Air Temperature

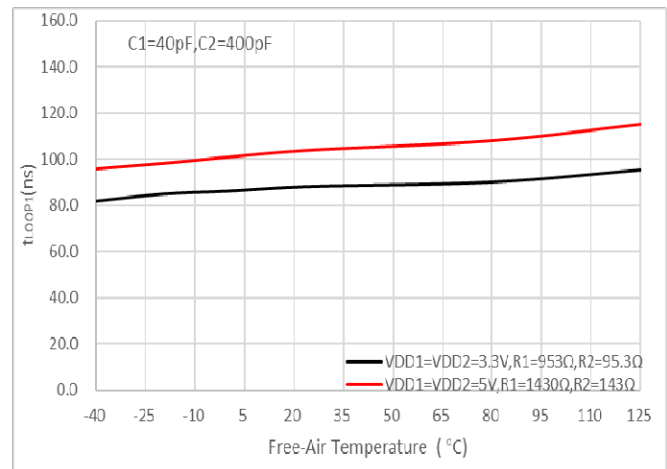


Figure 16.  $t_{LOOP1}$  vs Free-Air Temperature

PARAMETER MEASUREMENT INFORMATION

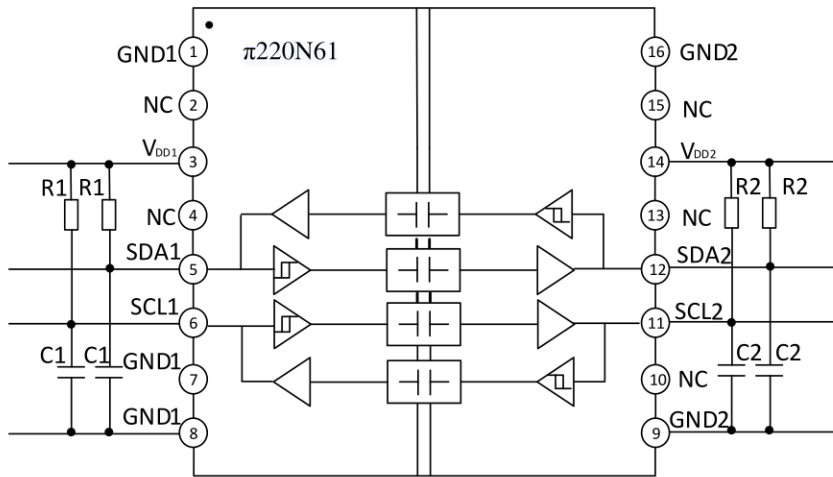


Figure 17. Test Diagram

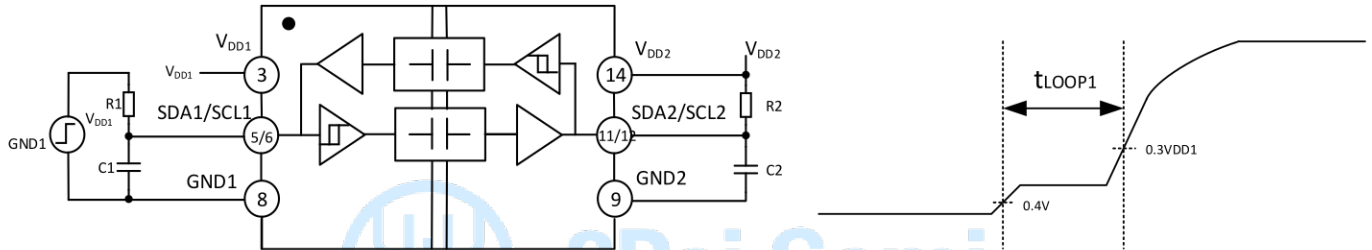


Figure 18.  $t_{LOOP1}$  Setup and Timing Diagram

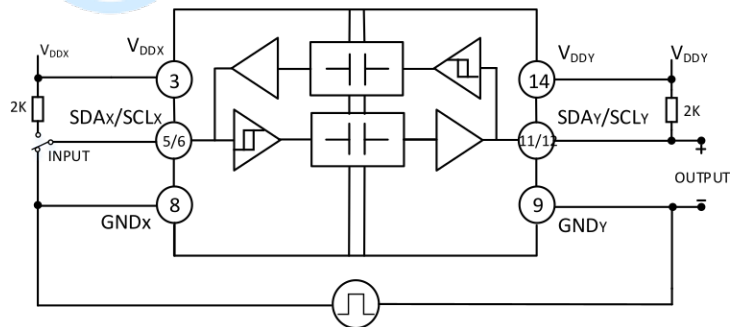


Figure 19. Common-Mode Transient Immunity Test Circuit

## APPLICATIONS INFORMATION

### Overview

The inter-integrated circuit (I<sup>2</sup>C) bus is a single-ended, two wire bus for efficient inter-IC communication and is used in a wide range of applications. The I<sup>2</sup>C bus is used for communication between multiple masters or a single master and slaves. The master device controls the serial clock line (SCL) and data is bidirectional transferred on the serial data line (SDA) between master and slaves. The I<sup>2</sup>C bus can theoretically add up to 112 communication nodes, however, the number of nodes will increase the load capacitance on the bus, thereby limiting the communication distances and communication speeds. In applications, tradeoffs are often made between communication speeds, bus length, and number of nodes based on actual conditions.

The I<sup>2</sup>C bus supports data transmission in four speeds: standard mode (up to 100Kbps), fast mode (up to 400Kbps), fast mode plus (up to 1Mbps), and high-speed mode (up to 3.4Mbps). The  $\pi$ 220N61/ $\pi$ 221N61 devices support all the above four communication modes.

### FUNCTIONAL DESCRIPTION

The  $\pi$ 220N61/ $\pi$ 221N61 devices are low-power bidirectional isolators compatible with the I<sup>2</sup>C interface and are based on iDivider<sup>®</sup> technology from 2PaiSemi. These devices have logic input and output buffers that are separated by using a silicon dioxide (SiO<sub>2</sub>) barrier. These devices block high voltages and prevent noise currents from entering the control side ground, avoiding circuit interference and damaging sensitive components. Each channel output of the  $\pi$ 220N61/ $\pi$ 221N61 devices is made open-drain to comply with the open-drain technology of I<sup>2</sup>C. Serial data line (SDA) and serial clock line (SCL) need to add pull-up resistors to ensure normal operation of the system. It is recommended that side 1 of the I<sup>2</sup>C isolator be connected to the processor and sides 2 to the bus when there are multiple nodes on the I<sup>2</sup>C bus as side 2 support up to 400 pF capacitance load.

The  $\pi$ 220N61/ $\pi$ 221N61 devices feature two bidirectional channels that have open-drain outputs. As shown in Figure 20. As a logic low on one side causes the corresponding pin on the other side to be pulled low, to avoid data-latching within the device, The output logic low (VOL) voltages of SDA1 and SCL1 are at least 60mV higher than the input threshold high (VIHT1) of SDA1 and SCL1, As shown in Figure 21.

Because the Side 2 logic levels/thresholds are standard I<sup>2</sup>C values, multiple  $\pi$ 220N61/ $\pi$ 221N61 devices connected to a bus by their Side 2 pins can communicate with each other and with other I<sup>2</sup>C compatible devices. However, because the Side 1 pin has a modified output level/ input threshold, this side of the  $\pi$ 220N61/ $\pi$ 221N61 can communicate only with devices that conform to the I<sup>2</sup>C standard.

The output low voltages of  $\pi$ 220N61/ $\pi$ 221N61 devices are guaranteed for sink currents of up to 35mA for side 2, and 3.5mA for side 1.

To enhance system reliability, it is recommended to connect the node with larger load capacitance and longer wires on side 2 for point-to-point communication.

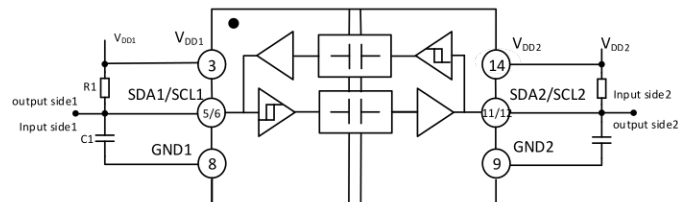


Figure 20.  $\pi$ 220N61 system operation diagram

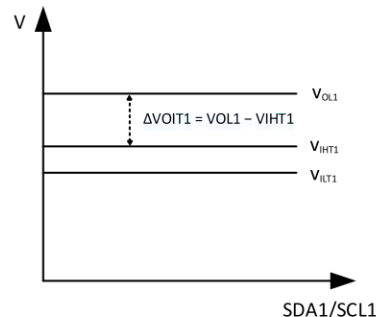


Figure 21.  $\pi$ 220N61/  $\pi$ 221N61 side 1 voltage Diagram

### TYPICAL APPLICATION DIAGRAM

Figure 22 shows a typical application circuit including the pull-up resistors required for both Side 1 and Side 2. Bypass capacitors with values from 0.1 $\mu$ F to 10 $\mu$ F are required between V<sub>DD1</sub> and GND1 and between V<sub>DD2</sub> and GND2. To enhance the robustness of a design, the user may connect a resistor (50-200  $\Omega$ ) in series between R2 and C1 and between R3 and C2 if the system is excessively noisy.

The  $\pi$ 220N61/ $\pi$ 221N61 are designed for operation at speeds up to 2 MHz. Due to the limited current available on side 1 and side2, operation at 2MHz limits the capacitance that can be driven at the minimum pull-up value to 40pF and 400pF.

Most applications operate at 100 kbps in standard mode or 400 kbps in fast mode. At these lower operating speeds, the limitation on the load capacitance can be significantly relaxed. If larger values for the pull up resistor are used, the maximum supported capacitance must be scaled down proportionately so that the rise time does not increase beyond the values required by the standard.

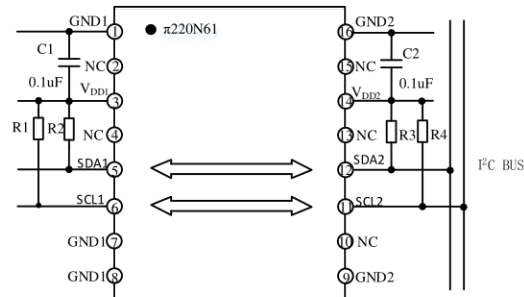


Figure 22. Typical Isolated I<sup>2</sup>C Interface Using the  $\pi$ 220N61

### OUTLINE DIMENSIONS

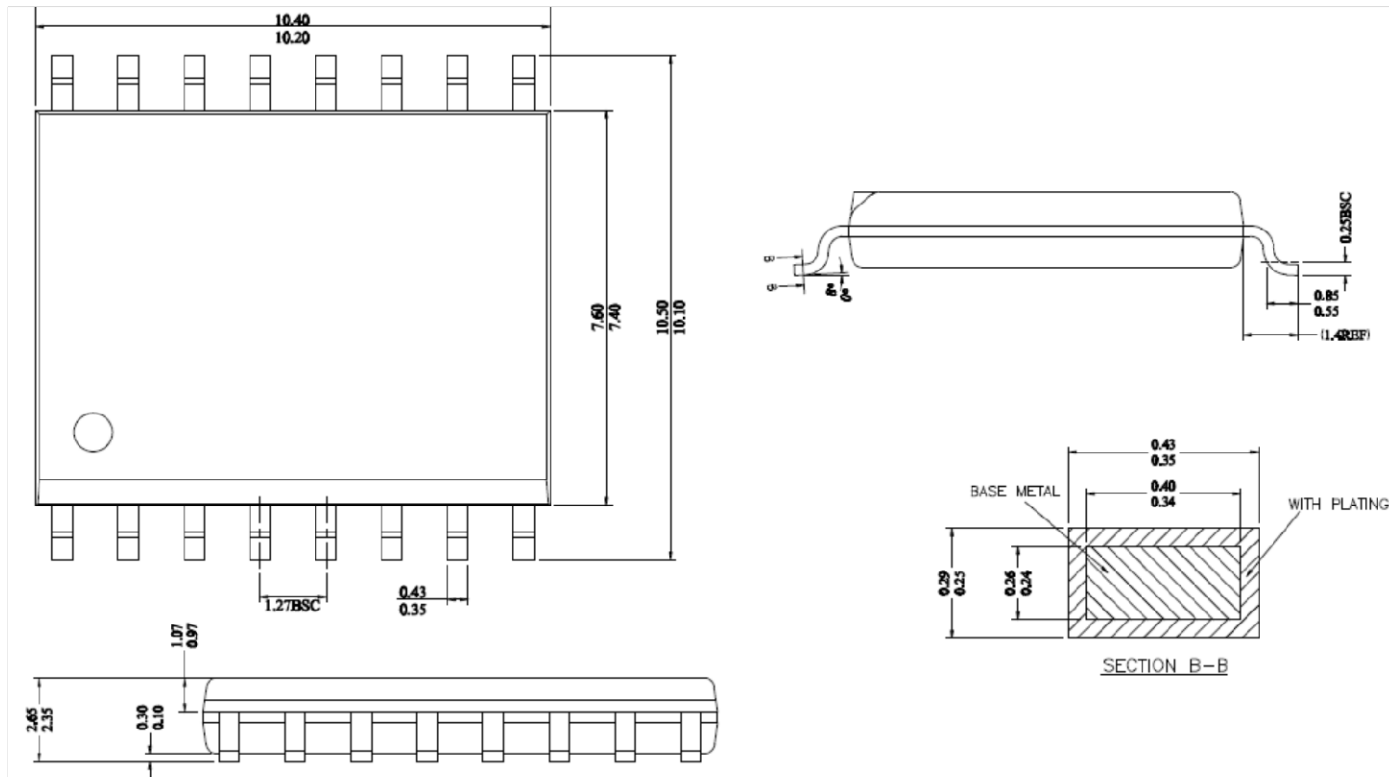


Figure 23. 16-Lead Wide Body SOIC [WB SOIC-16] Package—dimension unit(mm)

### Land Patterns

#### 16-Lead SOIC\_W [WB SOIC-16]

The figure below illustrates the recommended land pattern details for the  $\pi$ 16xxxx in a 16-pin wide-body SOIC package. The table lists the values for the dimensions shown in the illustration.

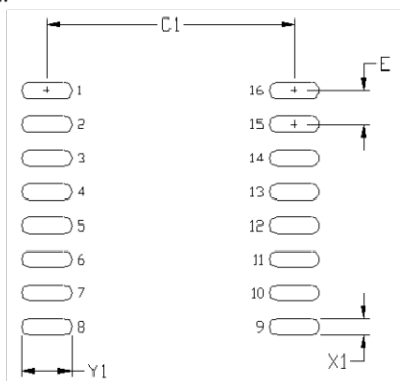


Figure 24.16-Lead Wide Body SOIC [WB SOIC-16] Land Pattern

Table 1.16-Lead SOIC\_W SOIC Land Pattern Dimensions

Dimension	Feature	Parameter	Unit
C1	Pad column spacing	9.40	mm
E	Pad row pitch	1.27	mm
X1	Pad width	0.60	mm
Y1	Pad length	1.90	mm

Note:

- 1.This land pattern design is based on IPC -7351
- 2.All feature sizes shown are at maximum material condition and a card fabrication tolerance of 0.05 mm is assumed.

### Top Marking

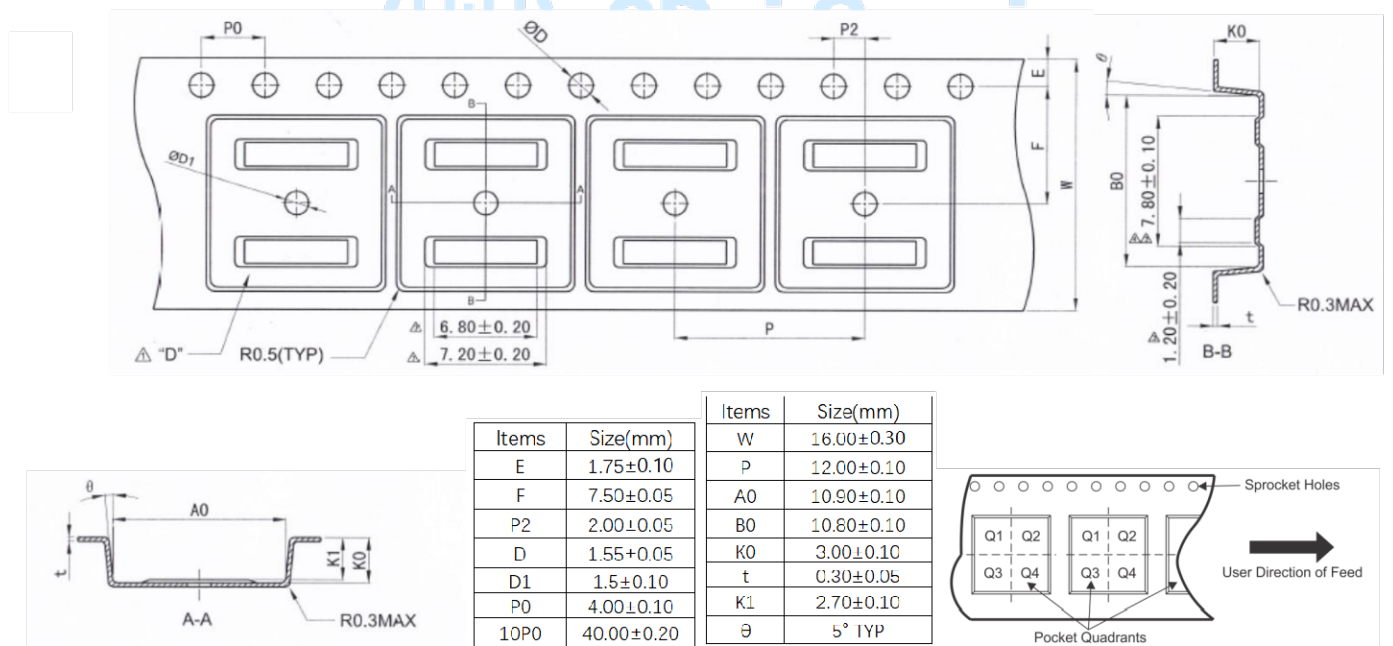


Line 1	$\pi 1xxxxxx$ =Product name
Line 2	YY = Work Year WW = Work Week ZZ=Manufacturing code from assembly house
Line 3	XXXX, no special meaning

Figure 25.Top Marking

### REEL INFORMATION

16-Lead SOIC\_W [WB SOIC-16]



Note: The Pin 1of the chip is in the quadrant Q1

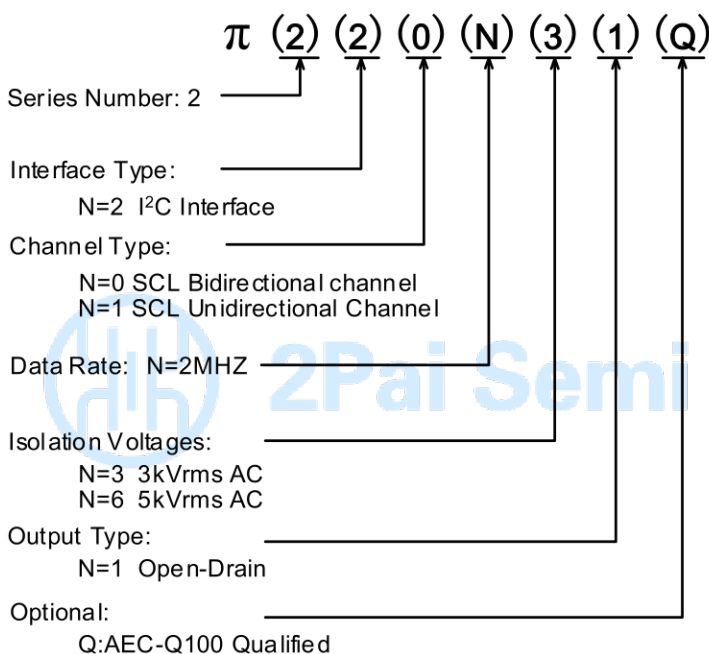
Figure 26.16-Lead Wide Body SOIC [WB SOIC-16] Reel Information

## ORDERING GUIDE

Model Name <sup>1</sup>		Temperature Range	No. of Inputs, V <sub>DD1</sub> Side	No. of Inputs, V <sub>DD2</sub> Side	Isolation Rating (kV rms)	Maximum Data Rate (MHZ)	Package Description	MSL Peak Temp <sup>2</sup>	MOQ/ Quantity per reel <sup>3</sup>
$\pi$ 220N61	Pai220N61	-40°C to +125°C	2	2	5	2	WB SOIC-16	Level-3-260C-168 HR	1500
$\pi$ 221N61	Pai221N61	-40°C to +125°C	2	1	5	2	WB SOIC-16	Level-3-260C-168 HR	1500

Note:  
<sup>1</sup> Pai2xxxx equals to  $\pi$ 2xxxx in the customer BOM  
<sup>2</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.  
<sup>3</sup> MOQ, minimum ordering quantity.

## PART NUMBER NAMED RULE



Notes:  
 Pai22xxxx equals to  $\pi$ 22xxxx in the customer BOM

Figure 27. Part Number Named Rule

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### REVISION HISTORY

Revision	Date	Page	Change Record
1.0	2020/02/24	All	Initial version
1.1	2021/05/17	Page6	Changed Regulatory Information

