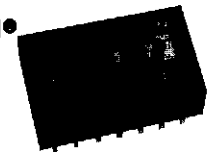
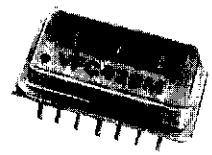
BURR-BROWN®





VFC42
VFC52

VOLTAGE-TO-FREQUENCY AND FREQUENCY-TO-VOLTAGE CONVERTER

FEATURES

- V/F OR F/V CONVERSION
- TWO FREQUENCY RANGES
  - 10kHz (VFC42)
  - 100kHz (VFC52)
- LOW NONLINEARITY
  - ±0.01% max (VFC42)
  - ±0.05% max (VFC52)
- MINIMAL EXTERNAL COMPONENTS REQUIRED
  - Add only one external resistor for V/F operation
- 6 DECADE DYNAMIC RANGE
- OUTPUT DTL/TTL/CMOS COMPATIBLE

DESCRIPTION

VFC42 and VFC52 are hybrid microcircuits which can be connected as voltage-to-frequency or frequency-to-voltage converters. They provide a simple, low cost method of converting analog signals into an equivalent digital form. The digital output is an open collector which can be made compatible with DTL, TTL, or CMOS logic. The output is a train of constant-amplitude, constant-width pulses whose repetition rate is proportional to the amplitude of the analog input voltage. In the frequency-to-voltage mode the pulses become the input and the proportional DC voltage, the output.

Both models are offered in epoxy (−25°C to +85°C) and hermetic metal (−25°C to +85°C and −55°C to +125°C) 14-pin DIP packages.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-390C

THEORY OF OPERATION

VFC42 and VFC52 hybrid voltage-to-frequency converters provide a digital pulse train output whose repetition rate is directly proportional to the analog input voltage. To understand the circuit's operation see Figure 1.

The input amplifier is connected in an integrator configuration. When a positive input voltage is applied at V_{IN}, a constant current flows through the input resistor causing voltage at f_{IN} to ramp down toward zero, according to $dV/dt = V_{IN}/R_1C_2$. During this time the constant current sink is disabled by the switch. When the ramp reaches zero volts, the comparator causes the one-shot to fire. The f_{out} signal then changes states, going from logic 0 to logic 1 and the switch closes, enabling the constant current sink. Ramp voltage then changes direction and begins to ramp up. Since V_{IN}/R_1 is always set to be less than 1mA, current in the integrating capacitor flows toward the summing junction and ramp voltage range of change will be

$$\frac{dV}{dt} = \frac{\left(\frac{V_{in}}{R_1}\right) - 1mA}{C_2}$$

Before the ramp voltage can saturate the input amplifier, the one-shot resets, disabling the current sink, changing the output state back to logic 0 and restarting the cycle.

To operate VFC42 and VFC52 as highly linear frequency-to-voltage converters, open the connection between V_{OUT} and F_{IN} and connect V_{IN} to V_{OUT}. The input frequency should be coupled through a capacitor to f_{IN}. A positive output voltage proportional to f_{IN} will be generated at the V_{OUT} connection. An external capacitor connected between pins 13 and 14 (paralleling C2) should be added to reduce output ripple. Refer to Operating Instructions for detailed information on F/V operation.

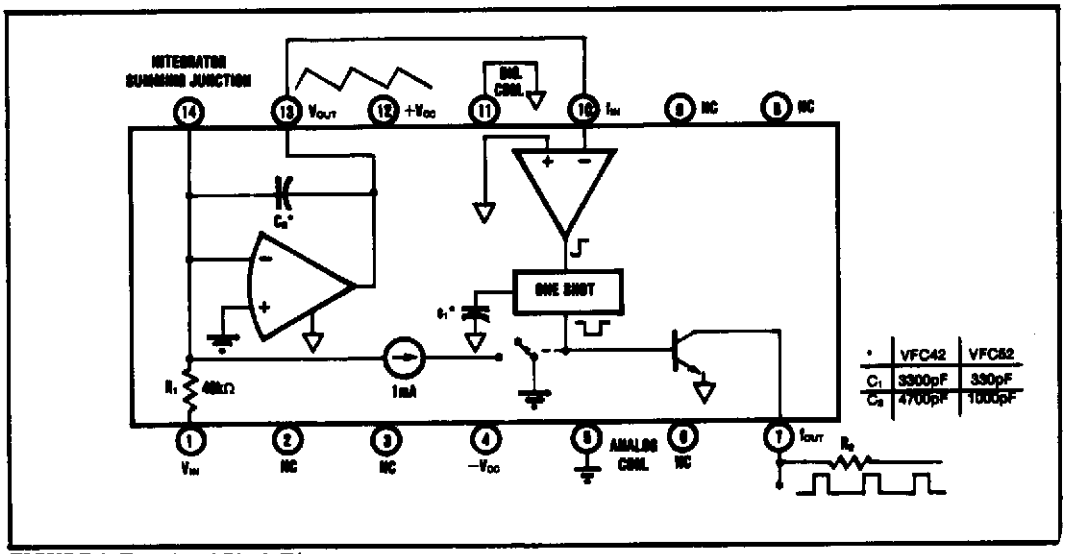


FIGURE 1. Functional Block Diagram.

DISCUSSION OF SPECIFICATIONS

LINEARITY

Linearity, the maximum deviation of the actual transfer function from a straight line drawn between the end points (full scale input and zero input), is the true measure of a FVC's performance and is a function of full scale frequency. The high linearity of VFC42 and VFC52 makes these devices an excellent choice for use in A/D converters with 10 (0.05%) and 12 bit (0.012%) accuracy and for highly accurate analog data transfer over long lines in noisy environments.

FREQUENCY STABILITY VS TEMPERATURE

Frequency stability vs temperature is expressed as parts per million of full scale range per °C. Since frequency drift is a function of the specified temperature range, the "SM" models will meet the lower drift specifications of the "BM" models over the narrower −25°C to +85°C temperature range. Error sources do not drift linearly over temperature, consequently the units drift much less at higher temperatures.

RESPONSE TIME

Response time of VFC42 and VFC52 to input signal level changes is specified for a full scale step and is 1μsec plus 1 period of the new frequency. Typical settling time to within rated linearity for a positive input voltage step of +10V is 101μsec for VFC42 and 11μsec for VFC52.

SPECIFICATIONS

ELECTRICAL

Specifications at T_A = +25°C, and ±15VDC power supplies unless otherwise noted.

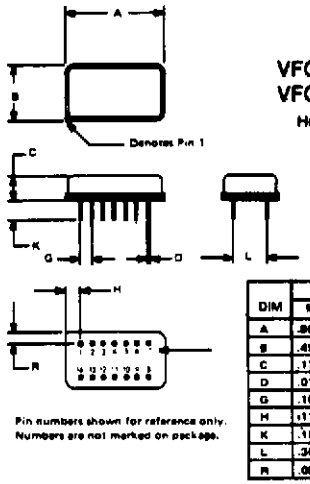
MODEL	VFC42			VFC52			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
Full Scale Frequency		10			100		kHz
INPUT							
Analog Input (V/F)							
Voltage Range	0		10	0		+10	V
Current Range	0		+0.25	0		+0.25	mA
Input Bias Current (pin 14) Inverting Input		6	8		6	8	nA
Input Offset Voltage (trimmable to zero)		100	200		100	200	µV
Input Impedance (pin 1)	32	40	48	32	40	48	kΩ
Frequency Input (F/V) (pin 10)							
Logic Levels: Logic "0"	$-V_{CC}$		−0.6	$-V_{CC}$		−0.6	V
Logic "1"	+1.0		$+V_{CC}$	+1.0		$+V_{CC}$	V
Pulse Width Range (t_p, Fig. 6)	0.1		15	0.1		1.5	µsec
Impedance	1 ‖ 10	1.2 ‖ 10		1 ‖ 10	1.2 ‖ 10		MΩ ‖ pF
TRANSFER CHARACTERISTICS							
Transfer Functions	$f_{OUT} = V_{IN}(1.00 \times 10^3)$ $V_{OUT} = f_{IN}(10 \times 10^{-4})$			$f_{OUT} = V_{IN}(1.00 \times 10^4)$ $V_{OUT} = f_{IN}(10 \times 10^{-4})$			Hz VDC
Accuracy							
Full Scale Gain (adjustable to zero)		0.1	0.2		0.1	0.2	%
Linearity Error: 0.01Hz ≤ F ≤ 10kHz		0.005	0.01				% of FSR[1]
0.1Hz ≤ F ≤ 100kHz					0.025	0.05	% of FSR
Offset Error (pin 1)		0.001	0.002		0.001	0.002	% of FSR
Power Supply Sensitivity[2]			0.015			0.015	% of FSR/%
Temperature Stability							
Analog Input							
Full Scale Drift (gain and offset)							
Grade: BP (hot/cold)[3]		±15/±50	±30/±100		±20/±50	±30/±150	ppm/°C
BM		±15/±50	±30/±100		±20/±50	±30/±150	ppm/°C
SM		±30/±60	±50/±100		±30/±60	±50/±150	ppm/°C
Offset Drift							
Grade: BP		±1	±3		±1	±3	ppm of FSR/°C
BM		±1	±3		±1	±3	ppm of FSR/°C
SM		±1	±3		±1	±3	ppm of FSR/°C
Frequency Input							
Full Scale Drift (gain and offset)							
Grade: BP (hot/cold)[3]		±15/±50	±30/±100		±20/±50	±30/±150	ppm/°C
BM		±15/±50	±30/±100		±20/±50	±30/±150	ppm/°C
SM		±30/±60	±50/±100		±30/±60	±50/±150	ppm/°C
Dynamic Response							
Settling Time to within linearity specification for full scale input step	1 period of new frequency + 1µsec			1 period of new frequency + 1µsec			
Overload Recovery Time	1 period of new frequency + 1µsec			1 period of new frequency + 1µsec			
OUTPUT							
Voltage Output							
Voltage Range ($I_O \leq 5mA$)	0 to +10			0 to +10			V
Output Current ($V_O \leq 7V$)	+10			+10			mA
Output Impedance (closed loop)			1			1	Ω
Capacitive Load			100			100	pF
Frequency Output (open collector)							
Pulse Characteristics: Logic "1"			$+V_{PULL-UP}$			$+V_{PULL-UP}$	V
Logic "0" (at $I_O \leq -8mA$)	0		+0.4	0		+0.4	V
Pulse Width	20	25		2.0	2.5		µsec
Output Sink Current (Logic "0", ≤ 0.4V)			8			8	mA
Output Leakage Current (Logic "1")			1			1	µA
Fall Time ($I_{OUT} = -5mA$, $C_{LOAD} = 500pF$)			400			400	nsec
POWER SUPPLY REQUIREMENTS							
Rated Supplies		±15			±15		V
Supply Range	±9		±20	±9		±20	V
Supply Drain (independent of operating frequency)		±6.5	±7.5		±6.5	±7.5	mA
TEMPERATURE RANGE							
Specification: BP, BM	−25		+85	−25		+85	°C
SM	−55		+125	−55		+125	°C
Operating: BM, SM	−55		+125	−55		+125	°C
BP	−55		+100	−55		+100	°C
Storage: BM, SM	−55		+125	−55		+125	°C
BP	−25		+85	−25		+85	°C

NOTES: (1) % of FSR = % of Full Scale Range. (2) Rated at full scale input and ±15V supplies. (3) Hot = +20°C to highest rated temperature; cold = lowest rated temperature to +20°C.

ABSOLUTE MAXIMUM RATINGS

Supply Voltages	±22V
Output Sink Current (F_{output})	50mA
Output Current (V_{output})	+20mA
Input Voltage, Pin 14	±Supply
Input Voltage, Pin 1	±Supply
Storage Temperature Range	
Grade: BM, SM	−55°C to +125°C
BP	−25°C to +85°C

MECHANICAL



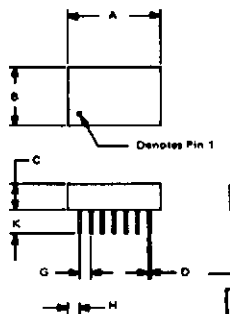
VFC42BM, VFC42SM
VFC52BM, VFC52SM

Hermetic Metal Package
14-Pin DIP

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.860	.880	21.84	22.35
B	.490	.510	12.46	12.95
C	.170	.260	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.115	.165	2.92	3.84
K	.150	.300	3.81	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.120	2.03	3.05

Pin numbers shown for reference only.
Numbers are not marked on package.

Tolerance (inches): .xxx ±0.005; .xx ±0.02
Connector: 14-pin DIP (145MC)
Case Material: Base - gold plated kovar, Cap - nickel-plated kovar or steel
Pin material and plating compositions: Conforms to MIL-STD-883, Method 2003 (solderability) except paragraph 3.2 (aging).
Hermeticity: Conforms to MIL-STD-883, Method 1014, Condition C, Step 1, Fluorocarbon (gross leak).



VFC42BP, VFC52BP

Epoxy Package
14-Pin DIP

Pin material and plating composition:
Conform to Method 2003 (solderability)
of MIL-STD-883 (except paragraph 3.2).

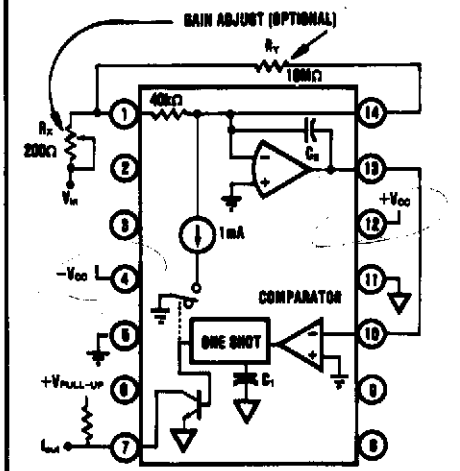
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.790	.810	20.07	20.57
B	.490	.510	12.45	12.95
C	.190	.260	4.83	6.60
D	.016	.021	0.46	0.53
G	.100 BASIC		2.54 BASIC	
H	.080	.115	2.03	2.92
K	.130	.300	3.30	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.115	2.03	2.92

Pin numbers shown for reference only.
Numbers are not marked on package.

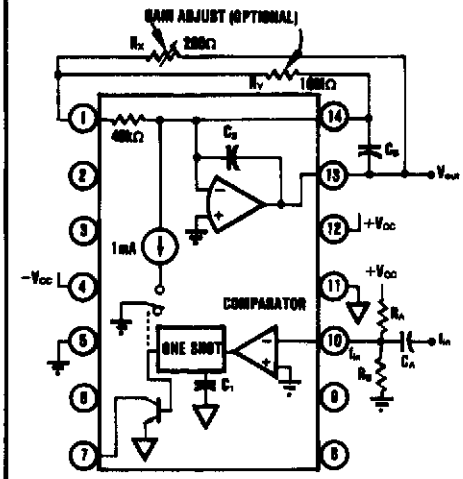
Tolerance (inches): .xxx ±0.005
.xx ±0.02
Connector: 14-pin DIP (145MC)
Case Material: Epoxy

CONNECTION DIAGRAMS

V/F Operation



F/V Operation



OPERATING INSTRUCTIONS

VFC42 and VFC52 can be connected for either V/F or F/V operation. Only one external component, the output pull-up resistor, is required for V/F operation. F/V operation requires the pull-up resistor and input biasing components. Gain error is the most significant error in either configuration and may be nulled out with the optional trim circuit (R_X and R_Y). The offset error is laser trimmed at the factory and no external adjustment is required.

Power Supply Consideration: Power supplies stable to within ±1% are recommended to maintain conversion accuracy. Each supply should be bypassed with 0.01μF capacitors located as close to the VFC as possible.

VOLTAGE-TO-FREQUENCY OPERATION

Calculating the Value of Pull-Up Resistor, R_P: The open collector output can be used to drive DTL, TTL, CMOS or discrete circuits. The maximum collector current allowed for TTL circuits in logic 0 is 8mA. R_P may be calculated by this equation:

$$R_P \text{ min} = V \text{ pull-up}/(8mA - i_{LOAD}).$$

A 10% carbon composition resistor is suitable for this purpose. The collector current may be as great as 30mA if a logic 0 voltage of 1.0V is tolerable.

Gain Adjustment Procedure: Connect R_X and R_Y as shown in Connection Diagram. Apply positive full scale voltage to the input and adjust R_X until 10kHz ±1Hz (VFC42) or 100kHz ±10Hz (VFC52) is obtained at f_{OUT}. R_X and R_Y should have temperature coefficients of <500ppm. These external components will add less than 5ppm/°C to temperature drift.

FREQUENCY-TO-VOLTAGE OPERATION

Input Characteristics: VFC42 and VFC52 can be connected as frequency-to-voltage converters as shown in Connection Diagram. f_{IN} should be a positive pulse train with minimum pulse width of 1.0μsec and rise and fall times of ≤ 300nsec. The input train (f_{IN}) is differential and applied to the input of the comparator (pin 10) (see Figure 2). Threshold voltage of the comparator lies between −0.6 and +1.0V. When comparator input is less than −0.6V it triggers the one-shot.

Selecting R_A, R_B, and C_A Input components R_A, R_B and C_A are selected so that the trigger voltage (V_T) is more negative than −0.6V and transition time (t_2) is between 0.3μsec and 15μsec for VFC42 and between 0.3μsec and 1.5μsec for VFC52. Table I give values for input components for several common signal sources. Values for R_A, R_B and C_A may be selected by the user when input signal characteristics differ from those listed. Conditions described above for trigger voltage and transition time must be observed.

TABLE I. F/V Input Component Selection

Input Type	V_{INPUT} (V)		V_{BIAS} (V)	VFC42			VFC52		
	Low	High		R_A (kΩ)	R_B (kΩ)	C_A (pF)	R_A (kΩ)	R_B (Ω)	C_A (pF)
TTL	≤+0.4	≥+2.8	+1.1	12	1.0	1000	8.2	680	680
6V CMOS	≤+0.5	≥+4.5	+1.2	18	1.6	2200	9.1	820	680
10V CMOS	≤+1.0	≥+9.0	+1.1	12	1.0	2200	6.2	510	680
15V CMOS	≤+1.5	≥+13.5	+1.1	12	1.0	2200	6.2	510	680

Equations to calculate trigger voltage and transition time are:

$$V_T = V_B + V_{in}(e^{-t_1/\tau} - 1)$$

$$t_2 = -\tau \ln\left[\frac{1 - V_B}{V_{in}(e^{-t_1/\tau} - 1)}\right]$$

V_B = Bias voltage on pin 10

V_{in} = Input pulse amplitude

t_1 = Input pulse width

τ = Time constant of R_A, R_B C_A as connected

If input pulse amplitude is greater than $+V_{CC} - 1V$, a voltage larger than $+V_{CC}$ will be applied to pin 10. Since this may damage the unit, a diode connected across R_A with the cathode tied to $+V_{CC}$ is required.

Output Characteristics: Selecting C_B: Output ripple voltage amplitude is inversely proportional to the input frequency and to the value of the integrating capacitance, $C_2 + C_B$. Conversely, time required for the output to settle is directly proportional to the value of $C_2 + C_B$ and is least with small values of $C_2 + C_B$. There is, therefore, a trade-off between output ripple amplitude and output settling time.

Because ripple amplitude is greatest at lowest input frequency it is at this point where the trade-off will usually be made. Ripple voltage and integrating capacitance value are related in this manner:

$$C_B = \frac{-(25 \times 10^{-6})t_{sec}}{\ln\left[1 - \frac{V_{Ripple}}{30V}\right]} \text{ farads}$$

where t is equal to 25μsec in the VFC42 and 2.5μsec in the VFC52 and C is the integrating capacitance.

Calculating output response time versus integrating capacitance is an iterative process and is plotted in Figure 3. These curves are for zero to full scale input frequency transitions. If faster response time with lower ripple voltage is desired, a low-pass filter can be connected in series with the output.

Gain Adjustment Procedure: Connect R_X and R_Y as shown in Connection Diagram. Apply full scale frequency to the input and adjust R_X until the full scale voltage is +10V ±1mV (discounting ripple). R_X and R_Y should have temperature coefficients of < 500ppm. These external components will add less than 5ppm/°C to temperature drift.

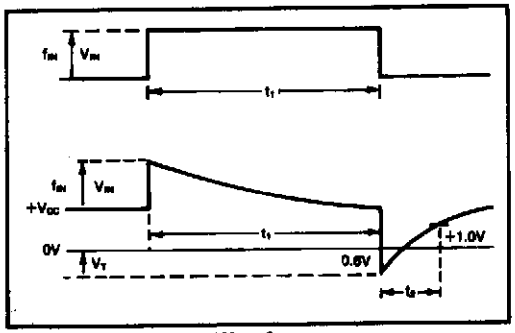


FIGURE 2. F/V Input Waveforms.

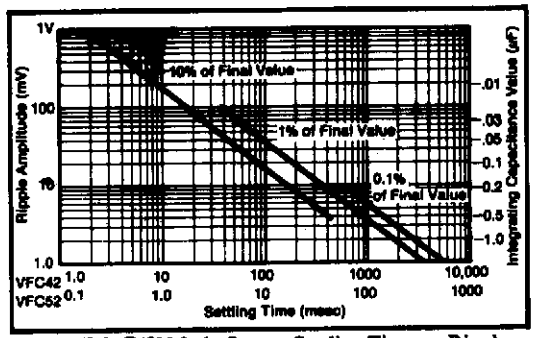


FIGURE 3. F/V Mode Output Settling Time vs. Ripple Voltage Amplitude for Full Scale Frequency Change.

APPLICATION

VFC42 and VFC52 can be used to convert analog data into a digital pulse train for transmission over long lines through high EMI environments. Illustrated in Figure 4 is a V/F, F/V combination that can be used to transmit analog data of 0 to +10V over a 100Ω shielded, twisted-pair. The voltage ripple amplitude at the output will be 10mV for a 10V output and the settling time for a full scale 0 to +10V change is 60 milliseconds.

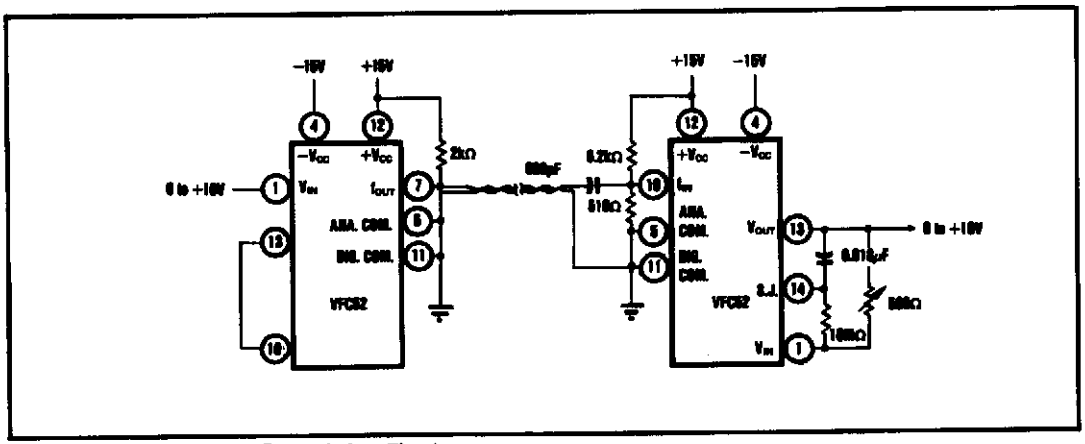


FIGURE 4. V/F, F/V Data Transmission Circuit.