

ZXMHC6A07N8

60V SO8 Complementary enhancement mode MOSFET H-Bridge

Summary

Device	$V_{(BR)DSS}$	Q_G	$R_{DS(on)}$	I_D $T_A = 25^\circ C$
N-CH	60V	3.2nC	0.25Ω @ $V_{GS} = 10V$	1.8A
			0.35Ω @ $V_{GS} = 4.5V$	1.5A
P-CH	-60V	5.1nC	0.40Ω @ $V_{GS} = -10V$	-1.4A
			0.60Ω @ $V_{GS} = -4.5V$	-1.2A



Description

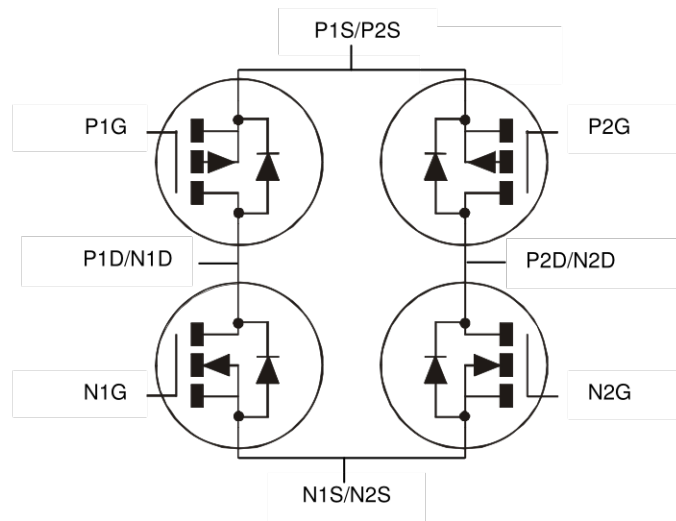
This new generation complementary MOSFET H-Bridge features low on-resistance achievable with low gate drive.

Features

- 2 x N + 2 x P channels in a SOIC package

Applications

- DC Motor control
- DC-AC Inverters

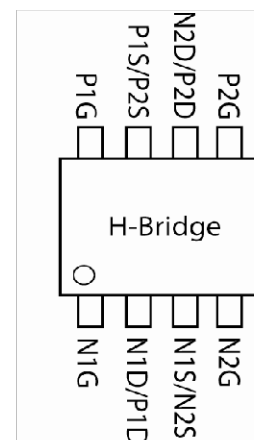


Ordering information

Device	Reel size (inches)	Tape width (mm)	Quantity per reel
ZXMHC6A07N8TC	13	12	2,500

Device marking

ZXMHC
6A07



Absolute maximum ratings

Parameter	Symbol	N-channel	P-channel	Unit
Drain-Source voltage	V_{DSS}	60	-60	V
Gate-Source voltage	V_{GS}	± 20	± 20	V
Continuous Drain current @ $V_{GS}=10V$; $T_A=25^\circ C$ ^(b) @ $V_{GS}=10V$; $T_A=70^\circ C$ ^(b) @ $V_{GS}=10V$; $T_A=25^\circ C$ ^(a) @ $V_{GS}=10V$; $T_L=25^\circ C$ ^(f)	I_D	1.80 1.40 1.39 1.42	-1.42 -1.28 -1.28 -1.33	A
Pulsed Drain current @ $V_{GS}=10V$; $T_A=25^\circ C$ ^(c)	I_{DM}	7.10	-6.03	A
Continuous Source current (Body diode) at $T_A=25^\circ C$ ^(b)	I_S	1.00	-1.00	A
Pulsed Source current (Body diode) at $T_A=25^\circ C$ ^(c)	I_{SM}	7.10	-6.03	A
Power dissipation at $T_A=25^\circ C$ ^(a) Linear derating factor	P_D	0.87 6.94		W mW/ $^\circ C$
Power dissipation at $T_A=25^\circ C$ ^(b) Linear derating factor	P_D	1.36 10.9		W mW/ $^\circ C$
Power dissipation at $T_L=25^\circ C$ ^(f) Linear derating factor	P_D	0.90 7.19		W mW/ $^\circ C$
Operating and storage temperature range	T_j, T_{stg}	-55 to 150		$^\circ C$

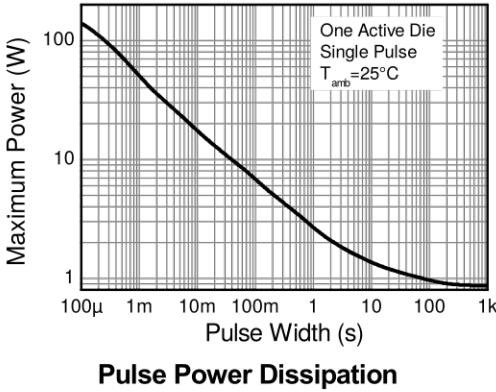
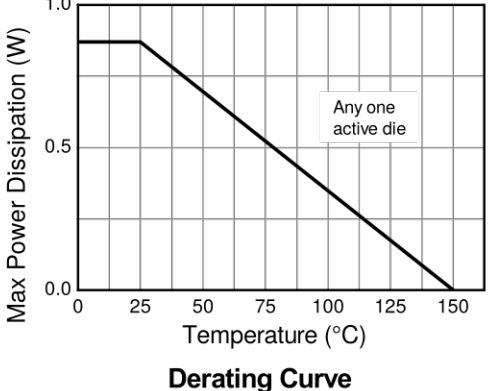
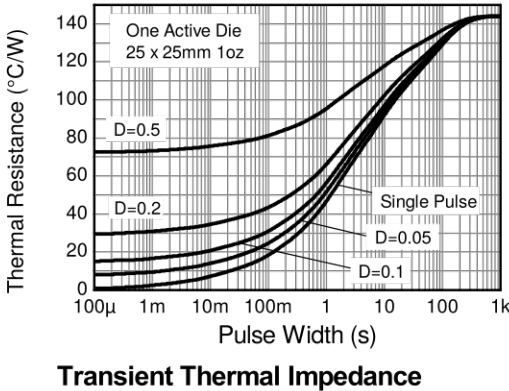
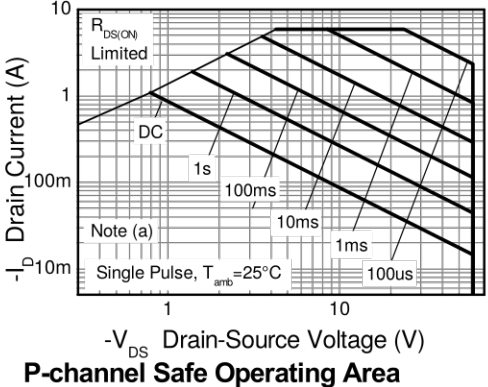
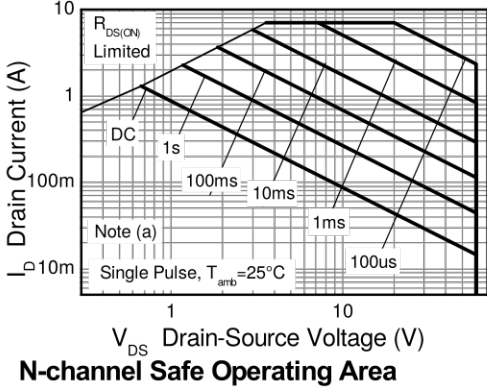
Thermal resistance

Parameter	Symbol	Value	Unit
Junction to ambient ^(a)	$R_{\theta JA}$	144	$^\circ C/W$
Junction to ambient ^(b)	$R_{\theta JA}$	92	$^\circ C/W$
Junction to ambient ^(d)	$R_{\theta JA}$	106	$^\circ C/W$
Junction to ambient ^(e)	$R_{\theta JA}$	254	$^\circ C/W$
Junction to lead ^(f)	$R_{\theta JL}$	139	$^\circ C/W$

NOTES:

- For a device surface mounted on 25mm x 25mm x 1.6mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions with the heat-sink split into two equal areas (one for each drain connection); the device is measured when operating in a steady-state condition with one active die.
- Same as note (a), except the device is measured at $t \leq 10$ sec.
- Same as note (a), except the device is pulsed with $D=0.02$ and pulse width 300 μs . The pulse current is limited by the maximum junction temperature.
- For a device surface mounted on 50mm x 50mm x 1.6mm FR4 PCB with high coverage of single sided 2oz copper, in still air conditions with the heat-sink split into two equal areas (one for each drain connection); the device is measured when operating in a steady-state condition with one active die.
- For a device surface mounted on minimum copper 1.6mm FR4 PCB, in still air conditions; the device is measured when operating in a steady-state condition with one active die.
- Thermal resistance from junction to solder-point (at the end of the drain lead); the device is operating in a steady-state condition with one active die.

Thermal characteristics



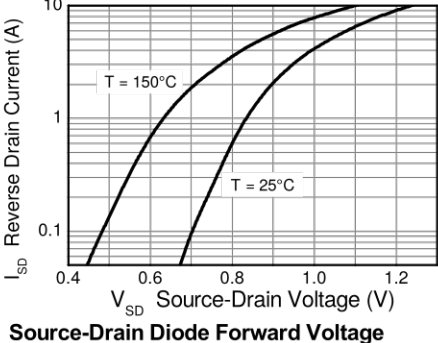
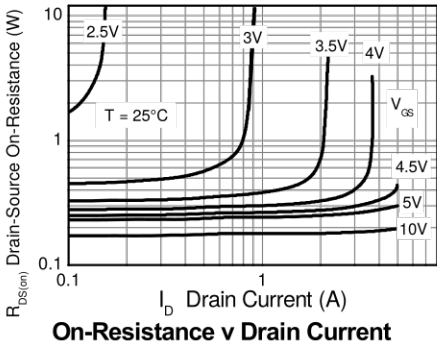
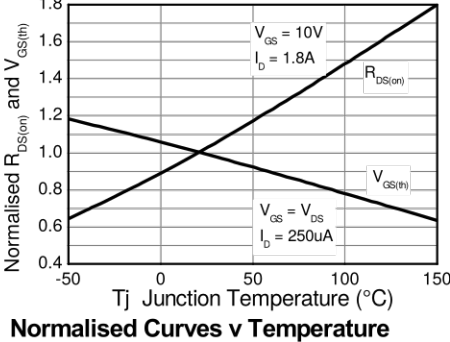
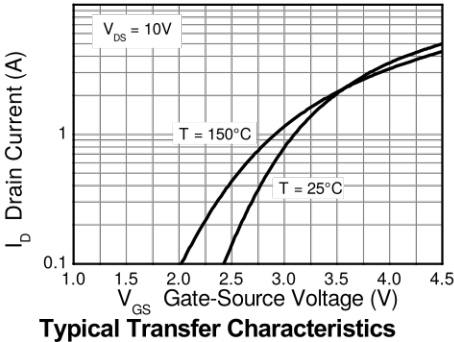
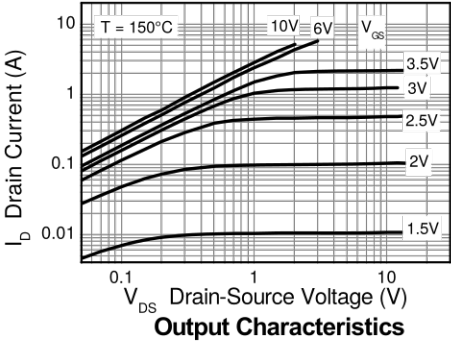
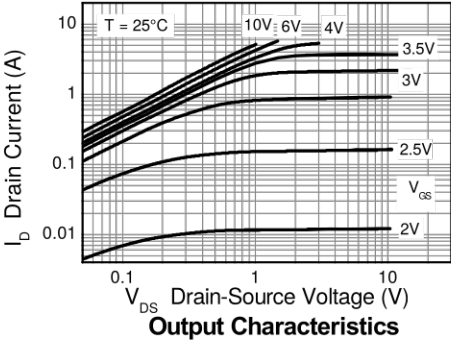
N-channel electrical characteristics (at $T_{amb} = 25^{\circ}\text{C}$ unless otherwise stated)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Static						
Drain-Source breakdown voltage	$V_{(BR)DSS}$	60			V	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$
Zero Gate voltage Drain current	I_{DSS}			0.5	μA	$V_{DS} = 60\text{V}$, $V_{GS} = 0\text{V}$
Gate-Body leakage	I_{GSS}			± 100	nA	$V_{GS} = \pm 20\text{V}$, $V_{DS} = 0\text{V}$
Gate-Source threshold voltage	$V_{GS(th)}$	1.0		3.0	V	$I_D = 250\mu\text{A}$, $V_{DS} = V_{GS}$
Static Drain-Source on-state resistance ^(a)	$R_{DS(on)}$			0.25 0.35	Ω	$V_{GS} = 10\text{V}$, $I_D = 1.8\text{A}$ $V_{GS} = 4.5\text{V}$, $I_D = 1.3\text{A}$
Forward Transconductance ^{(a) (c)}	g_{fs}		2.3		S	$V_{DS} = 15\text{V}$, $I_D = 1.8\text{A}$
Dynamic						
Capacitance ^(c)						
Input capacitance	C_{iss}		166		pF	$V_{DS} = 40\text{V}$, $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$
Output capacitance	C_{oss}		19.5		pF	
Reverse transfer capacitance	C_{rss}		8.7		pF	
Switching ^{(b) (c)}						
Turn-on-delay time	$t_{d(on)}$		1.8		ns	$V_{DD} = 30\text{V}$, $V_{GS} = 10\text{V}$ $I_D = 1.8\text{A}$ $R_G \cong 6.0\Omega$,
Rise time	t_r		1.4		ns	
Turn-off delay time	$t_{d(off)}$		4.9		ns	
Fall time	t_f		2.0		ns	
Gate charge ^(c)						
Total Gate charge	Q_g		3.2		nC	$V_{DS} = 30\text{V}$, $V_{GS} = 10\text{V}$ $I_D = 1.8\text{A}$
Gate-Source charge	Q_{gs}		0.67		nC	
Gate-Drain charge	Q_{gd}		0.82		nC	
Source-Drain diode						
Diode forward voltage ^(a)	V_{SD}		0.80	0.95	V	$I_S = 0.45\text{A}$, $V_{GS} = 0\text{V}$
Reverse recovery time ^(c)	t_{rr}		20.5		ns	$I_S = 1.8\text{A}$, $di/dt = 100\text{A}/\mu\text{s}$
Reverse recovery charge ^(c)	Q_{rr}		21.3		nC	

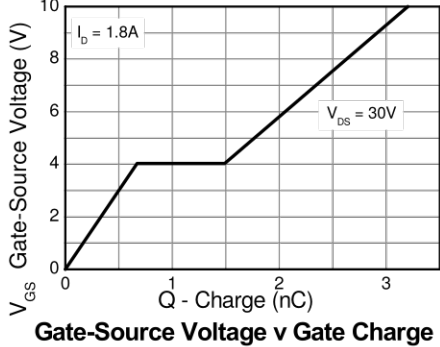
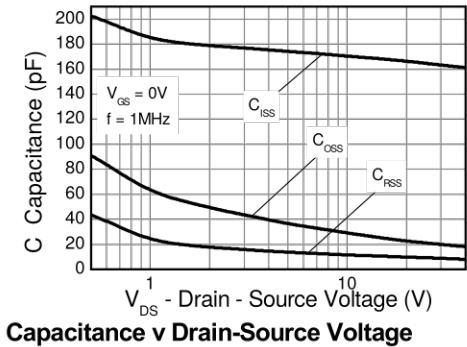
NOTES:

- (a) Measured under pulsed conditions. Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
 (b) Switching characteristics are independent of operating junction temperature.
 (c) For design aid only, not subject to production testing

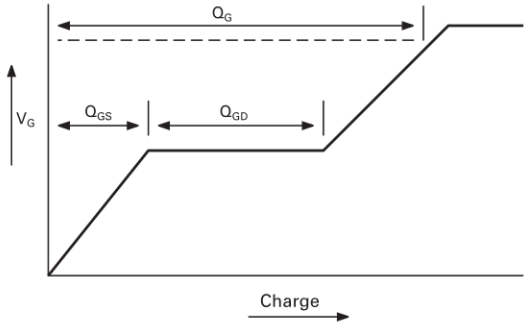
N-channel typical characteristics



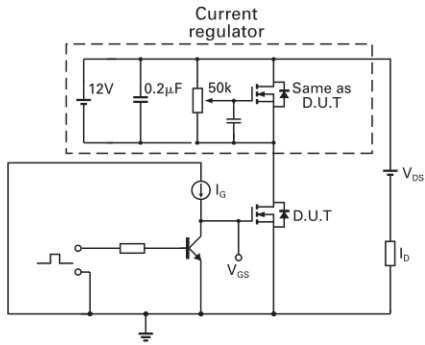
N-channel typical characteristics –continued



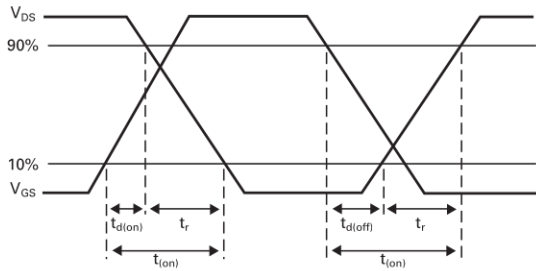
Test circuits



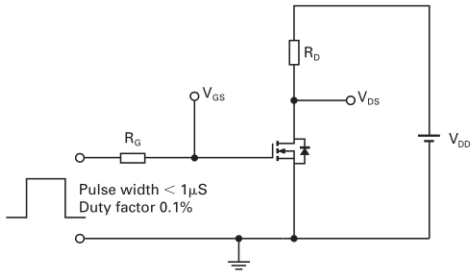
Basic gate charge waveform



Gate charge test circuit



Switching time waveforms



Switching time test circuit

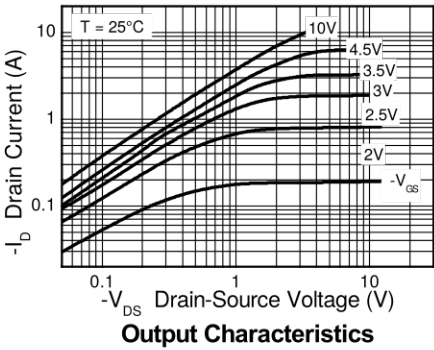
P-channel electrical characteristics (at $T_{amb} = 25^{\circ}\text{C}$ unless otherwise stated)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Static						
Drain-Source breakdown voltage	$V_{(BR)DSS}$	-60			V	$I_D = -250\mu\text{A}$, $V_{GS} = 0\text{V}$
Zero Gate voltage Drain current	I_{DSS}			-0.5	μA	$V_{DS} = -60\text{V}$, $V_{GS} = 0\text{V}$
Gate-Body leakage	I_{GSS}			± 100	nA	$V_{GS} = \pm 20\text{V}$, $V_{DS} = 0\text{V}$
Gate-Source threshold voltage	$V_{GS(th)}$	-1.0		-3.0	V	$I_D = -250\mu\text{A}$, $V_{DS} = V_{GS}$
Static Drain-Source on-state resistance ^(a)	$R_{DS(on)}$			0.40 0.60	Ω	$V_{GS} = -10\text{V}$, $I_D = -0.9\text{A}$ $V_{GS} = -4.5\text{V}$, $I_D = -0.8\text{A}$
Forward Transconductance ^{(a) (c)}	g_{fs}		1.8		S	$V_{DS} = -15\text{V}$, $I_D = -0.9\text{A}$
Dynamic						
Capacitance ^(c)						
Input capacitance	C_{iss}		141		pF	$V_{DS} = -50\text{V}$, $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$
Output capacitance	C_{oss}		13.1		pF	
Reverse transfer capacitance	C_{rss}		10.8		pF	
Switching ^{(b) (c)}						
Turn-on-delay time	$t_{d(on)}$		1.6		ns	$V_{DD} = -30\text{V}$, $V_{GS} = -10\text{V}$ $I_D = -1.0\text{A}$ $R_G \cong 6.0\Omega$
Rise time	t_r		2.3		ns	
Turn-off delay time	$t_{d(off)}$		13		ns	
Fall time	t_f		5.8		ns	
Gate charge ^(c)						
Total Gate charge	Q_g		5.1		nC	$V_{DS} = -30\text{V}$, $V_{GS} = -10\text{V}$ $I_D = -0.9\text{A}$
Gate-Source charge	Q_{gs}		0.7		nC	
Gate-Drain charge	Q_{gd}		0.7		nC	
Source-Drain diode						
Diode forward voltage ^(a)	V_{SD}		-0.85	-0.95	V	$I_S = -0.8\text{A}$, $V_{GS} = 0\text{V}$
Reverse recovery time ^(c)	t_{rr}		22.6		ns	$I_S = -0.9\text{A}$, $di/dt = 100\text{A}/\mu\text{s}$
Reverse recovery charge ^(c)	Q_{rr}		23.2		nC	

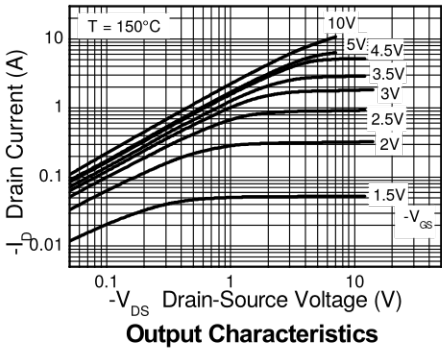
NOTES:

- (a) Measured under pulsed conditions. Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
 (b) Switching characteristics are independent of operating junction temperature.
 (c) For design aid only, not subject to production testing

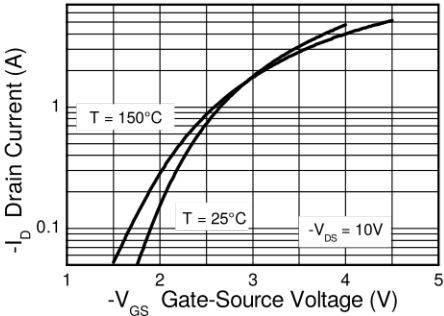
P-channel typical characteristics



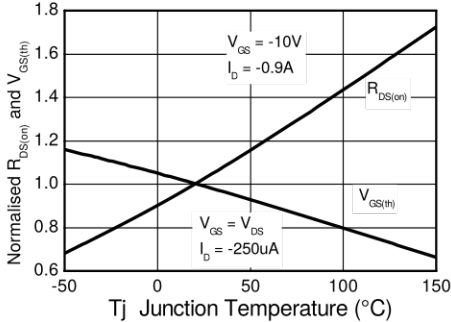
Output Characteristics



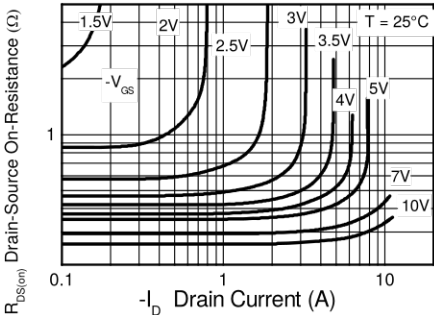
Output Characteristics



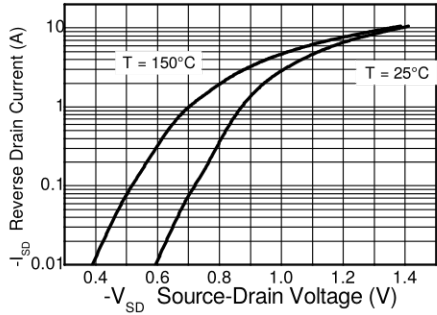
Typical Transfer Characteristics



Normalised Curves v Temperature

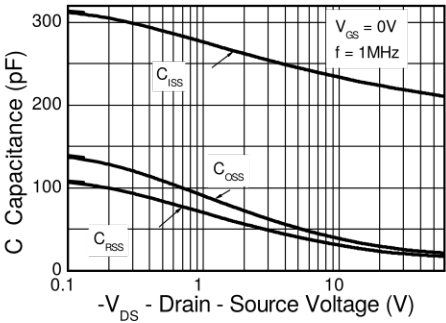


On-Resistance v Drain Current

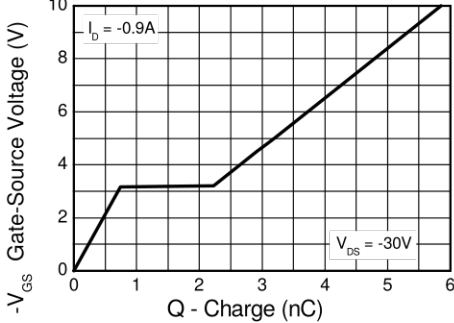


Source-Drain Diode Forward Voltage

P-channel typical characteristics –continued

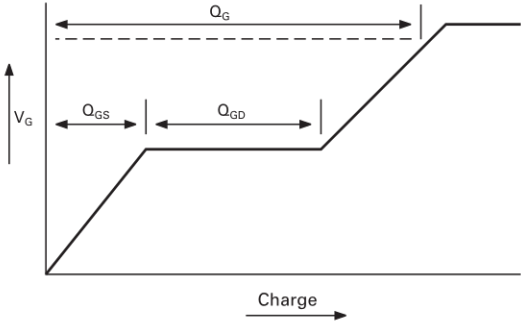


Capacitance v Drain-Source Voltage

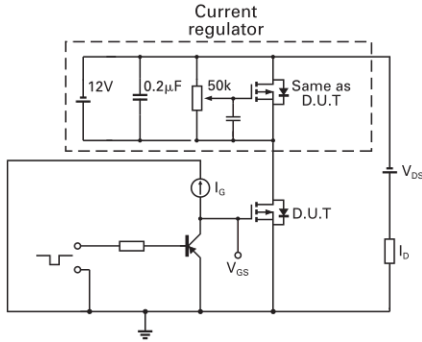


Gate-Source Voltage v Gate Charge

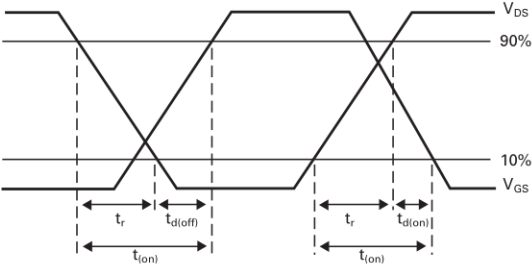
Test circuits



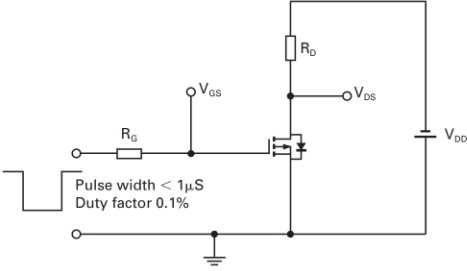
Basic gate charge waveform



Gate charge test circuit

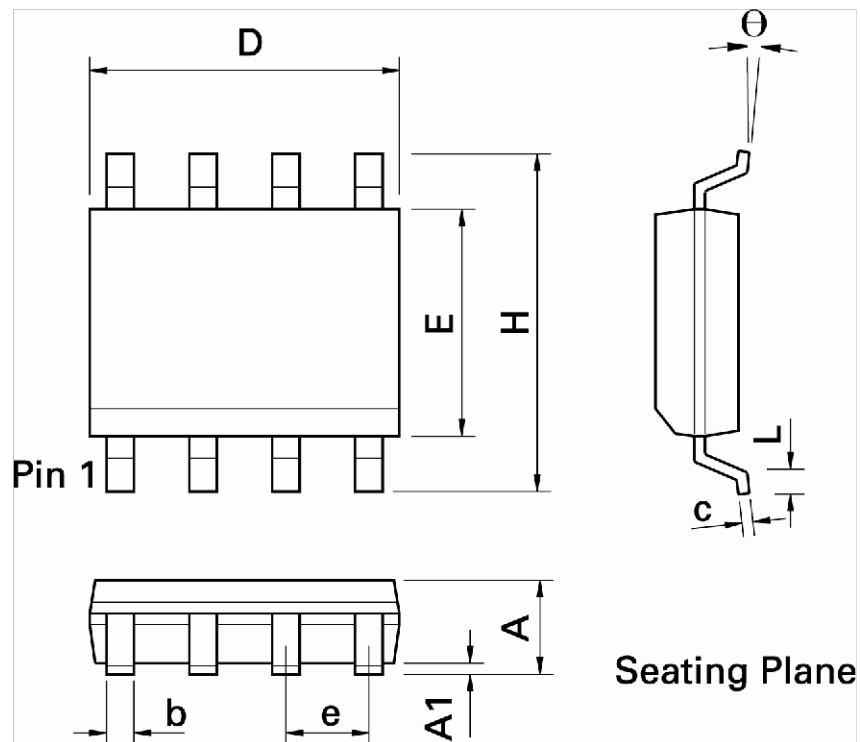


Switching time waveforms



Switching time test circuit

Packaging details - SO8



DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.053	0.069	1.35	1.75	e	0.050 BSC		1.27 BSC	
A1	0.004	0.010	0.10	0.25	b	0.013	0.020	0.33	0.51
D	0.189	0.197	4.80	5.00	c	0.008	0.010	0.19	0.25
H	0.228	0.244	5.80	6.20	θ	0°	8°	0°	8°
E	0.150	0.157	3.80	4.00	-	-	-	-	-
L	0.016	0.050	0.40	1.27	-	-	-	-	-

Note: Controlling dimensions are in inches. Approximate dimensions are provided in millimeters

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