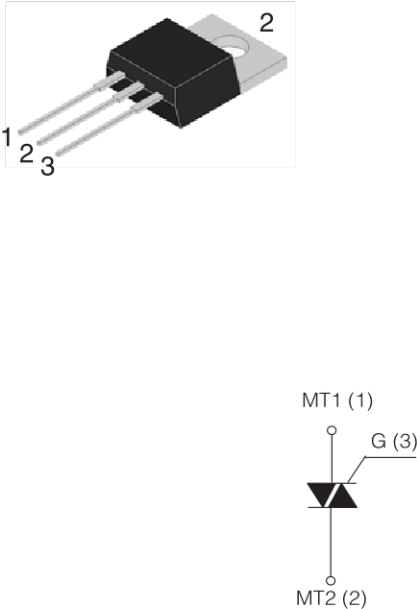



**LOGIC LEVEL TRIAC**

<b>TO-220AB</b>  	<b>On-State Current</b> 4 Amp	<b>Gate Trigger Current</b> ≤ 10 mA	
	<b>Off-State Voltage</b> 400 V ÷ 800 V		
	<b>FEATURES</b> <ul style="list-style-type: none"> <li>• Glass/passivated die junctions</li> <li>• Medium current Triac</li> <li>• Ideal for automated placement</li> <li>• Low thermal resistance</li> <li>• High surge current capability</li> <li>• Low forward voltage drop</li> <li>• Solder dip 260°C, 10s</li> <li>• Component in accordance to RoHS 2011/65/EU and WEEE 2002/96/EC</li> <li>• Meets MSL level 3, per J-STD-020, LF maximum peak of 260° C</li> </ul>		 <b>RoHS COMPLIANT</b>
	<b>MECHANICAL DATA</b> <ul style="list-style-type: none"> <li>• <b>Case:</b> TO-220AB. Epoxy meets UL 94V-0 flammability rating.</li> <li>• <b>Polarity:</b> As marked on the body.</li> <li>• <b>Terminals:</b> Matte tin plated leads, solderable per MIL-STD-750 Method 2026, J-STD-002 and JESD22-B102. Consumer grade, meets JESD 201 class 1A whisker test.</li> </ul>		
<b>TYPICAL APPLICATIONS</b> Logic level versions are designed to interface directly with low power drivers such as microcontrollers.			

**Maximun Ratings and Electrical Characteristics at 25°C**

SYMBOL	PARAMETER	CONDITIONS	Value	Unit
$I_{T(RMS)}$	RMS On-state Current (full sine wave)	All Conduction Angle, $T_c = 95^\circ C$	4	A
$I_{TSM}$	Non-repetitive On-State Current	Full Cycle, 60 Hz ( $t = 16.7$ ms)	33	A
$I_{TSM}$	Non-repetitive On-State Current	Full Cycle, 50 Hz ( $t = 20$ ms)	30	A
$I^2t$	Fusing Current	$t_p = 10$ ms, Half Cycle	4.5	A <sup>2</sup> s
$I_{GM}$	Peak Gate Current	20 $\mu$ s max. $T_j = 125^\circ C$	4	A
$P_{G(AV)}$	Average Gate Power Dissipation	$T_j = 125^\circ C$	1	W
$di/dt$	Critical rate of rise of on-state current	$I_G = 2 \times I_{GT}$ , $t_r \leq 100$ ns $f = 120$ Hz, $T_j = 125^\circ C$	50	A/ $\mu$ s
$T_j$	Operating Temperature		(-40 +125)	°C
$T_{stg}$	Storage Temperature		(-40 +150)	°C
$T_{sld}$	Soldering Temperature	10s max	260	°C

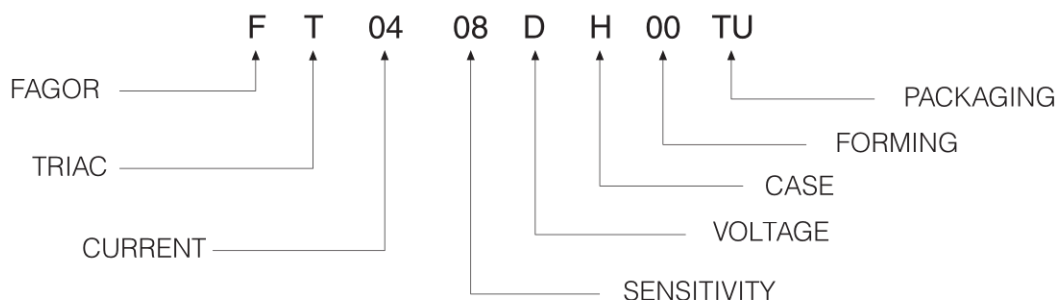
SYMBOL	PARAMETER	VOLTAGE			Unit
		D	M	N	
$V_{DRM}/V_{RRM}$	Repetitive Peak Off State Voltage	400	600	800	V

**LOGIC LEVEL TRIAC**
**Electrical Characteristics at Tamb = 25 °C**

SYMBOL	PARAMETER	CONDITIONS	Quadrant		SENSITIVITY					Unit
					04	05	07	08	09	
I <sub>GT</sub> <sup>(1)</sup>	Gate Trigger Current	V <sub>D</sub> = 12 V <sub>DC</sub> , R <sub>L</sub> = 33Ω, T <sub>j</sub> = 25 °C	Q1÷Q3	MAX	5	5	5	10	10	mA
			Q4	MAX		5	7		10	mA
V <sub>GT</sub>	Gate Trigger Voltage	V <sub>D</sub> = 12 V <sub>DC</sub> , R <sub>L</sub> = 33Ω, T <sub>j</sub> = 25 °C	Q1÷Q3	MAX	1.3					V
			Q1÷Q4	MAX	1.3					V
V <sub>GD</sub>	Gate Non Trigger Voltage	V <sub>D</sub> = V <sub>DRM</sub> , R <sub>L</sub> = 3.3 KΩ, T <sub>j</sub> = 125 °C	Q1÷Q3	MIN	0.2					V
			Q1÷Q4	MIN	0.2					V
I <sub>H</sub> <sup>(2)</sup>	Holding Current	I <sub>T</sub> = 100 mA, Gate open, T <sub>j</sub> = 25 °C		MAX	10	10	15	15	20	mA
I <sub>L</sub>	Latching Current	I <sub>G</sub> = 1.2 I <sub>GT</sub> , T <sub>j</sub> = 25 °C	Q1,Q3	MAX	10			25		mA
			Q1,Q3,Q4	MAX		10	20		20	mA
			Q2	MAX	20	20	30	30	25	mA
dV/dt <sup>(2)</sup>	Critical Rate of Voltage Rise	V <sub>D</sub> = 0.67 x V <sub>DRM</sub> , Gate open T <sub>j</sub> = 125 °C		MIN	20	20	20	40	40	V/μs
(dl/dt) <sub>c</sub> <sup>(2)</sup>	Critical Rate of Current Rise	(dv/dt) <sub>c</sub> = 0.1 V/μs T <sub>j</sub> = 125 °C		MIN	1.8	1.8	1.8	2.7	2.5	A/ms
		(dv/dt) <sub>c</sub> = 10 V/μs T <sub>j</sub> = 125 °C		MIN	0.9	0.9	0.9	2.0	1.5	A/ms
		without snubber T <sub>j</sub> = 125 °C		MIN	-	-	-	-	-	
V <sub>TM</sub> <sup>(2)</sup>	On-state Voltage	I <sub>T</sub> = 5.5 Amp, t <sub>p</sub> = 380 μs, T <sub>j</sub> = 25 °C		MAX	1.6					V
V <sub>t(o)</sub> <sup>(2)</sup>	Threshold Voltage	T <sub>j</sub> = 125 °C		MAX	0.9					V
r <sub>d</sub> <sup>(2)</sup>	Dynamic resistance	T <sub>j</sub> = 125 °C		MAX	120					mΩ
I <sub>DRM</sub> /I <sub>RRM</sub>	Off-State Leakage Current	V <sub>D</sub> = V <sub>DRM</sub> , T <sub>j</sub> = 125 °C		MAX	0.5					mA
		V <sub>R</sub> = V <sub>RRM</sub> , T <sub>j</sub> = 25 °C		MAX	5					μA
R <sub>th(j-c)</sub>	Thermal Resistance Junction-Case	for AC 360° conduction angle			2.0					°C/W
R <sub>th(j-a)</sub>	Thermal Resistance Junction-Ambient				60					°C/W

(1) Minimum I<sub>GT</sub> is guaranteed at 5% of I<sub>GT</sub> max.

(2) For either polarity of electrode MT2 voltage with reference to electrode MT1.

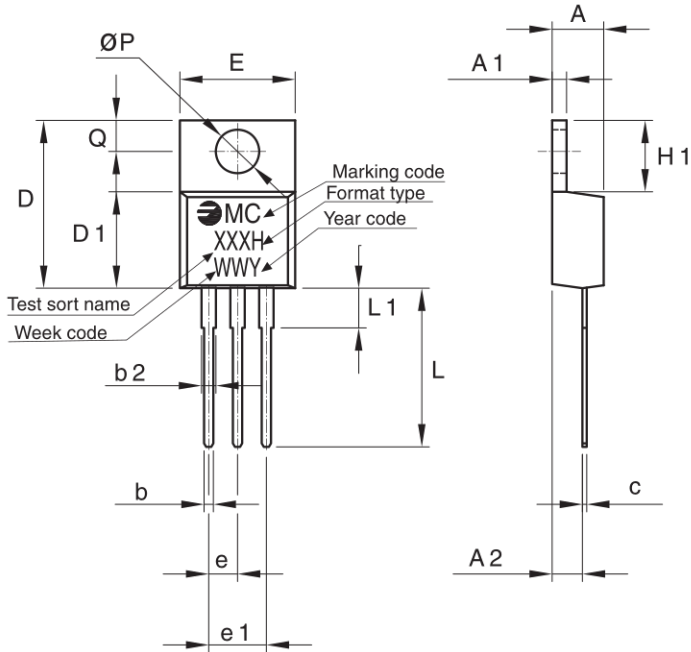
**Part Number Information**


**LOGIC LEVEL TRIAC**

**Ordering information**

PREFERRED P/N	PACKAGE CODE	DELIVERY MODE	BASE QUANTITY	UNIT WEIGHT (g)
FT0408MH 00TU	TU	TUBE	1,000	2.30

**Package Outline Dimensions: (mm) TO-220AB**



The technical drawing shows a TO-220AB package with various dimensions labeled:  $\varnothing P$ , E, Q, D, D1, L1, L, b2, b, e, e1, A, A1, A2, H1, and c. The marking code is shown as MC, XXXH, and WWY, with arrows pointing to 'Marking code', 'Format type', and 'Year code'. The test sort name and week code are also indicated.

REF.	DIMENSIONS	
	Milimeters	
	Min.	Max.
A	4.47	4.67
A1	1.17	1.37
A2	2.52	2.82
b	0.71	0.91
b2	1.17	1.37
c	0.31	0.53
D	14.65	15.35
D1	8.50	8.90
E	10.01	10.36
e	2.51	2.57
e1	4.98	5.18
H1	6.15	6.45
L	13.40	13.96
L1	3.56	3.96
P	3.735	3.935
Q	2.59	2.89

<b>Mounting Torque</b>	<b>0.8 N.m</b>
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**LOGIC LEVEL TRIAC**

**Ratings and Characteristics (Ta 25 °C unless otherwise noted)**

Fig. 1: Maximum power dissipation versus RMS on-state current (full cycle).

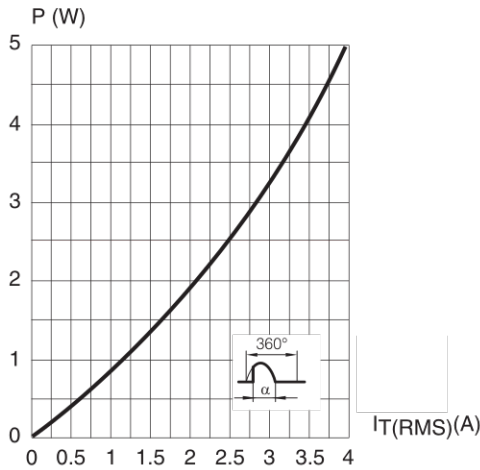


Fig. 2: RMS on-state current versus case temperature (full cycle).

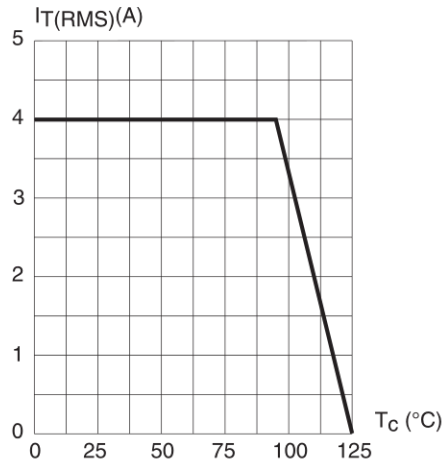


Fig. 3: Relative variation of thermal impedance versus pulse duration.

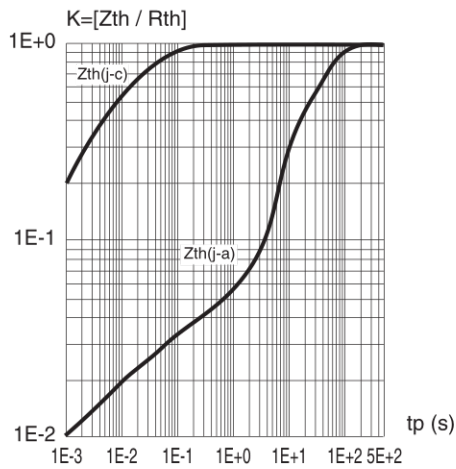


Fig. 4: On-state characteristics (maximum values)

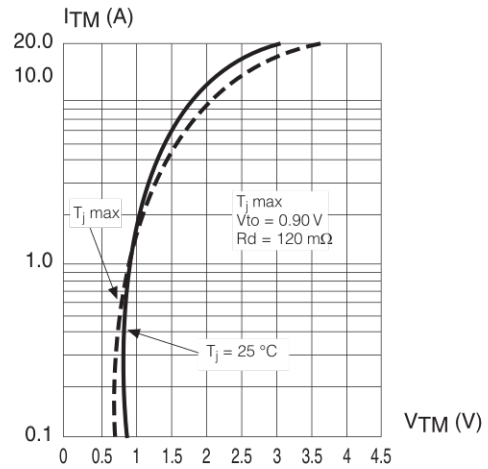


Fig. 5: Surge peak on-state current versus number of cycles

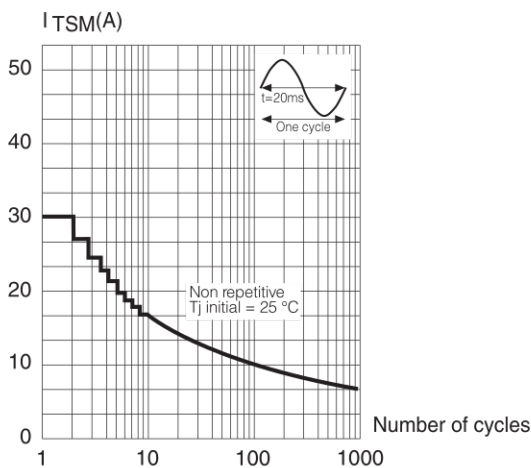
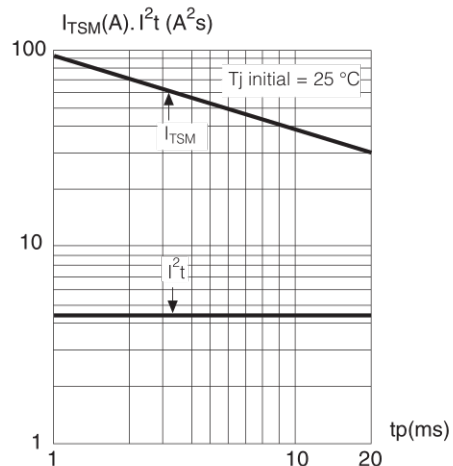


Fig. 6: Non repetitive surge peak on-state current for a sinusoidal pulse with width: tp < 10 ms, and corresponding value of I²t.



**LOGIC LEVEL TRIAC**

**Ratings and Characteristics (Ta 25 °C unless otherwise noted)**

Fig. 7: Relative variation of gate trigger current, holding current and latching versus junction temperature (typical values)

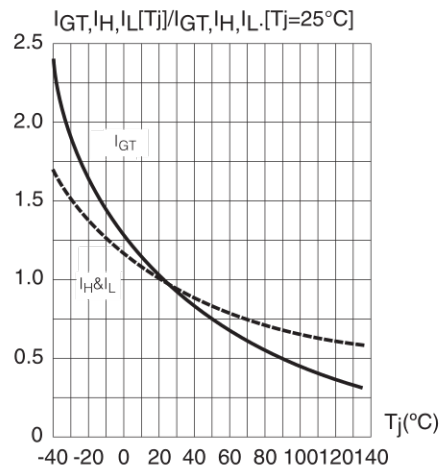


Fig. 8: Relative variation of critical rate of decrease of main current versus junction temperature

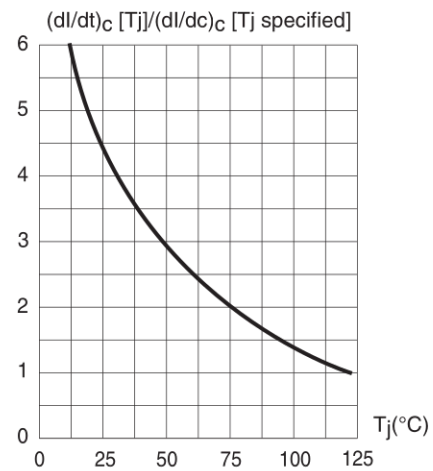
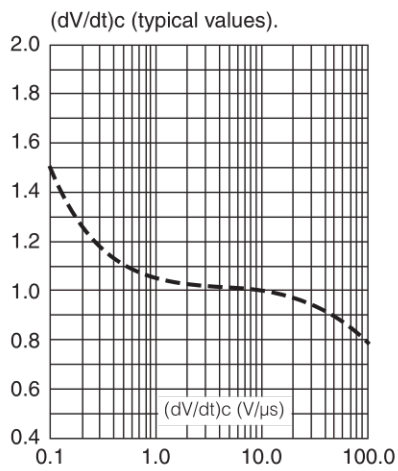


Fig. 9: Relative variation of critical rate of decrease of main current versus



**LOGIC LEVEL TRIAC****Revision History**

Date	Revision	Description of Changes
14-Jun-2011	0	Original Data Sheet
10-Mar-2015	1	200V and 700V eliminated

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