FAIRCHILD SEMICONDUCTOR®

July 2012

UniFET™

FDP18N50 / FDPF18N50 / FDPF18N50T

500V N-Channel MOSFET

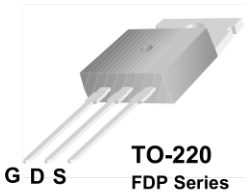
Features

- 18A, 500V, $R_{DS(on)}$ = 0.265Ω @V_{GS} = 10 V
- Low gate charge (typical 45 nC)
- Low C_{rss} (typical 25 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

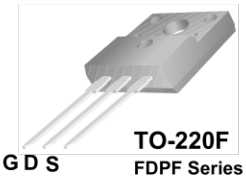
Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

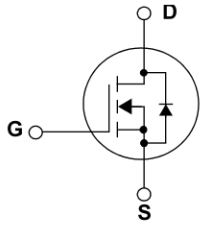
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies and active power factor correction.



TO-220
FDP Series



TO-220F
FDPF Series



Absolute Maximum Ratings

Symbol	Parameter		FDP18N50	FDPF18N50 / FDPF18N50T	Unit
V_{DSS}	Drain-Source Voltage		500		V
I_D	Drain Current	- Continuous (T_C = 25°C) - Continuous (T_C = 100°C)	18 10.8	18 * 10.8 *	A A
I_{DM}	Drain Current	- Pulsed (Note 1)	72	72 *	A
V_{GSS}	Gate-Source voltage		±30		V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	945		mJ
I_{AR}	Avalanche Current	(Note 1)	18		A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	23.5		mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5		V/ns
P_D	Power Dissipation	(T_C = 25°C) - Derate above 25°C	235 1.88	38.5 0.3	W W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150		°C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds		300		°C

* Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	FDP18N50	FDPF18N50 / FDPF18N50T	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.53	3.3	°C/W
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink Typ.	0.5	--	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	62.5	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDP18N50	FDP18N50	TO-220	-	-	50
FDPF18N50	FDPF18N50	TO-220F	-	-	50
FDPF18N50T	FDPF18N50T	TO-220F	-	-	50

Electrical Characteristics

T_C = 25°C unless otherwise noted

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	500	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250μA, Referenced to 25°C	--	0.5	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500V, V_{GS} = 0V V_{DS} = 400V, T_C = 125°C	-- --	-- --	1 10	μA μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30V, V_{DS} = 0V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30V, V_{DS} = 0V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10V, I_D = 9A	--	0.220	0.265	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40V, I_D = 9A (Note 4)	--	25	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz	--	2200	2860	pF
C_{oss}	Output Capacitance		--	330	430	pF
C_{rss}	Reverse Transfer Capacitance		--	25	40	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 250V, I_D = 18A, R_G = 25Ω	--	55	120	ns
t_r	Turn-On Rise Time		--	165	340	ns
$t_{d(off)}$	Turn-Off Delay Time		--	95	200	ns
t_f	Turn-Off Fall Time	(Note 4, 5)	--	90	190	ns
Q_g	Total Gate Charge	V_{DS} = 400V, I_D = 18A, V_{GS} = 10V	--	45	60	nC
Q_{gs}	Gate-Source Charge		--	12.5	--	nC
Q_{gd}	Gate-Drain Charge	(Note 4, 5)	--	19	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	18	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	72	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0V, I_S = 18A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, I_S = 18A, dI_F/dt =100A/μs (Note 4)	--	500	--	ns
Q_{rr}	Reverse Recovery Charge		--	5.4	--	μC

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L = 5.2mH, I_{AS} = 18A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
3. I_{SD} ≤ 18A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
5. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

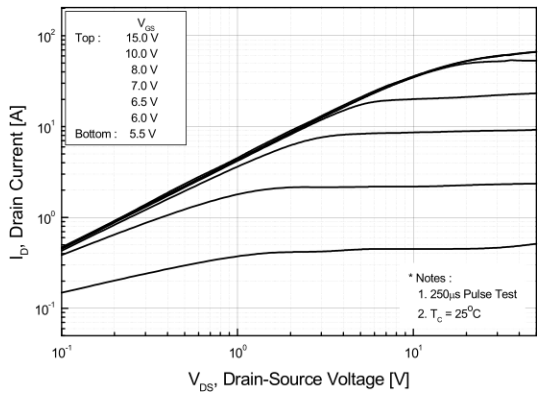


Figure 2. Transfer Characteristics

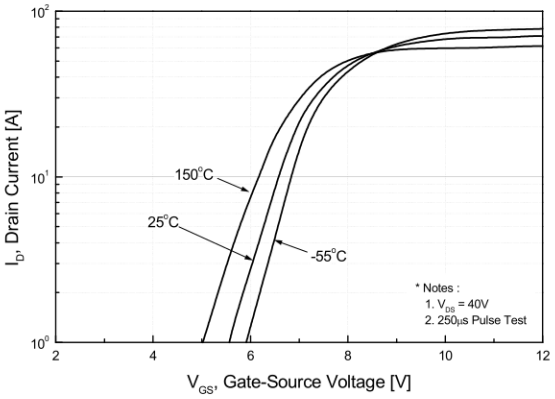


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

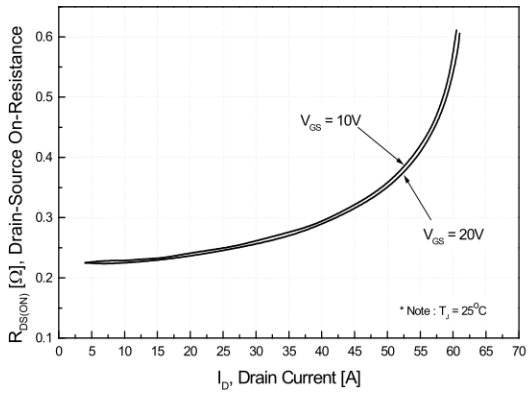


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperatue

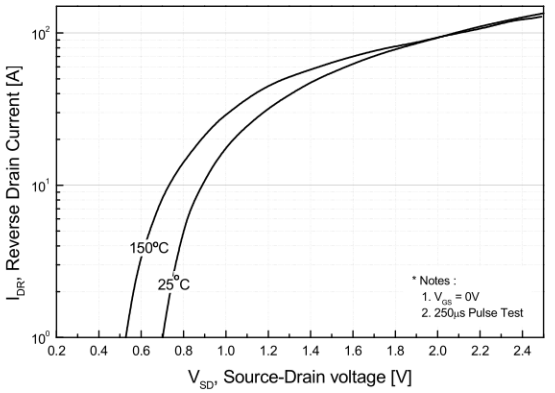


Figure 5. Capacitance Characteristics

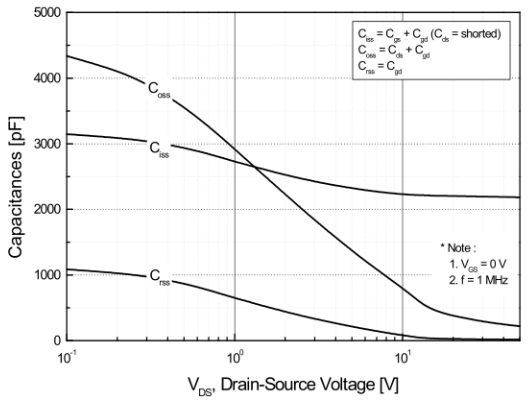
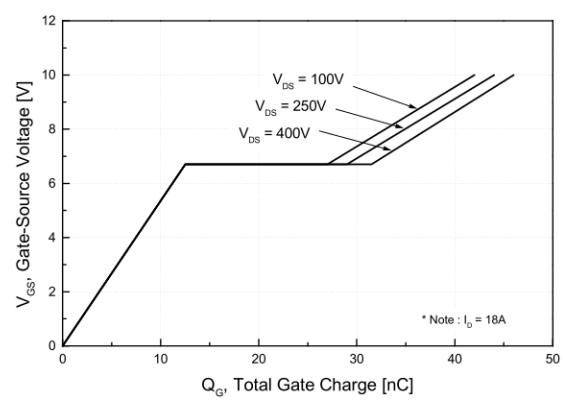


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

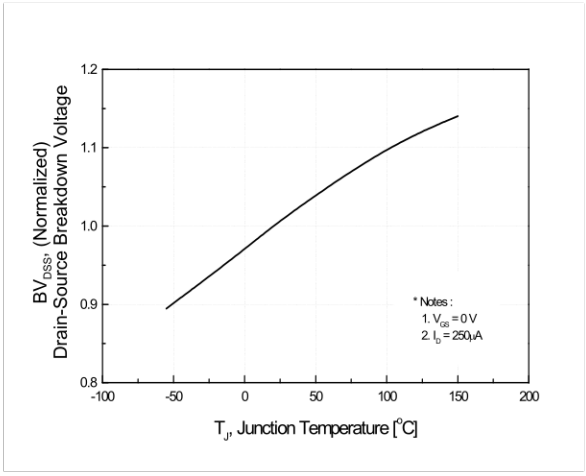


Figure 8. On-Resistance Variation vs. Temperature

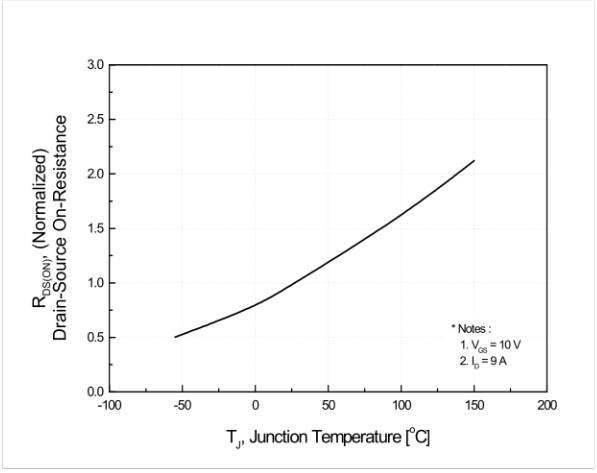


Figure 9-1. Maximum Safe Operating Area - FDP18N50

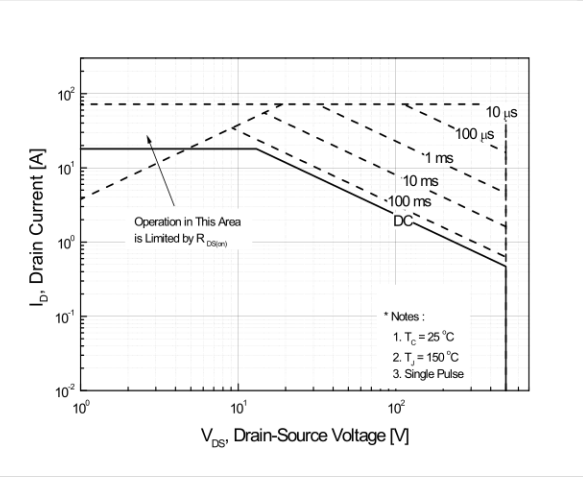


Figure 9-2. Maximum Safe Operating Area -FDPF18N50 / FDPF18N50T

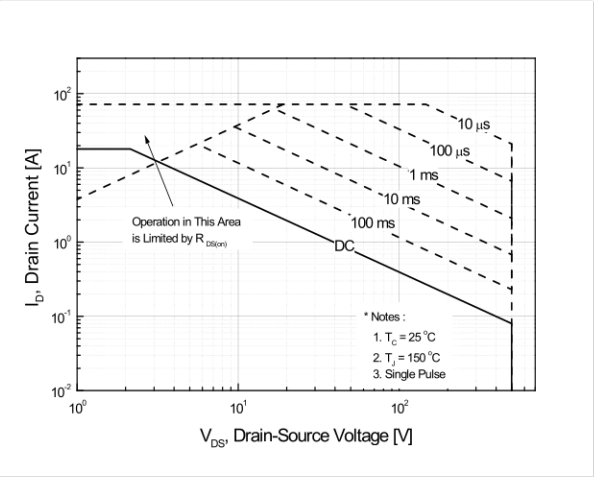
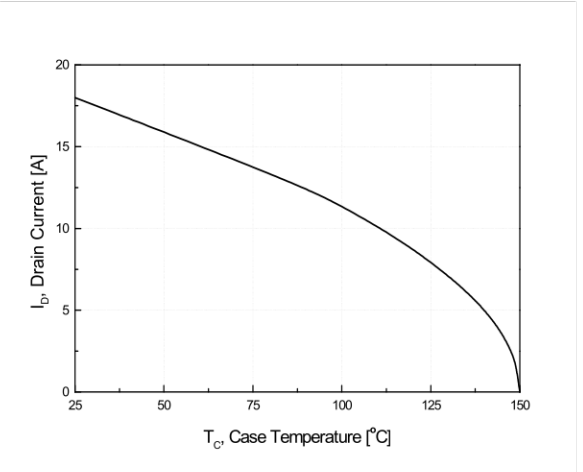


Figure 10. Maximum Drain Currentvs. Case Temperature



Typical Performance Characteristics (Continued)

Figure 11-1. Transient Thermal Response Curve - FDP18N50

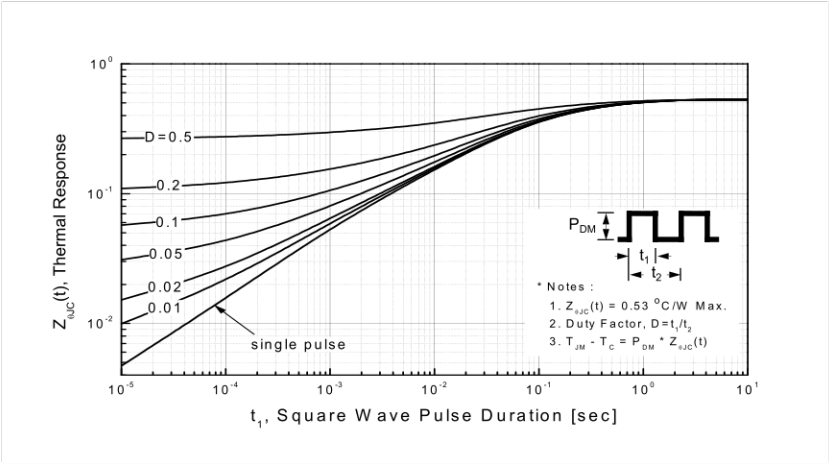
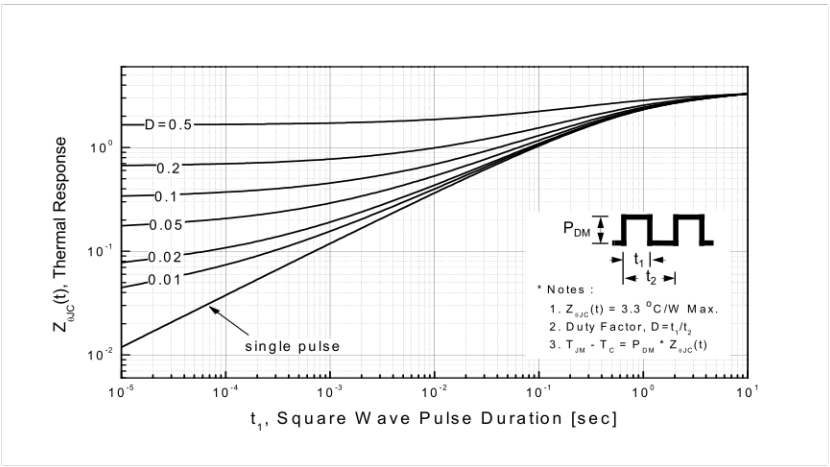
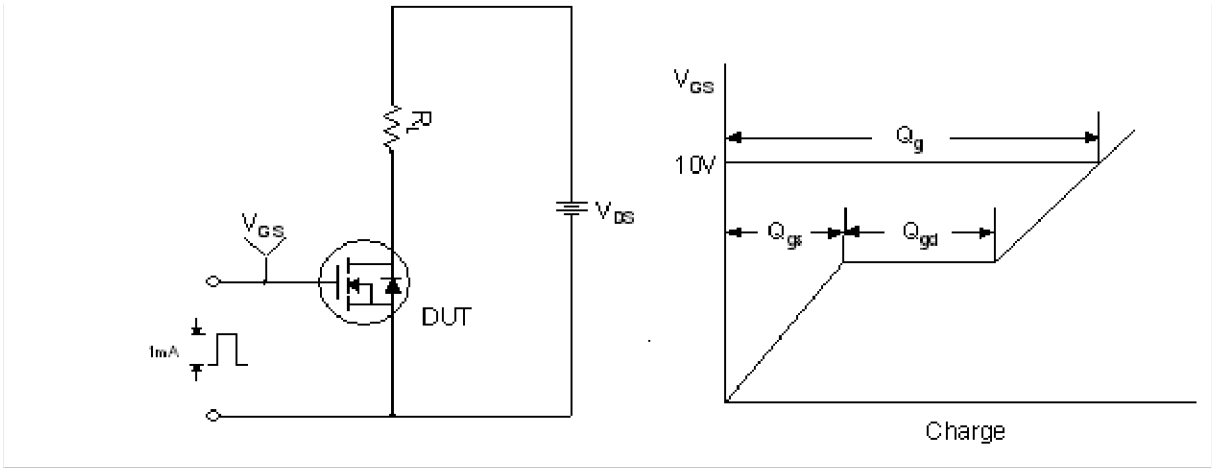


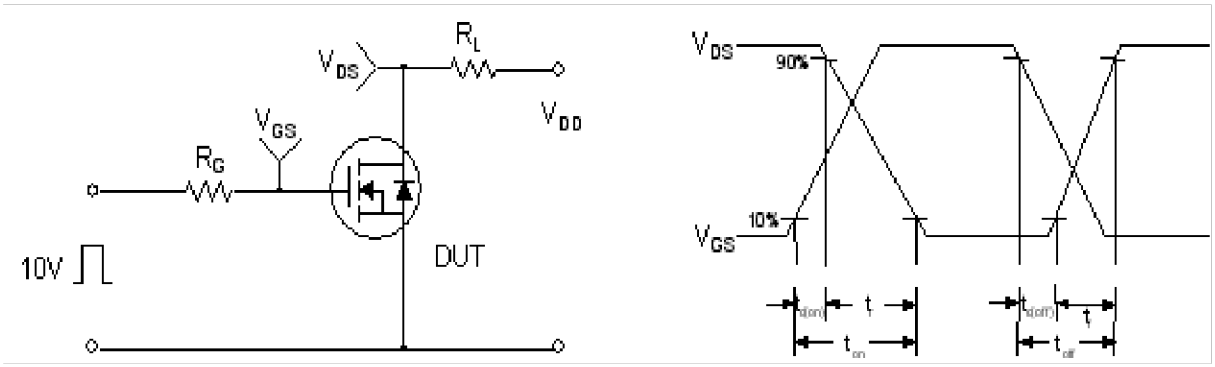
Figure 11-2. Transient Thermal Response Curve - FDPF18N50 / FDPF18N50T



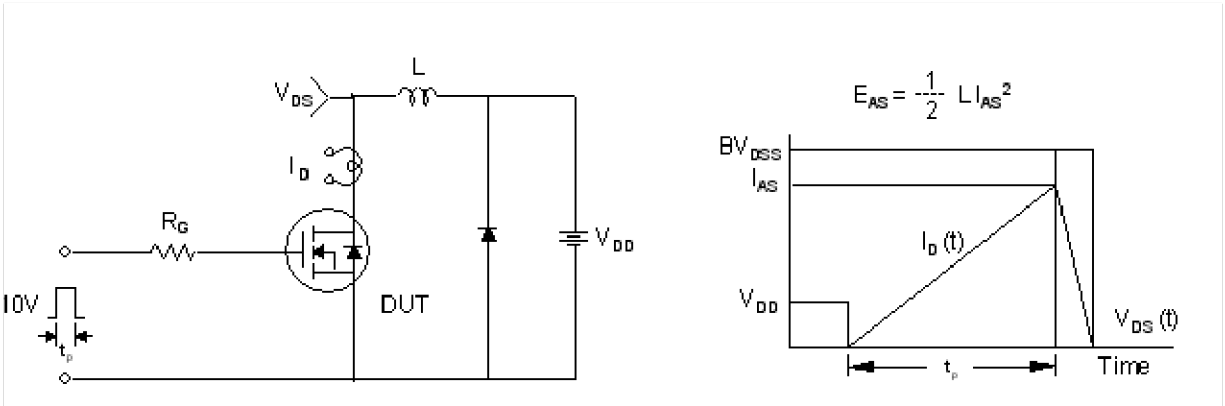
Gate Charge Test Circuit & Waveform



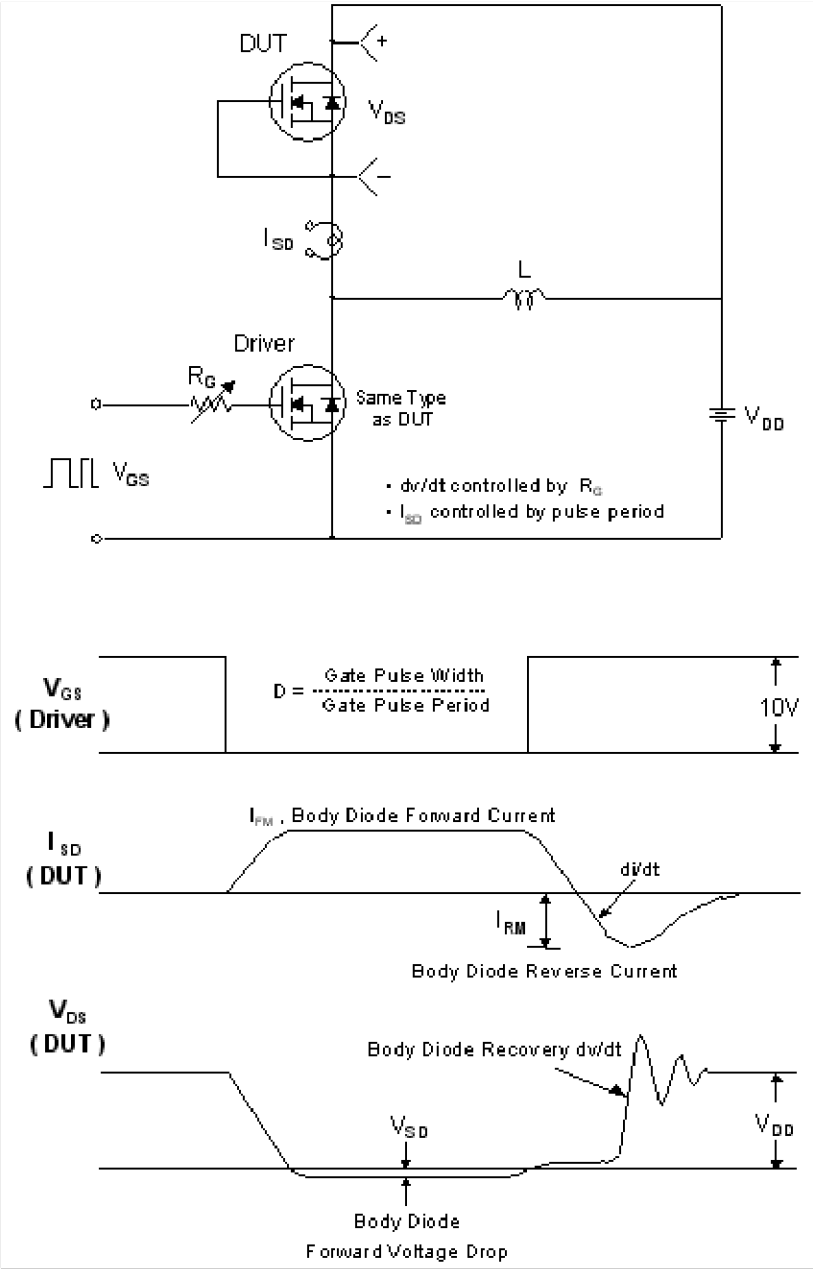
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

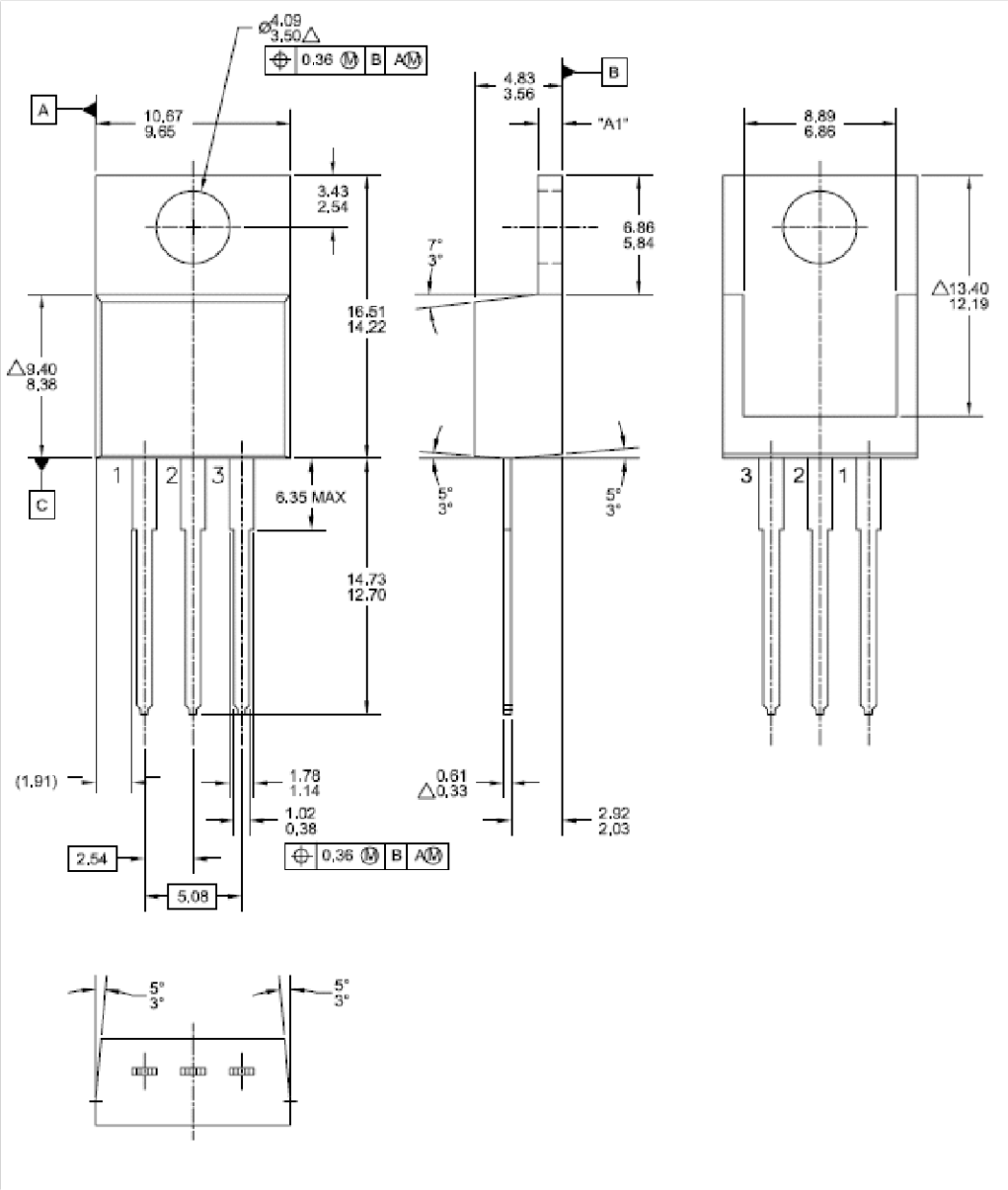


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

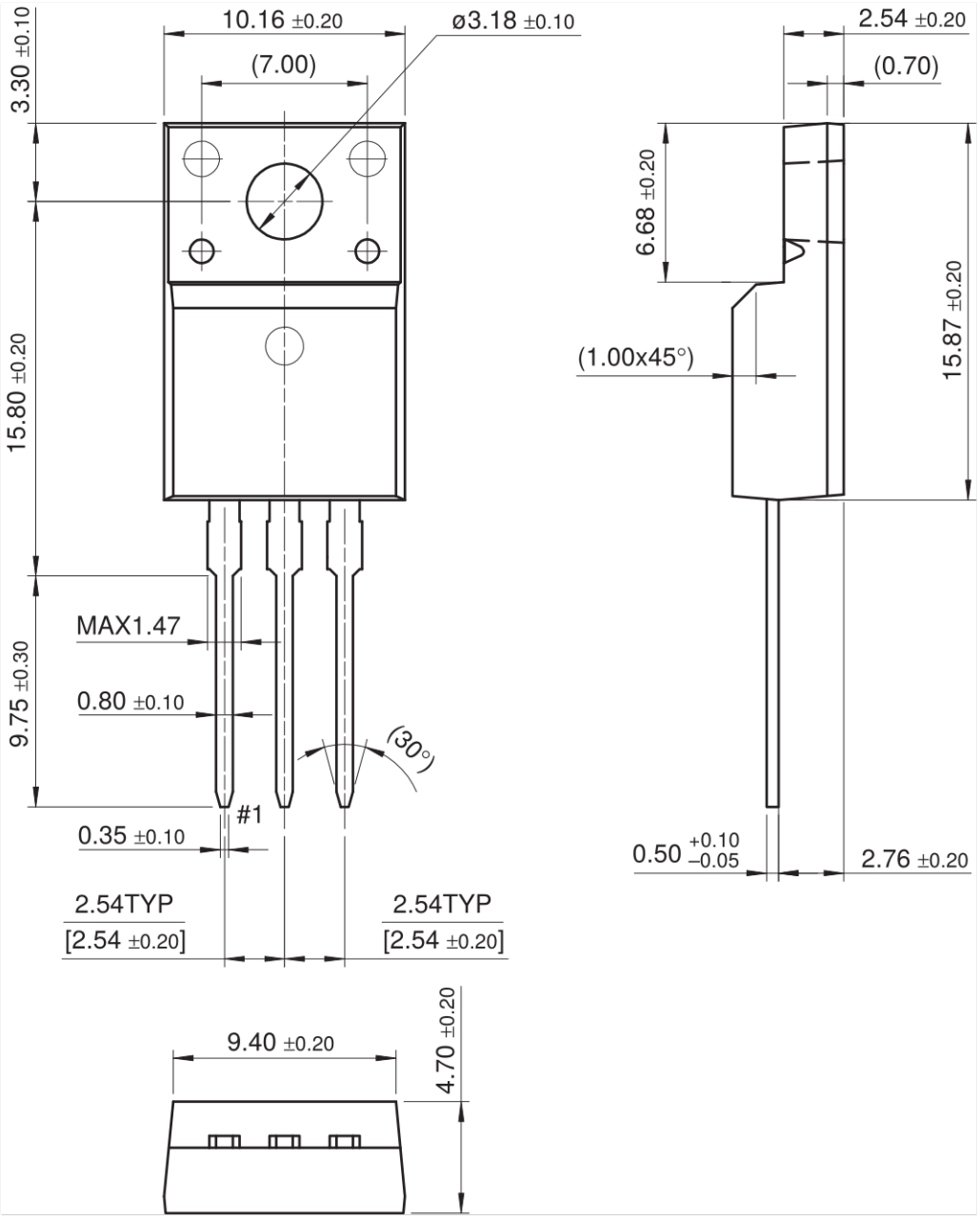
TO-220



Dimensions in Millimeters

Mechanical Dimensions

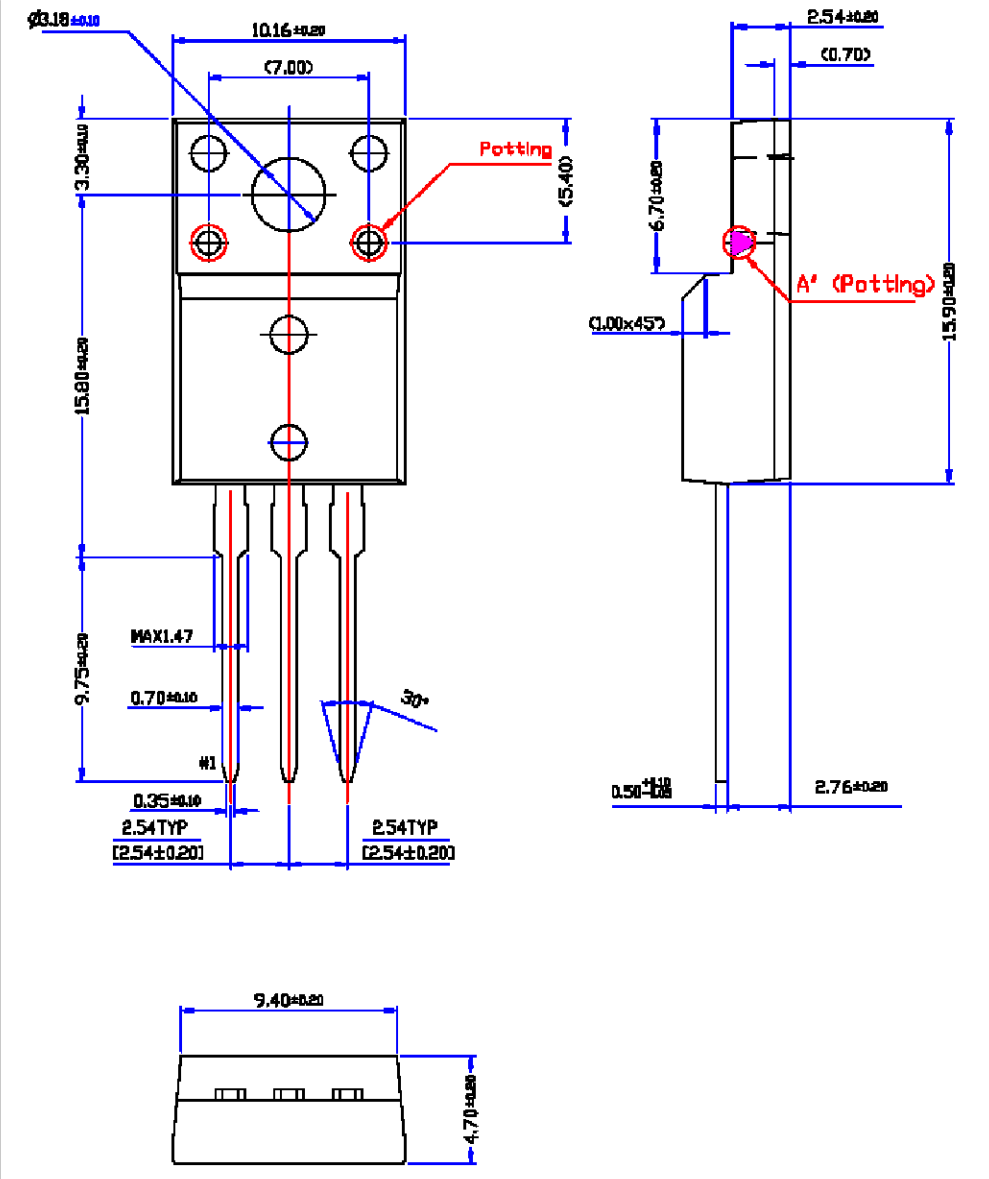
TO-220F



Dimensions in Millimeters

Package Dimensions

TO-220F Potted



* Front/Back Side Isolation Voltage : AC 2500V

Dimensions in Millimeters

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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