

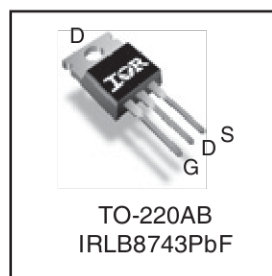
IRLB8743PbF

HEXFET® Power MOSFET

Applications

- Optimized for UPS/Inverter Applications
- High Frequency Synchronous Buck Converters for Computer Processor Power
- High Frequency Isolated DC-DC Converters with Synchronous Rectification for Telecom and Industrial use

V_{DS}	$R_{DS(on)}$ max	Qg
30V	3.2m Ω	36nC



Benefits

- Very Low RDS(on) at 4.5V V_{GS}
- Ultra-Low Gate Impedance
- Fully Characterized Avalanche Voltage and Current
- Lead-Free

G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	± 20	
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	150④	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	110	
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V (Package Limited)	78	
I_{DM}	Pulsed Drain Current ①	620	W
P_D @ $T_C = 25^\circ\text{C}$	Maximum Power Dissipation ⑥	140	
P_D @ $T_C = 100^\circ\text{C}$	Maximum Power Dissipation ⑥	68	$W/^\circ\text{C}$
	Linear Derating Factor	0.90	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	$^\circ\text{C}$
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw ⑦	10lbf·in (1.1N·m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑧	—	1.11	$^\circ\text{C/W}$
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface	0.5	—	
$R_{\theta JA}$	Junction-to-Ambient ⑨	—	62	

Notes ①through ⑨ are on page 9
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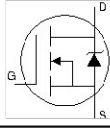
Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	17	—	mV/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	2.5	3.2	m Ω	$V_{GS} = 10V, I_D = 40A$ ③
		—	3.5	4.2		$V_{GS} = 4.5V, I_D = 32A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	1.35	1.8	2.35	V	$V_{DS} = V_{GS}, I_D = 100\mu A$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-7.7	—	mV/ $^\circ\text{C}$	
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 24V, V_{GS} = 0V$
		—	—	100		$V_{DS} = 24V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
g_{fs}	Forward Transconductance	190	—	—	S	$V_{DS} = 15V, I_D = 32A$
Q_g	Total Gate Charge	—	36	54	nC	$V_{DS} = 15V$ $V_{GS} = 4.5V$ $I_D = 32A$
Q_{gs1}	Pre-Vth Gate-to-Source Charge	—	9.1	—		
Q_{gs2}	Post-Vth Gate-to-Source Charge	—	4.2	—		
Q_{gd}	Gate-to-Drain Charge	—	13	—		
Q_{godr}	Gate Charge Overdrive	—	13	—		
Q_{sw}	Switch Charge ($Q_{gs2} + Q_{gd}$)	—	17.2	—		
Q_{oss}	Output Charge	—	21	—	nC	$V_{DS} = 16V, V_{GS} = 0V$
R_G	Gate Resistance	—	0.85	1.5	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	23	—	ns	$V_{DD} = 15V, V_{GS} = 4.5V$ ③ $I_D = 32A$ $R_G = 1.8\Omega$
t_r	Rise Time	—	92	—		
$t_{d(off)}$	Turn-Off Delay Time	—	25	—		
t_f	Fall Time	—	36	—		
C_{iss}	Input Capacitance	—	5110	—	pF	$V_{GS} = 0V$ $V_{DS} = 15V$ $f = 1.0MHz$
C_{oss}	Output Capacitance	—	960	—		
C_{rss}	Reverse Transfer Capacitance	—	440	—		

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	310	mJ
I_{AR}	Avalanche Current ①	—	32	A
E_{AR}	Repetitive Avalanche Energy ①	—	14	mJ

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	150 ④	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	620		
V_{SD}	Diode Forward Voltage	—	—	1.0	V	$T_J = 25^\circ\text{C}, I_S = 32A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	29	44	ns	$T_J = 25^\circ\text{C}, I_F = 32A, V_{DD} = 15V$
Q_{rr}	Reverse Recovery Charge	—	49	74	nC	$di/dt = 200A/\mu s$ ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

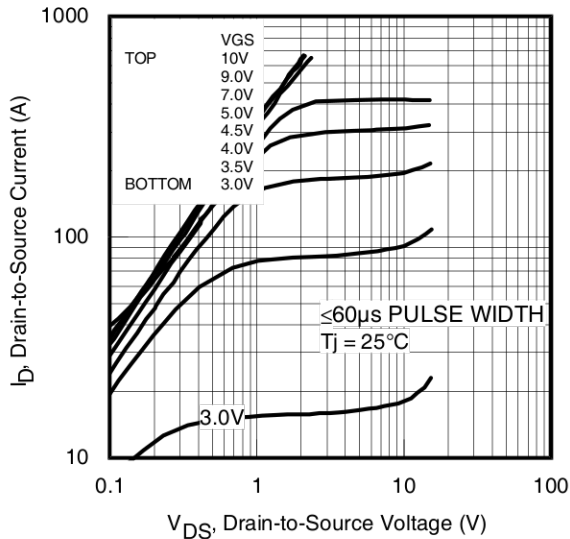


Fig 1. Typical Output Characteristics

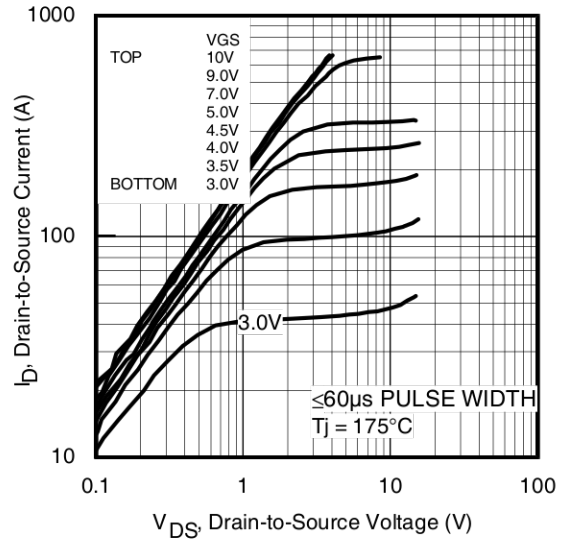


Fig 2. Typical Output Characteristics

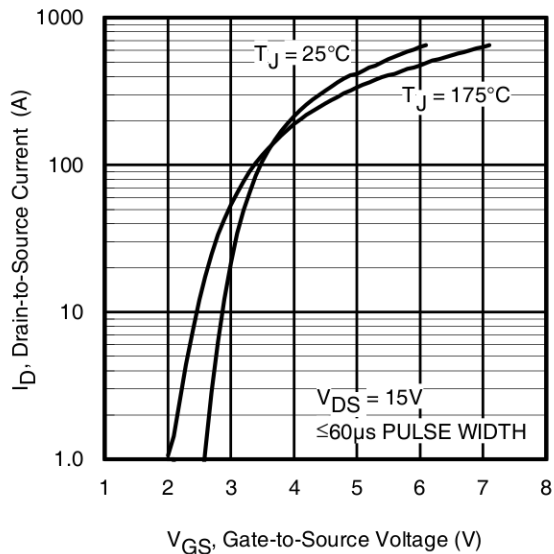


Fig 3. Typical Transfer Characteristics

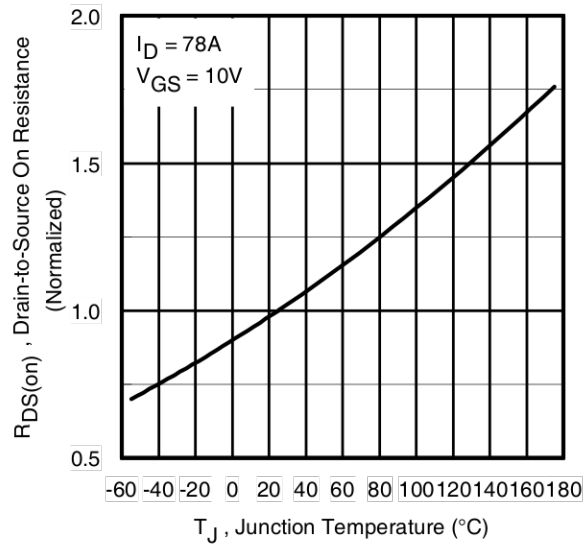
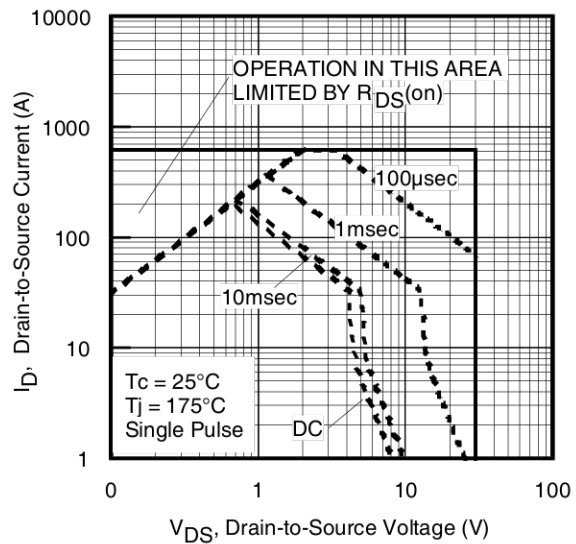
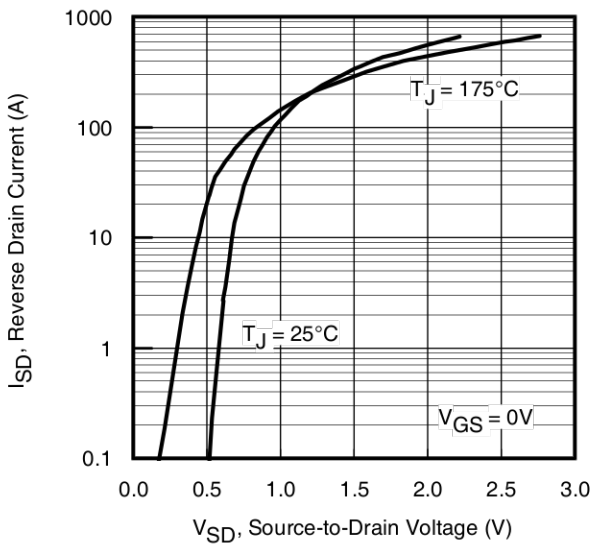
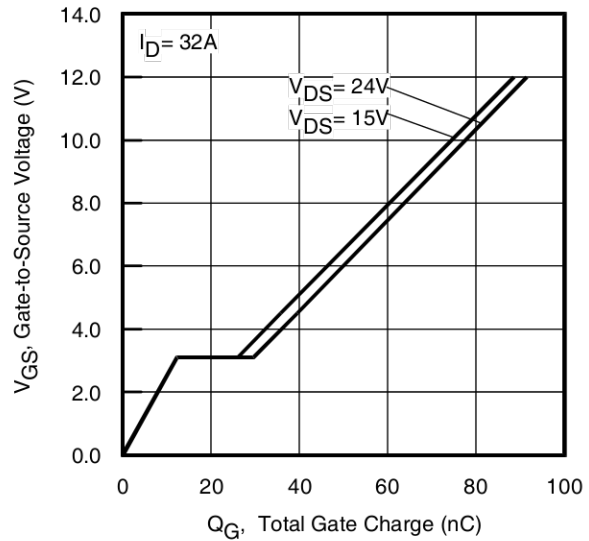
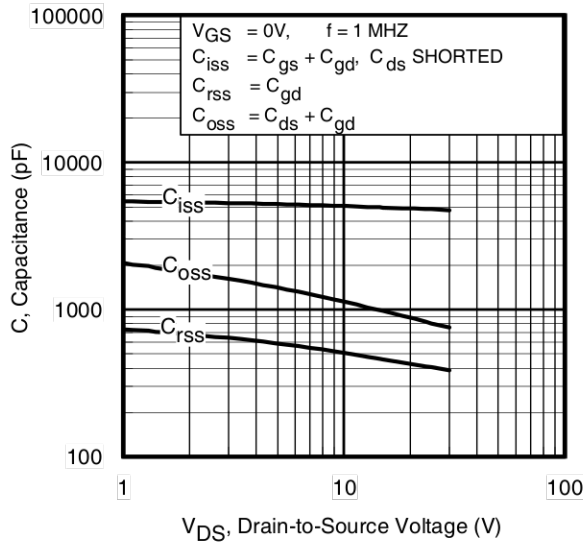
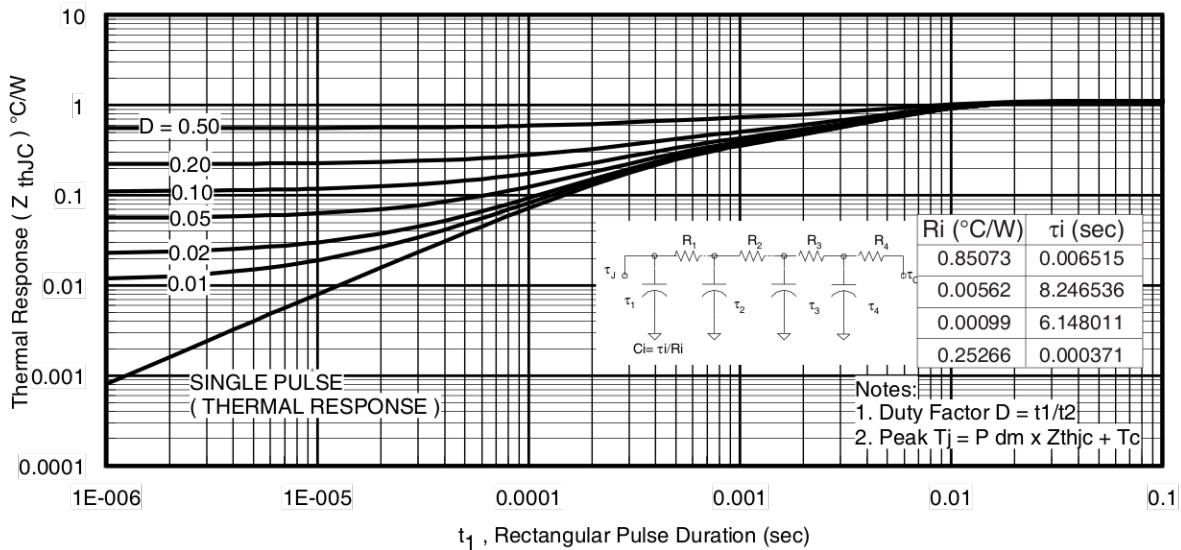
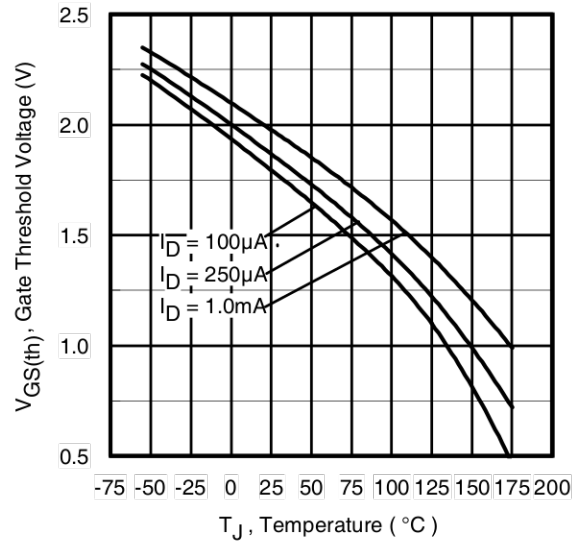
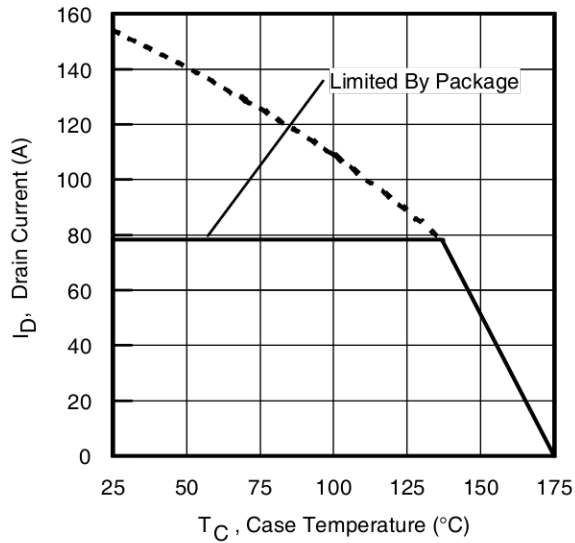


Fig 4. Normalized On-Resistance vs. Temperature

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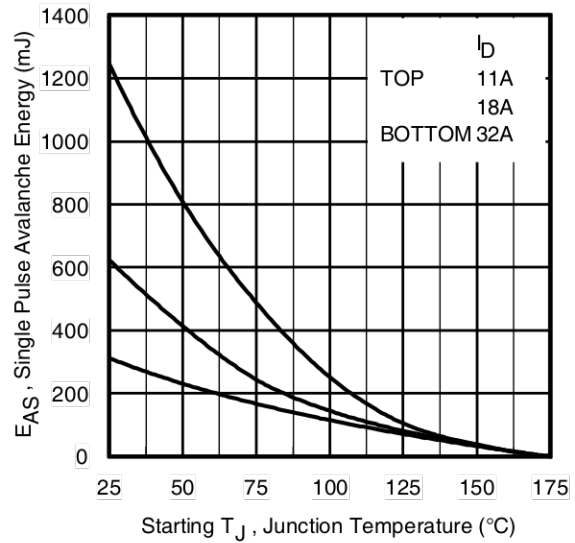
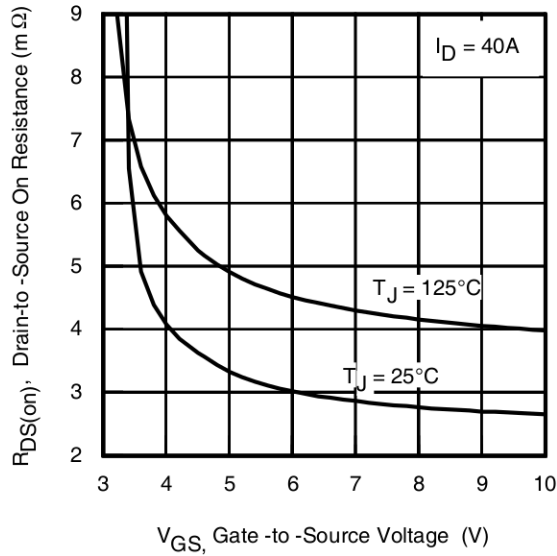


Fig 12. On-Resistance vs. Gate Voltage

Fig 13c. Maximum Avalanche Energy vs. Drain Current

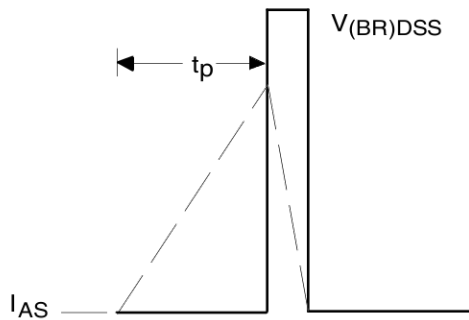
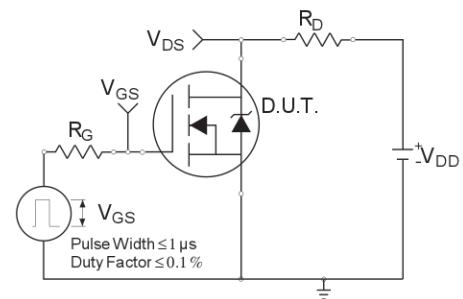
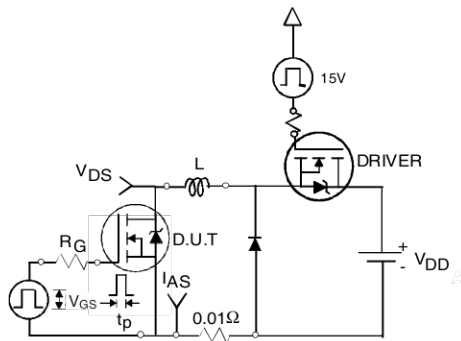
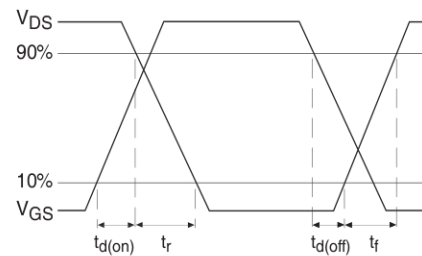


Fig 14a. Switching Time Test Circuit



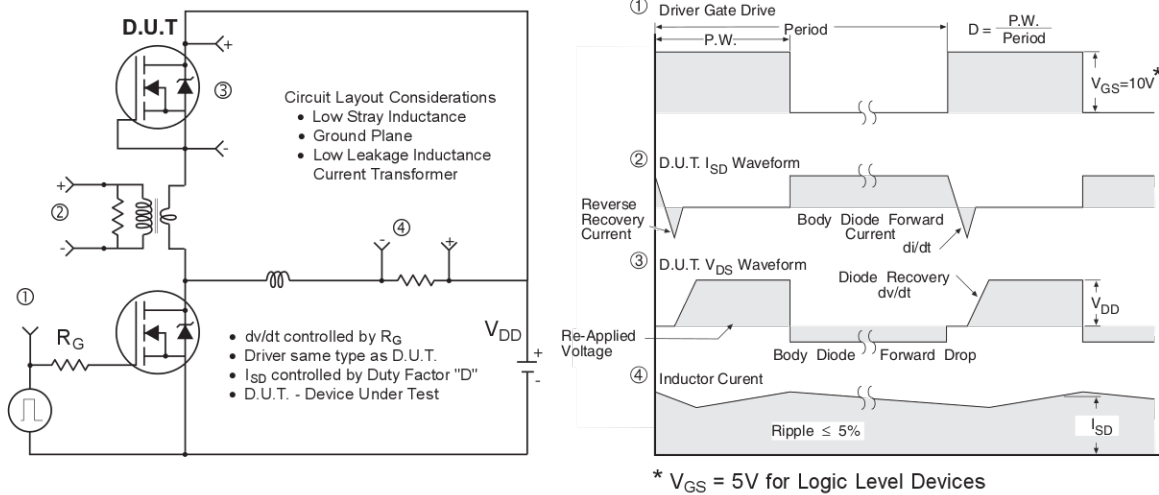


Fig 15. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

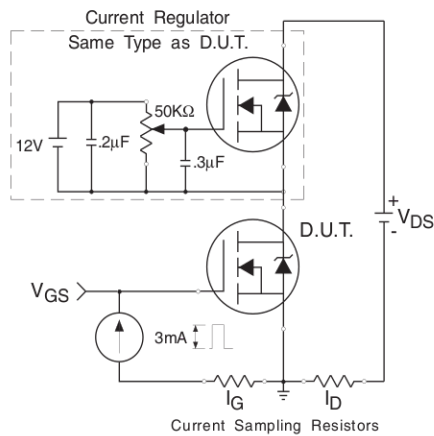


Fig 16. Gate Charge Test Circuit

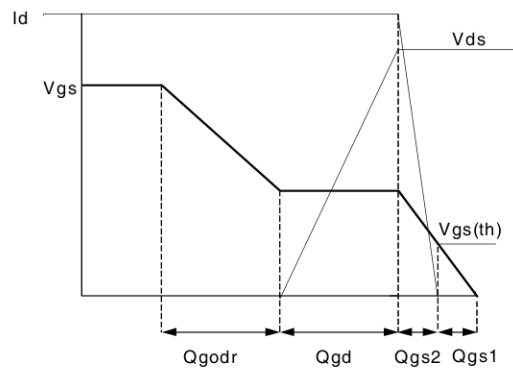
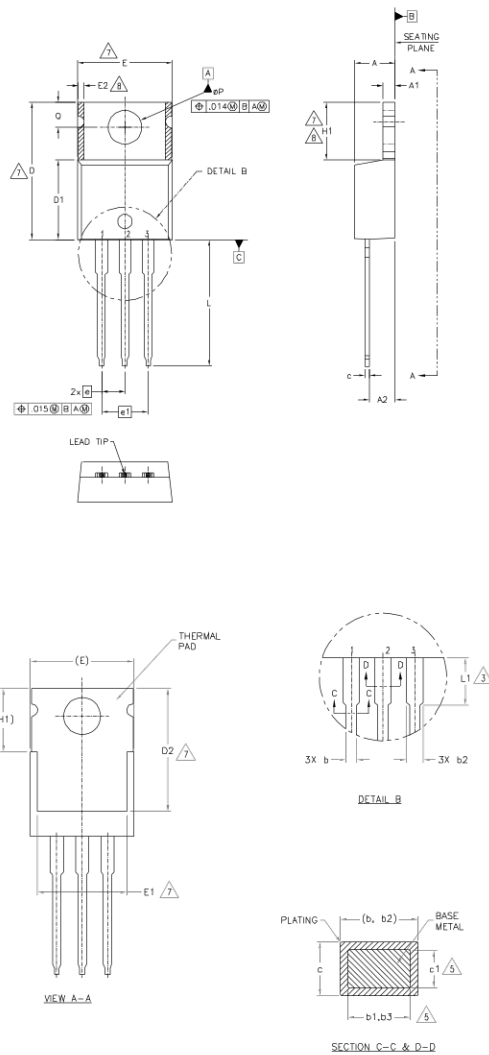


Fig 17. Gate Charge Waveform

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TO-220AB Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

- 1.- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
- 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS]
- 3.- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- 4.- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 5.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
- 6.- CONTROLLING DIMENSION : INCHES.
- 7.- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
- 8.- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
- 9.- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	0.51	1.40	.020	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.97	.015	.038	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	11.68	12.88	.460	.507	7
E	9.65	10.67	.380	.420	4,7
E1	6.86	8.89	.270	.350	7
E2	—	0.76	—	.030	8
e	2.54 BSC		.100 BSC		
e1	5.08 BSC		.200 BSC		
H1	5.84	6.86	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	3.56	4.06	.140	.160	3
øP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

LEAD ASSIGNMENTS

HEMIFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE

IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER

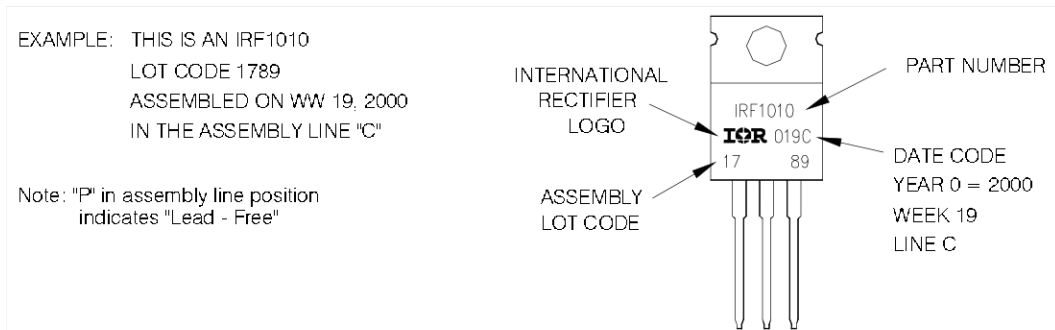
DIODES

- 1.- ANODE
- 2.- CATHODE
- 3.- ANODE

TO-220AB packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

TO-220AB Part Marking Information



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.61\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 32\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 78A.
- ⑤ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑥ R_θ is measured at T_J approximately 90°C .
- ⑦ This is only applied to TO-220AB package.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

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