Data Sheet No. PD60028-M

International IOR Rectifier

# IR2111(S) & (PbF)

## HALF-BRIDGE DRIVER

## Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- CMOS Schmitt-triggered inputs with pull-down
- Matched propagation delay for both channels
- Internally set deadtime
- High side output in phase with input
- Also available LEAD-FREE

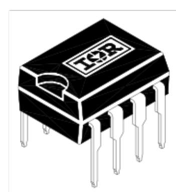
## Product Summary

| | |
|---|---|
| $V_{OFFSET}$ | 600V max. |
| $I_O$+/- | 200 mA / 420 mA |
| $V_{OUT}$ | 10 - 20V |
| $t_{on/off}$ (typ.) | 750 & 150 ns |
| Deadtime (typ.) | 650 ns |

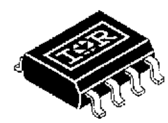
## Description

The IR2111(S) is a high voltage, high speed power MOSFET and IGBT driver with dependent high and low side referenced output channels designed for half-bridge applications. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic input is compatible with standard CMOS outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Internal deadtime is provided to avoid shoot-through in the output half-bridge. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

## Packages

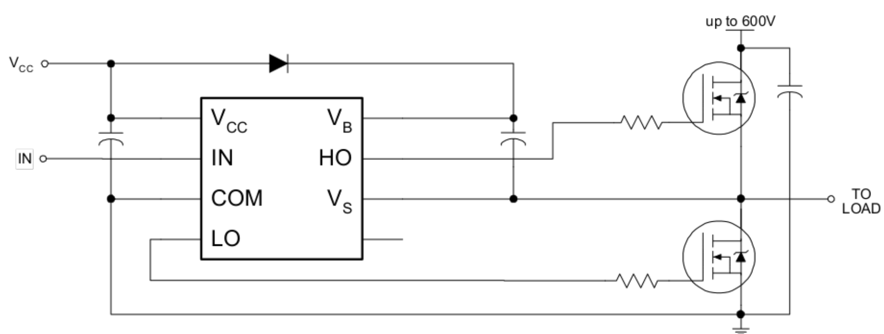


8-Lead PDIP



8-Lead SOIC

## Typical Connection




(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in figures 7 through 10.

| Symbol | Definition | | Min. | Max. | Units |
|---|---|---|---|---|---|
| $V_B$ | High side floating supply voltage | | -0.3 | 625 | V |
| $V_S$ | High side floating supply offset voltage | | $V_B$ - 25 | $V_B$ + 0.3 | |
| $V_{HO}$ | High side floating output voltage | | $V_S$ - 0.3 | $V_B$ + 0.3 | |
| $V_{CC}$ | Low side and logic fixed supply voltage | | -0.3 | 25 | |
| $V_{LO}$ | Low side output voltage | | -0.3 | $V_{CC}$ + 0.3 | |
| $V_{IN}$ | Logic input voltage | | -0.3 | $V_{CC}$ + 0.3 | |
| $dV_s/dt$ | Allowable offset supply voltage transient (figure 2) | | — | 50 | V/ns |
| $P_D$ | Package power dissipation @ $T_A \leq +25°C$ | (8 Lead PDIP) | — | 1.0 | W |
| | | (8 lead SOIC) | — | 0.625 | |
| $Rth_{JA}$ | Thermal resistance, junction to ambient | (8 lead PDIP) | — | 125 | °C/W |
| | | (8 lead SOIC) | — | 200 | |
| $T_J$ | Junction temperature | | — | 150 | °C |
| $T_S$ | Storage temperature | | -55 | 150 | |
| $T_L$ | Lead temperature (soldering, 10 seconds) | | — | 300 | |

## Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The $V_S$ offset rating is tested with all supplies biased at 15V differential.

| Symbol | Definition | Min. | Max. | Units |
|---|---|---|---|---|
| $V_B$ | High side floating supply absolute voltage | $V_S$ + 10 | $V_S$ + 20 | V |
| $V_S$ | High side floating supply offset voltage | Note 1 | 600 | |
| $V_{HO}$ | High side floating output voltage | $V_S$ | $V_B$ | |
| $V_{CC}$ | Low side and logic fixed supply voltage | 10 | 20 | |
| $V_{LO}$ | Low side output voltage | 0 | $V_{CC}$ | |
| $V_{IN}$ | Logic input voltage | 0 | $V_{CC}$ | |
| $T_A$ | Ambient temperature | -40 | 125 | °C |

Note 1: Logic operational for $V_S$ of -5 to +600V. Logic state held for $V_S$ of -5V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

## Dynamic Electrical Characteristics

$V_{BIAS}$ ($V_{CC}$, $V_{BS}$) = 15V, $C_L$ = 1000 pF and $T_A$ = 25°C unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in figure 3.

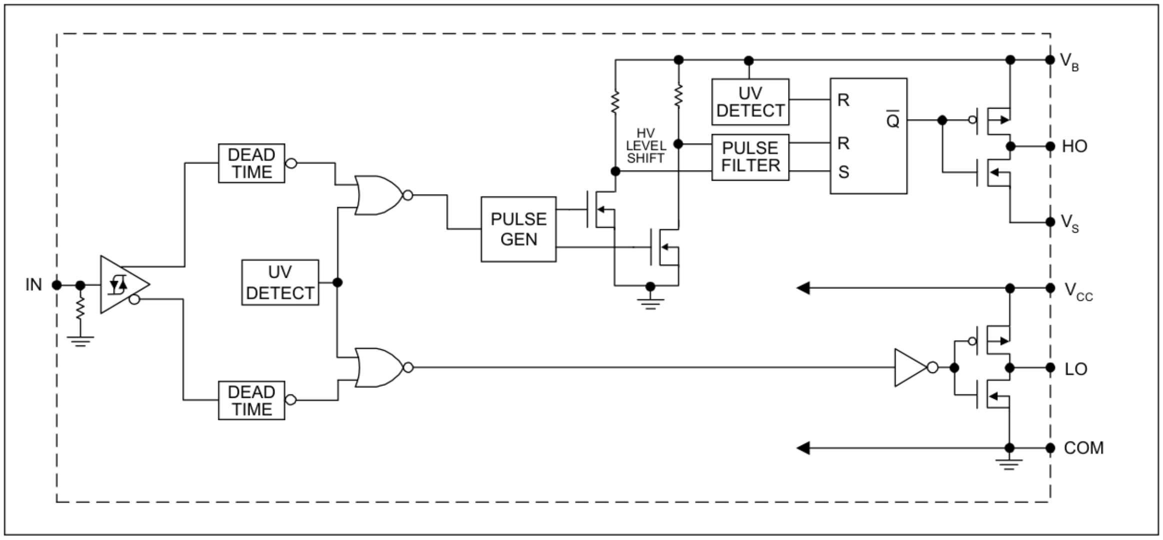
| Symbol | Definition | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $t_{on}$ | Turn-on propagation delay | 550 | 750 | 950 | ns | $V_S$ = 0V |
| $t_{off}$ | Turn-off propagation delay | — | 150 | 180 | | $V_S$ = 600V |
| $t_r$ | Turn-on rise time | — | 80 | 130 | | |
| $t_f$ | Turn-off fall time | — | 40 | 65 | | |
| DT | Deadtime, LS turn-off to HS turn-on & HS turn-off to LS turn-on | 480 | 650 | 820 | | |
| MT | Delay matching, HS & LS turn-on/off | — | 30 | — | | |

## Static Electrical Characteristics

$V_{BIAS}$ ($V_{CC}$, $V_{BS}$) = 15V and $T_A$ = 25°C unless otherwise specified. The $V_{IN}$, $V_{TH}$ and $I_{IN}$ parameters are referenced to COM. The $V_O$ and $I_O$ parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

| Symbol | Definition | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Logic "1" input voltage for HO & logic "0" for LO | 6.4 | — | — | V | $V_{CC}$ = 10V |
| | | 9.5 | — | — | | $V_{CC}$ = 15V |
| | | 12.6 | — | — | | $V_{CC}$ = 20V |
| $V_{IL}$ | Logic "0" input voltage for HO & logic "1" for LO | — | — | 3.8 | | $V_{CC}$ = 10V |
| | | — | — | 6.0 | | $V_{CC}$ = 15V |
| | | — | — | 8.3 | | $V_{CC}$ = 20V |
| $V_{OH}$ | High level output voltage, $V_{BIAS}$ - $V_O$ | — | — | 100 | mV | $I_O$ = 0A |
| $V_{OL}$ | Low level output voltage, $V_O$ | — | — | 100 | | $I_O$ = 0A |
| $I_{LK}$ | Offset supply leakage current | — | — | 50 | µA | $V_B$ = $V_S$ = 600V |
| $I_{QBS}$ | Quiescent $V_{BS}$ supply current | — | 50 | 100 | | $V_{IN}$ = 0V or $V_{CC}$ |
| $I_{QCC}$ | Quiescent $V_{CC}$ supply current | — | 70 | 180 | | $V_{IN}$ = 0V or $V_{CC}$ |
| $I_{IN+}$ | Logic "1" input bias current | — | 30 | 50 | | $V_{IN}$ = $V_{CC}$ |
| $I_{IN-}$ | Logic "0" input bias current | — | — | 1.0 | | $V_{IN}$ = 0V |
| $V_{BSUV+}$ | $V_{BS}$ supply undervoltage positive going threshold | 7.6 | 8.6 | 9.6 | V | |
| $V_{BSUV-}$ | $V_{BS}$ supply undervoltage negative going threshold | 7.2 | 8.2 | 9.2 | | |
| $V_{CCUV+}$ | $V_{CC}$ supply undervoltage positive going threshold | 7.6 | 8.6 | 9.6 | | |
| $V_{CCUV-}$ | $V_{CC}$ supply undervoltage negative going threshold | 7.2 | 8.2 | 9.2 | | |
| $I_{O+}$ | Output high short circuit pulsed current | 200 | 250 | — | mA | $V_O$ = 0V, $V_{IN}$ = $V_{CC}$ PW ≤10 µs |
| $I_{O-}$ | Output low short circuit pulsed current | 420 | 500 | — | | $V_O$ = 15V, $V_{IN}$ = 0V PW ≤10 µs |

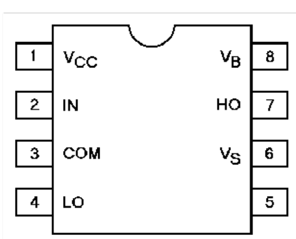
## Functional Block Diagram



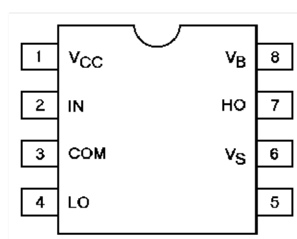

## Lead Definitions

| Symbol | Description |
|---|---|
| IN | Logic input for high side and low side gate driver outputs (HO & LO), in phase with HO |
| $V_B$ | High side floating supply |
| HO | High side gate drive output |
| $V_S$ | High side floating supply return |
| $V_{CC}$ | Low side and logic fixed supply |
| LO | Low side gate drive output |
| COM | Low side return |

## Lead Assignments




8 Lead DIP




8 Lead SOIC

| IR2111 | IR2111S |
|---|---|
| Part Number | |

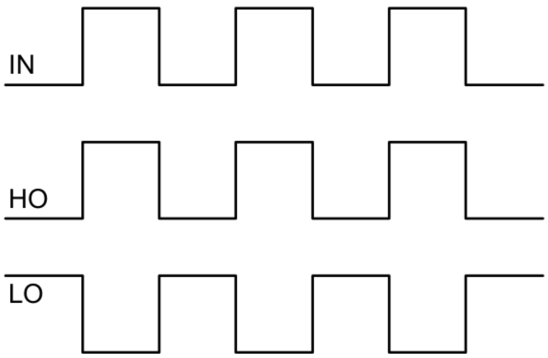



Figure 1. Input/Output Timing Diagram

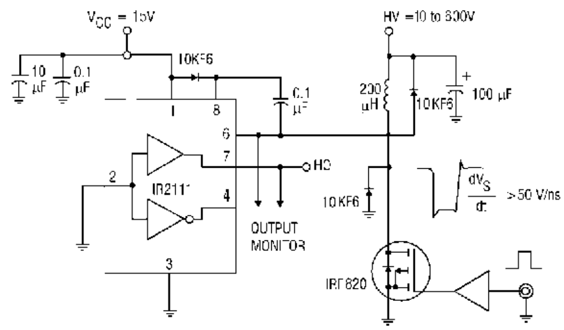



Figure 2. Floating Supply Voltage Transient Test Circuit

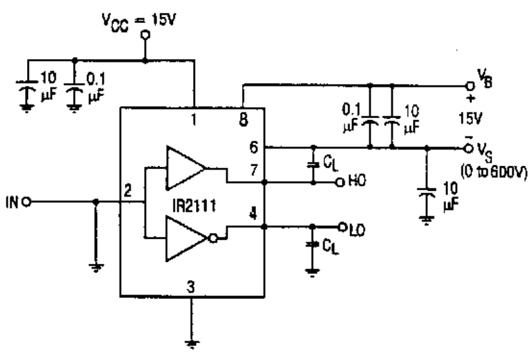



Figure 3. Switching Time Test Circuit

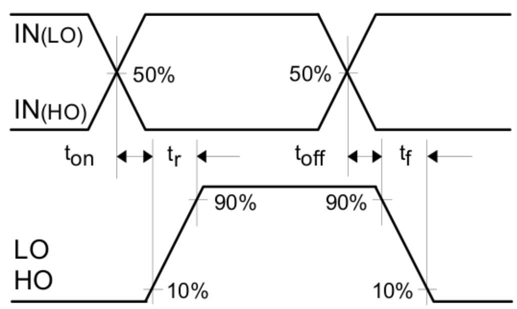



Figure 4. Switching Time Waveform Definition

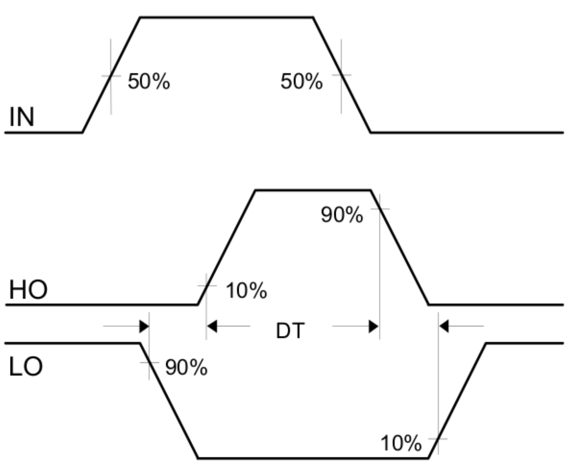



Figure 5. Deadtime Waveform Definitions

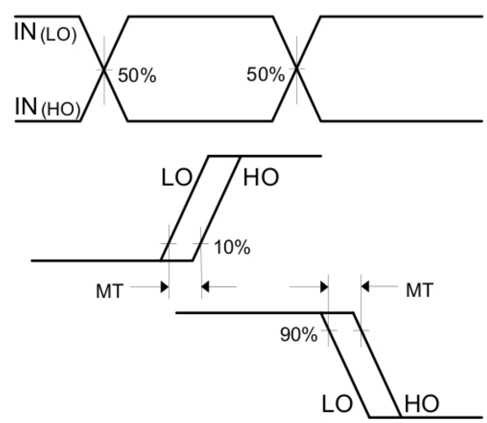



Figure 6. Delay Matching Waveform Definitions

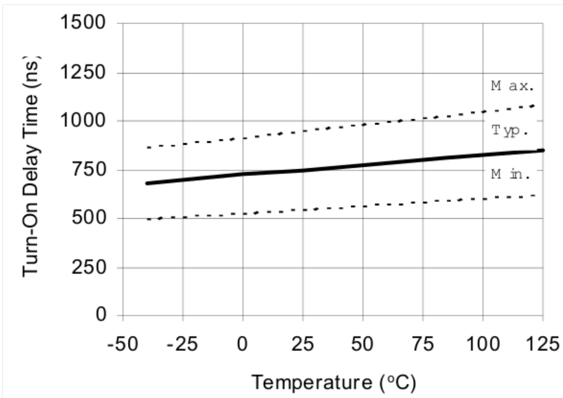



**Figure 11A Turn-On Time vs Temperature**

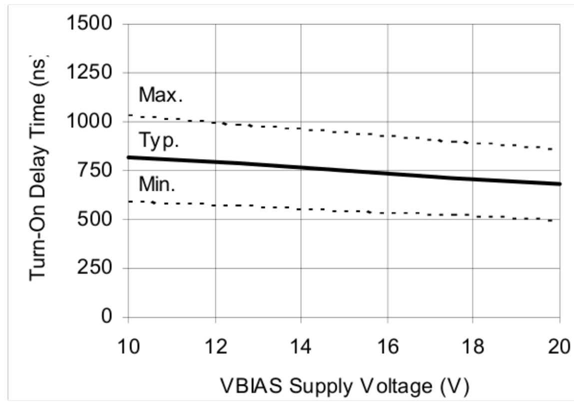



**Figure 11B Turn-On Time vs Voltage**

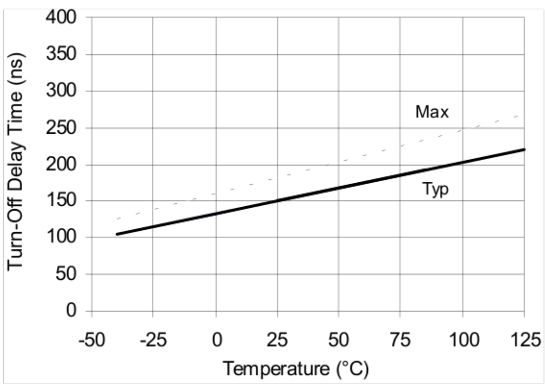



**Figure 12A Turn-Off Time vs Temperature**

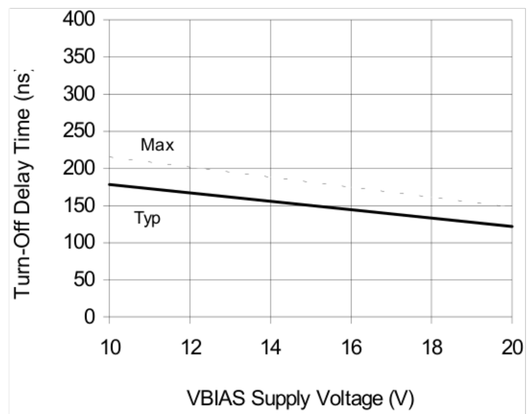



**Figure 12B Turn-Off Time vs Voltage**

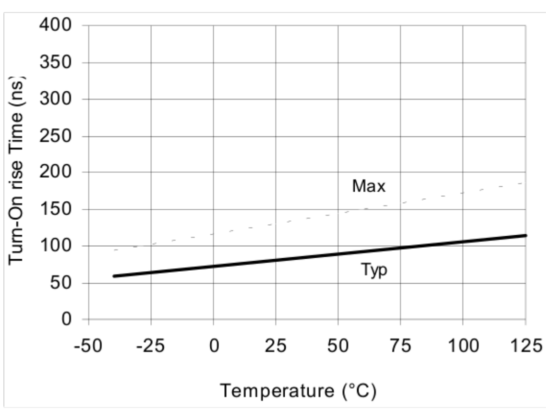



**Figure 13A Turn-On RiseTime vs Temperature**

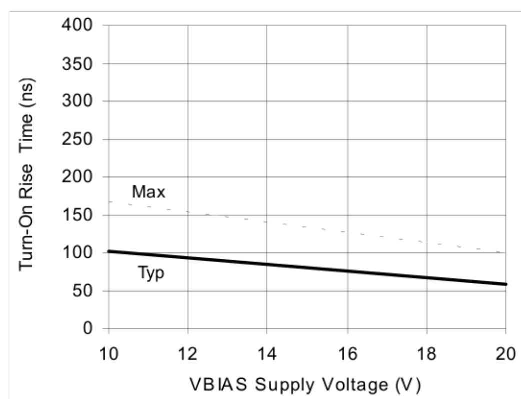



**Figure 13B Turn-On RiseTime vs Voltage**

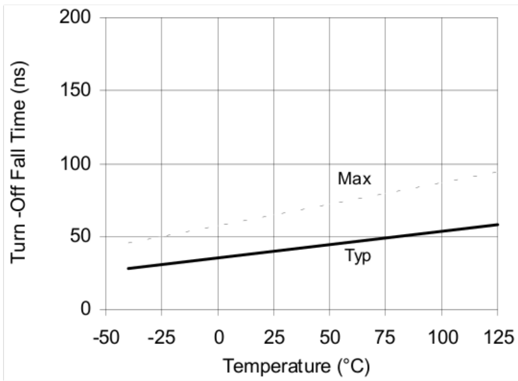



**Figure 14A Turn-Off Fall Time vs Temperature**

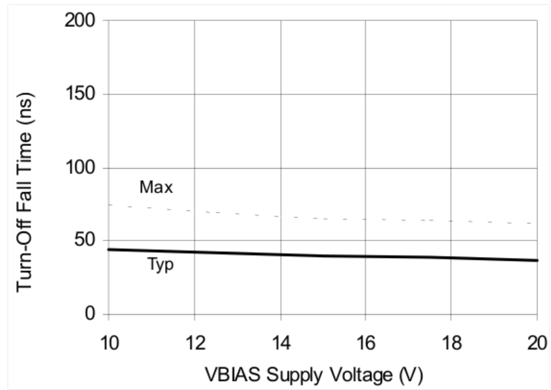



**Figure 14B Turn-Off Fall Time vs Voltage**

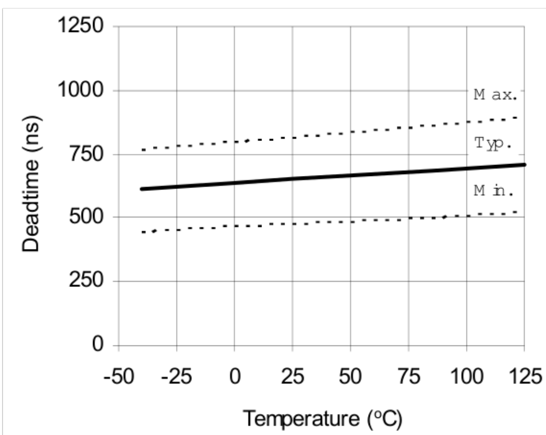



**Figure 15A Dead Time vs Temperature**

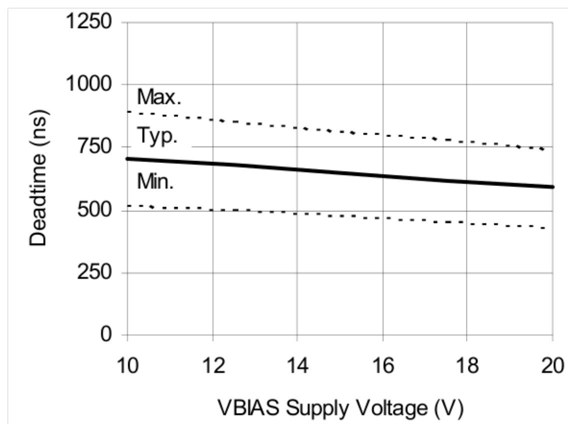



**Figure 15B Dead Time vs Voltage**

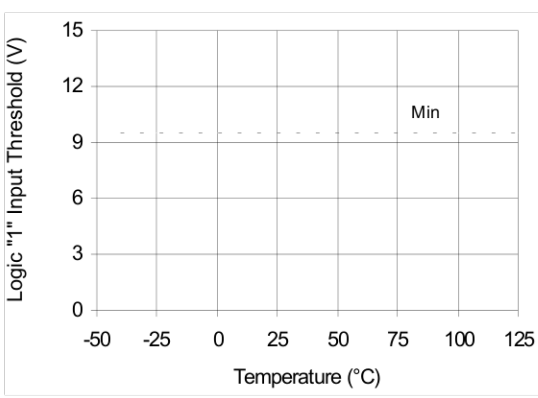



**Figure 16A Logic "I" Input voltage for HO & Logic "0" for LO vs Temperature**

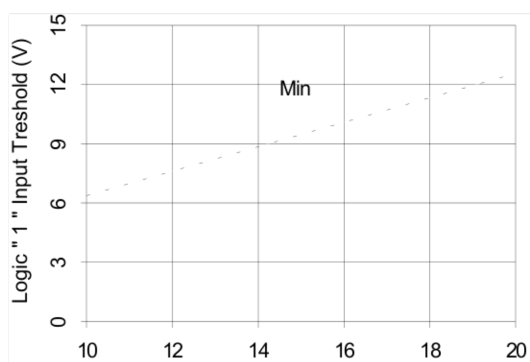



**Figure 16B Logic "I" Input voltage for HO & Logic "0" for LO vs Voltage**

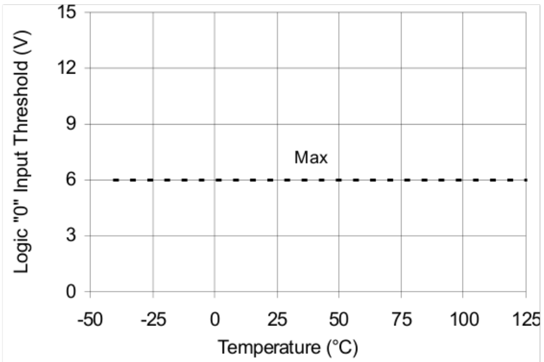



**Figure 17A Logic "0" Input voltage for HO & Logic "I" for LO vs Temperature**

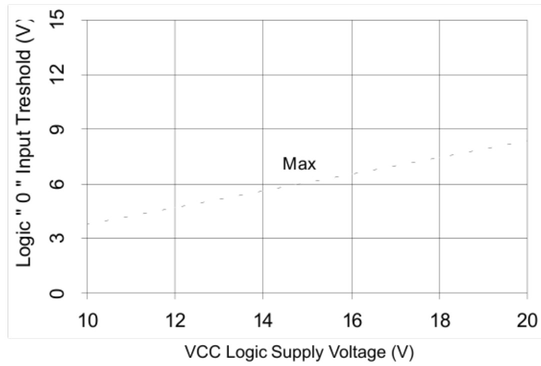



**Figure 17B Logic "0" Input voltage for HO & Logic "I" for LO vs Voltage**

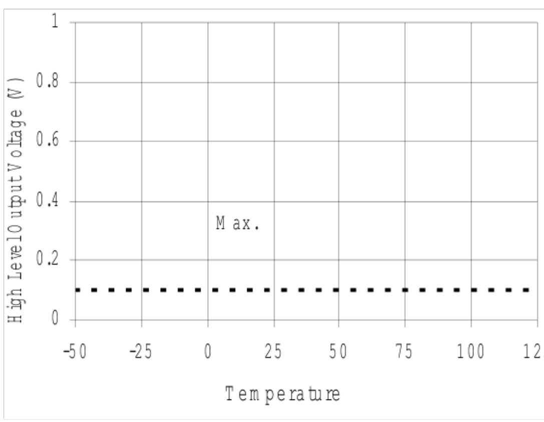



**Figure 18A. High Level Output vs. Temperature**

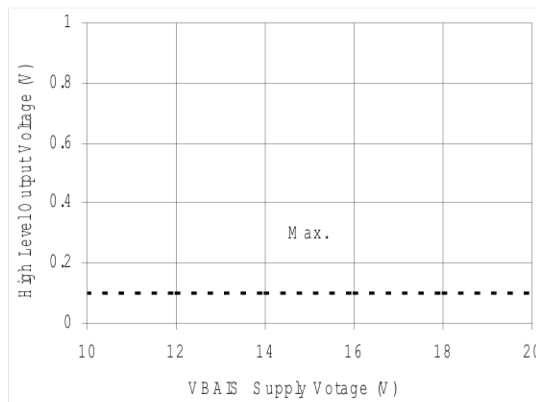



**Figure 18B. High Level Output vs. Voltage**

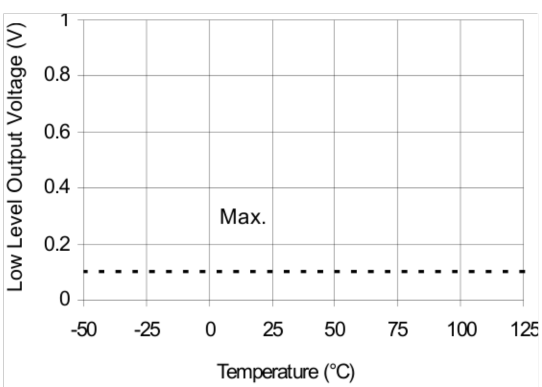



**Figure 19A. Low Level Output vs. Temperature**

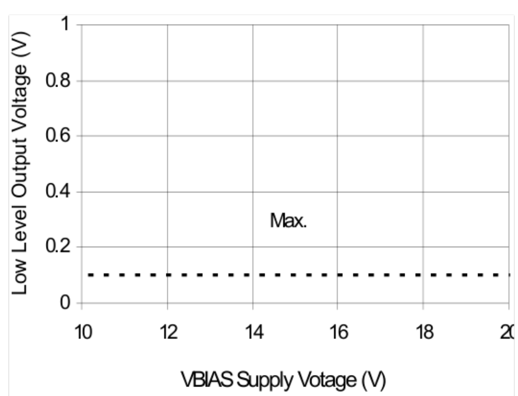



**Figure 19B. Low Level Output vs. Voltage**

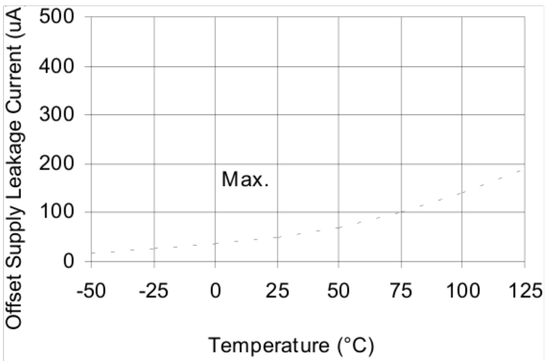



**Figure 20A Offset Supply Current vs Temperature**

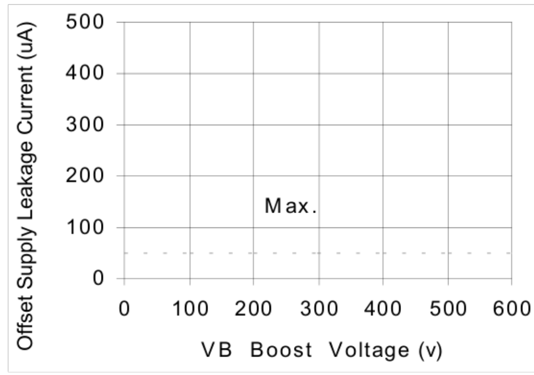



**Figure 20B Offset Supply Current vs Voltage**

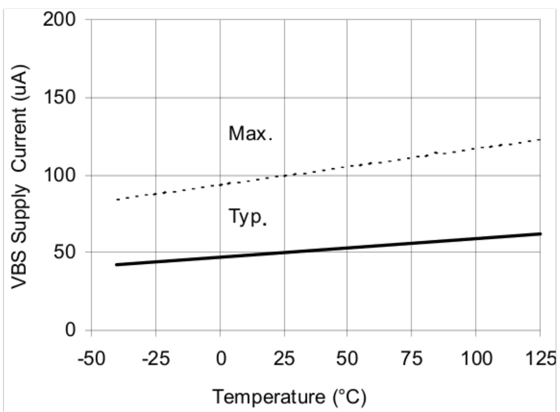



**Figure 21A VBS Supply Current vs Temperature**

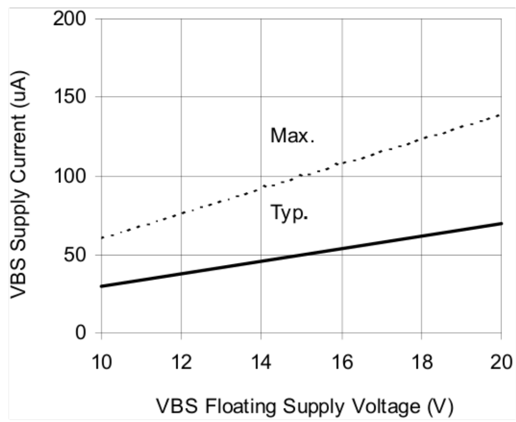



**Figure 21B VBS Supply Current vs Voltage**

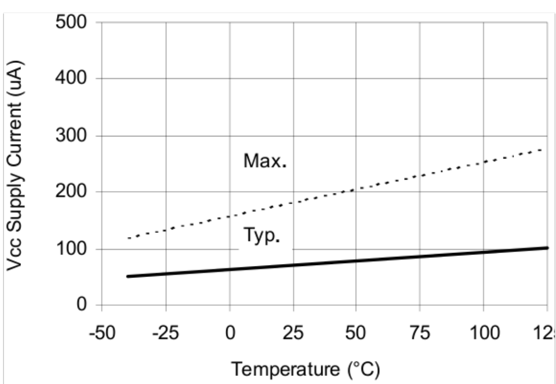



**Figure 22A VCC Supply Current vs Temperature**

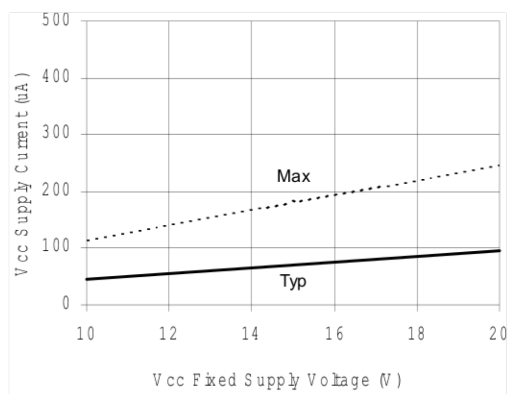



**Figure 22B VCC Supply Current vs Voltage**

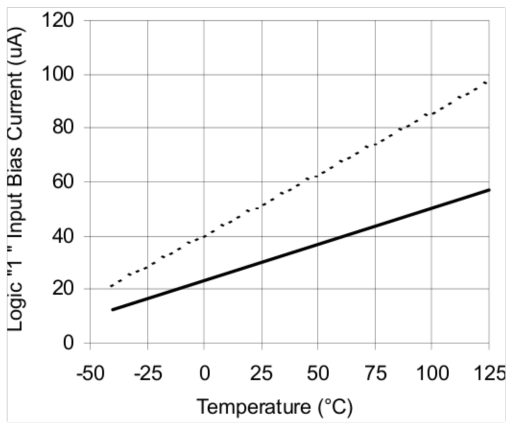



**Figure 23A Logic “1” Input Current vs Temperature**

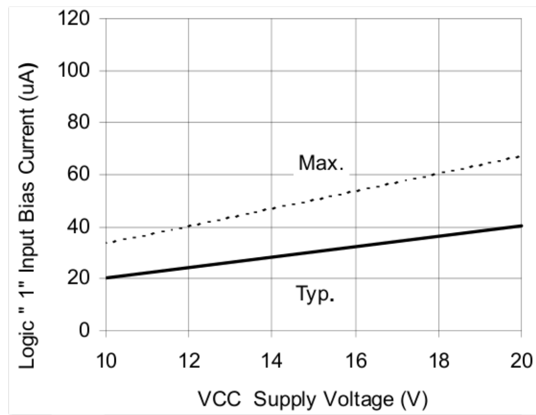



**Figure 23B Logic “1” Input Current vs $V_{CC}$ Voltage**

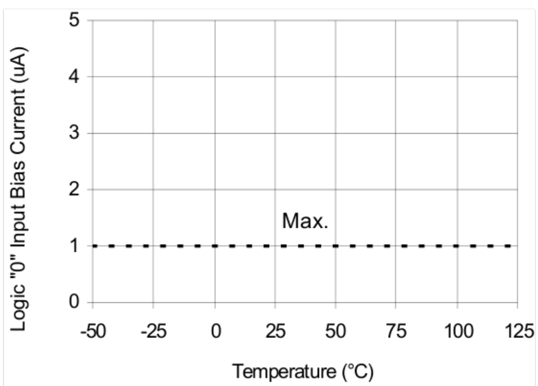



**Figure 24A. Logic “0” Input Current vs. Temperature**

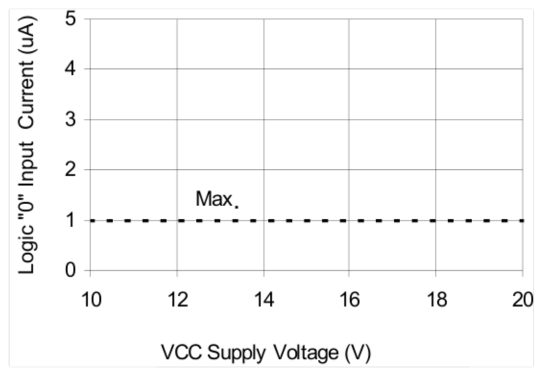



**Figure 24B. Logic “0” Input Current vs. $V_{CC}$ Voltage**

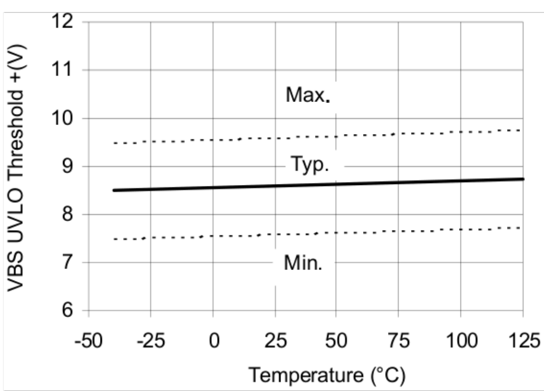



**Figure 25 VBS Undervoltage Threshold (+) vsTemperature**

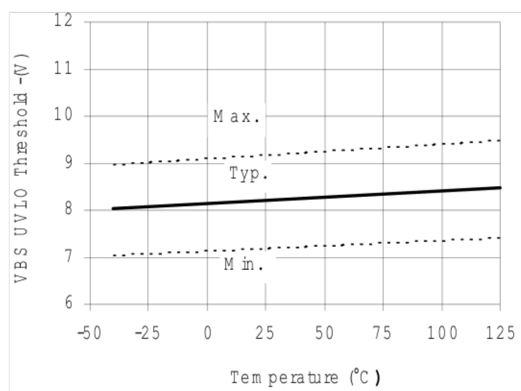



**Figure 26 VBS Undervoltage Threshold (-) vsTemperature**

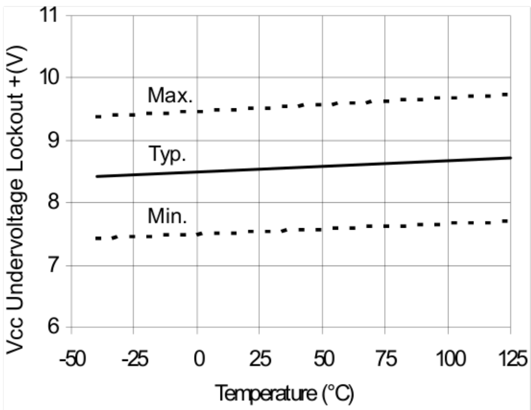



**Figure 27 Vcc Undervoltage (-) vs Temperature**

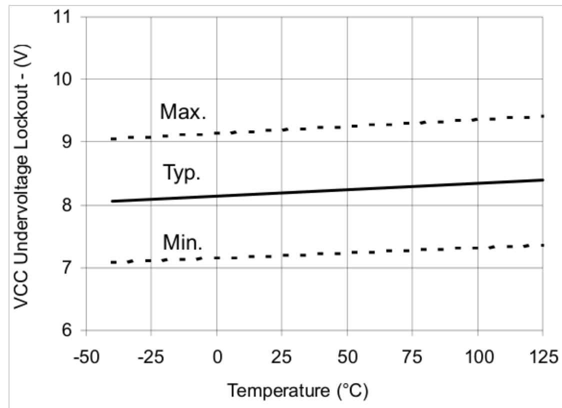



**Figure 28 Vcc Undervoltage (-) vs Temperature**

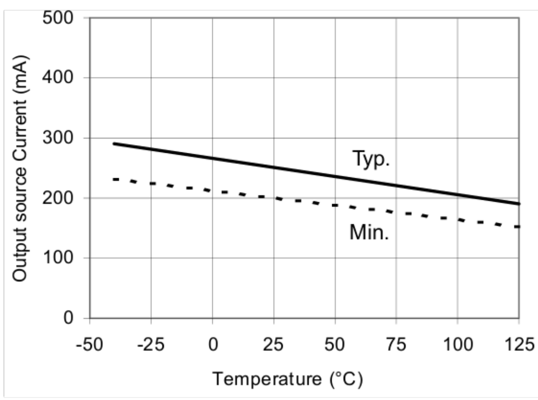



**Figure 29A Output Source Current vs Temperature**

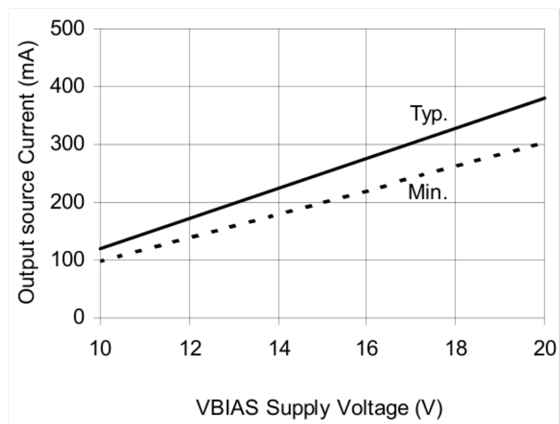



**Figure 29B Output Source Current vs Voltage**

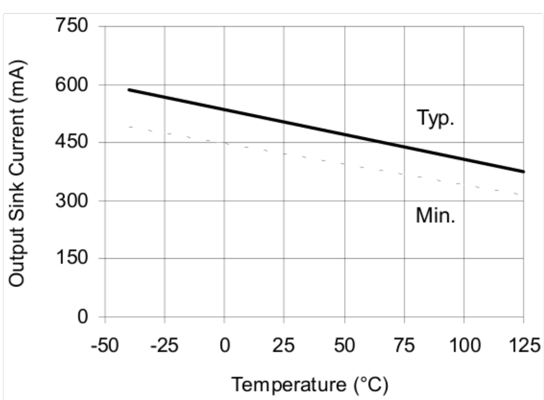



**Figure 30A Output Sink Current vs Temperature**

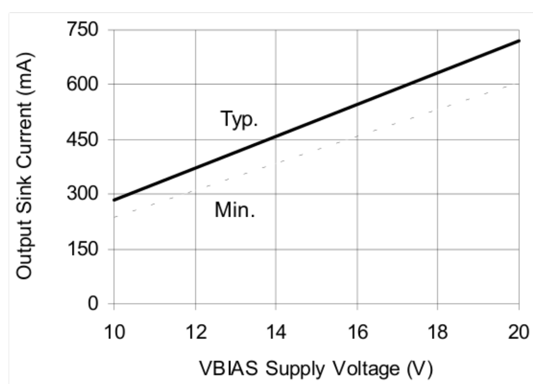
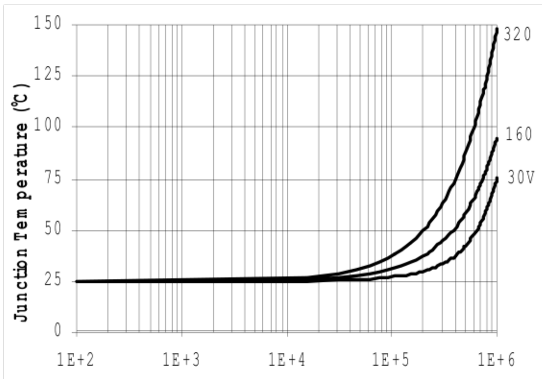
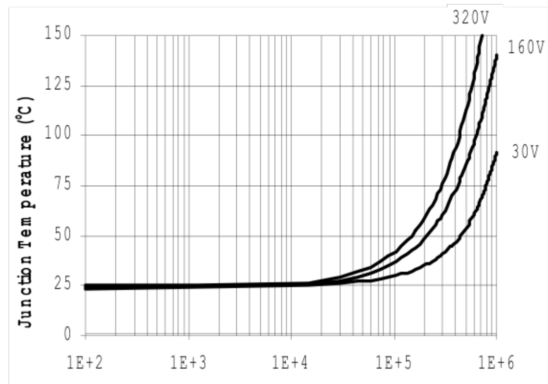



**Figure 30B Output Sink Current vs Voltage**



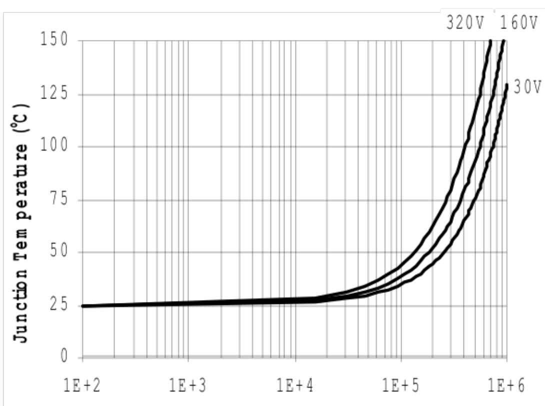

Frequency (Hz)

**Figure 31. IR2111 $T_J$ vs. Frequency (IRFBC20)**
**$R_{GATE}$ = 33Ω, $V_{CC}$ = 15V**



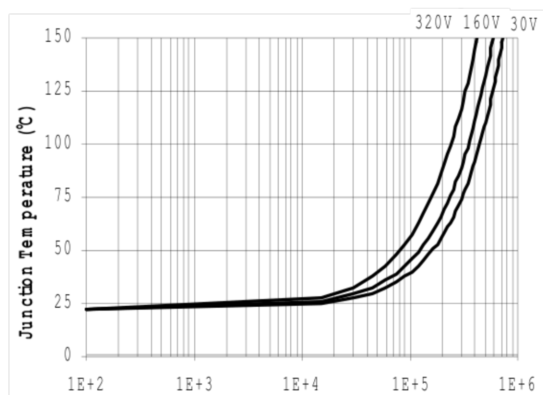

Frequency (Hz)

**Figure 32. IR2111 $T_J$ vs. Frequency (IRFBC30)**
**$R_{GATE}$ = 22Ω, $V_{CC}$ = 15V**




Frequency (Hz)

**Figure33. IR2111 $T_J$ vs. Frequency (IRFBC40)**
**$R_{GATE}$ = 15Ω, $V_{CC}$ = 15V**




Frequency (Hz)

**Figure 34. IR2111 $T_J$ vs. Frequency (IRFPC50)**
**$R_{GATE}$ = 10Ω, $V_{CC}$ = 15V**

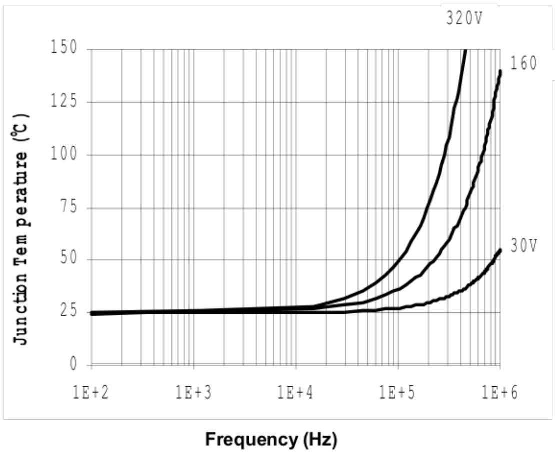



**Figure 35. IR2111S $T_J$ vs. Frequency (IRFBC20)**
**$R_{GATE}$ = 33Ω, $V_{CC}$ = 15V**

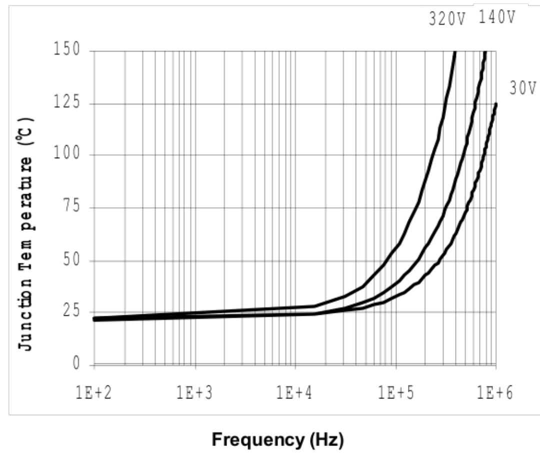



**Figure 36. IR2111S $T_J$ vs. Frequency (IRFBC30)**
**$R_{GATE}$ = 22Ω, $V_{CC}$ = 15V**

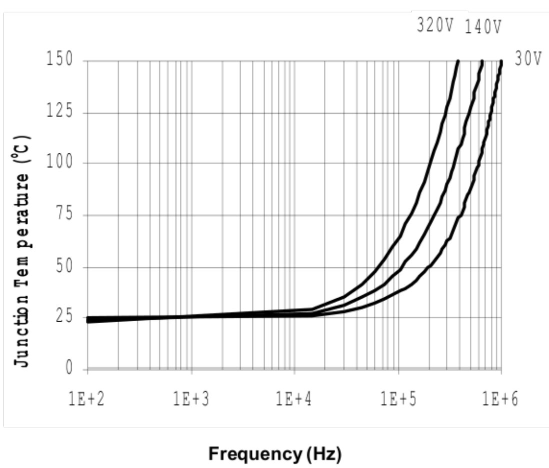



**Figure 37. IR2111S $T_J$ vs. Frequency (IRFBC40)**
**$R_{GATE}$ = 15Ω, $V_{CC}$ = 15V**

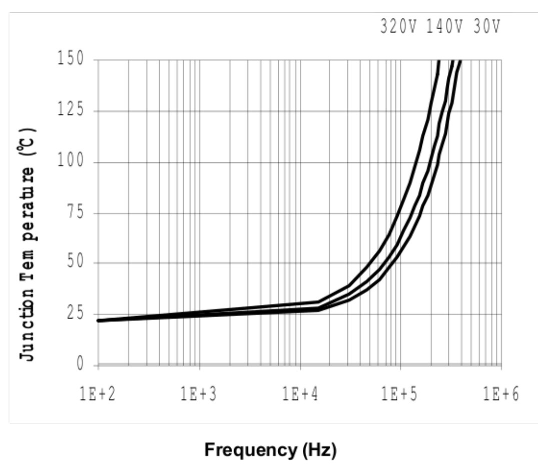
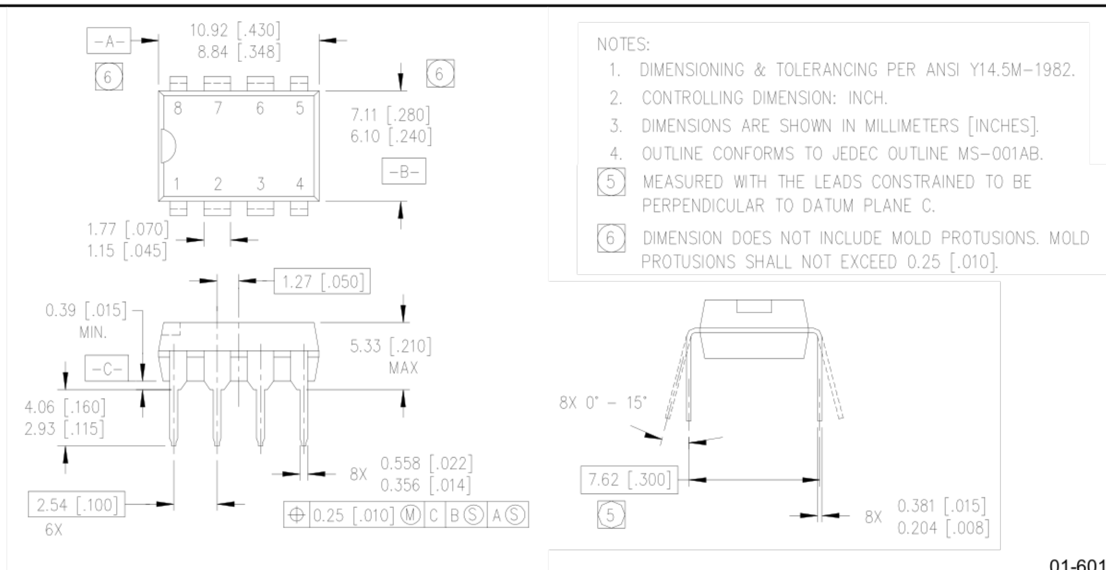


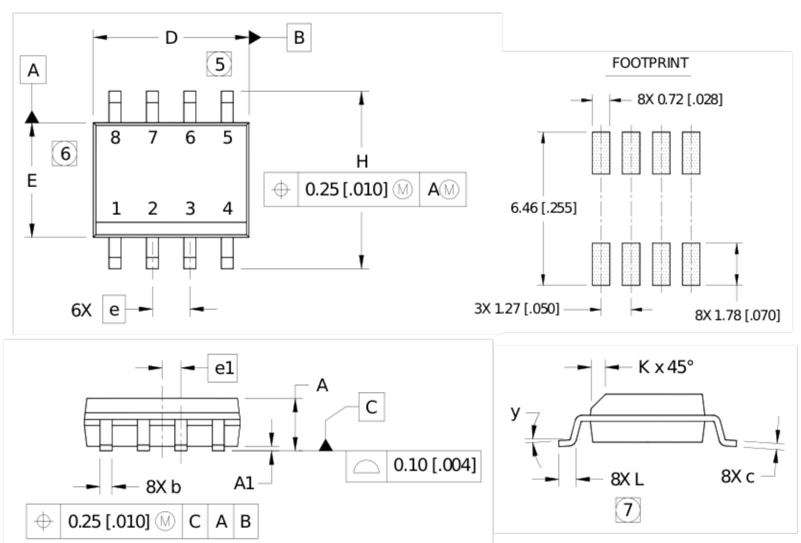

**Figure 38. IR2111S $T_J$ vs. Frequency (IRFPC50)**
**$R_{GATE}$ = 10Ω, $V_{CC}$ = 15V**

## Case outlines




**8-Lead PDIP**

01-6014
01-3003 01 (MS-001AB)




| DIM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | .0532 | .0688 | 1.35 | 1.75 |
| A1 | .0040 | .0098 | 0.10 | 0.25 |
| b | .013 | .020 | 0.33 | 0.51 |
| c | .0075 | .0098 | 0.19 | 0.25 |
| D | .189 | .1968 | 4.80 | 5.00 |
| E | .1497 | .1574 | 3.80 | 4.00 |
| e | .050 BASIC | | 1.27 BASIC | |
| e 1 | .025 BASIC | | 0.635 BASIC | |
| H | .2284 | .2440 | 5.80 | 6.20 |
| K | .0099 | .0196 | 0.25 | 0.50 |
| L | .016 | .050 | 0.40 | 1.27 |
| y | 0° | 8° | 0° | 8° |

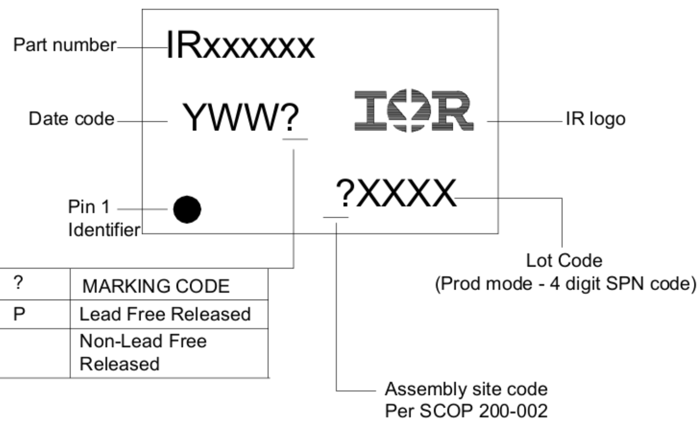
NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

**8-Lead SOIC**

01-6027
01-0021 11 (MS-012AA)

## LEADFREE PART MARKING INFORMATION




| ? | MARKING CODE |
|---|---|
| P | Lead Free Released |
| | Non-Lead Free Released |

## ORDER INFORMATION

**Basic Part (Non-Lead Free)**
8-Lead PDIP IR2111 order IR2111
8-Lead SOIC IR2111S order IR2111S

**Leadfree Part**
8-Lead PDIP IR2111 order IR2111PbF
8-Lead SOIC IR2111S order IR2111SPbF

International
IOR Rectifier
**IR WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105
**This product has been qualified per industrial level**
*Data and specifications subject to change without notice. 4/12/2004*