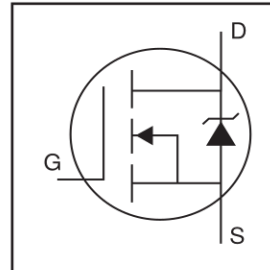


**Typical Applications**

- Climate Control, ABS, Electronic Braking, Windshield Wipers

**Features**

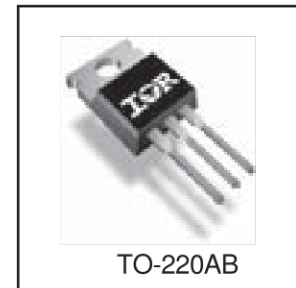
- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax



$V_{DSS} = 55V$
$R_{DS(on)} = 4.7m\Omega$
$I_D = 75A$

**Description**

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.



**Absolute Maximum Ratings**

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon limited)	175	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (See Fig.9)	120	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Package limited)	75	
$I_{DM}$	Pulsed Drain Current ①	700	
$P_D @ T_C = 25^\circ C$	Power Dissipation	330	W
	Linear Derating Factor	2.2	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy②	450	mJ
$E_{AS} (6 \text{ sigma})$	Single Pulse Avalanche Energy Tested Value②	1220	
$I_{AR}$	Avalanche Current③	See Fig.12a, 12b, 15, 16	A
$E_{AR}$	Repetitive Avalanche Energy③		mJ
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	
	Mounting Torque, 6-32 or M3 screw	1.1 (10)	N•m (lbf•in)

**Thermal Resistance**

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.45	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

HEXFET(R) is a registered trademark of International Rectifier.

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# IRF2805

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## Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	55	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS/ΔT<sub>J</sub></sub>	Breakdown Voltage Temp. Coefficient	—	0.06	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DSON</sub>	Static Drain-to-Source On-Resistance	—	3.9	4.7	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 104A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> = 10V, I <sub>D</sub> = 250μA
g <sub>fs</sub>	Forward Transconductance	91	—	—	S	V <sub>DS</sub> = 25V, I <sub>D</sub> = 104A
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	20	μA	V <sub>DS</sub> = 55V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 55V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	200	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V <sub>GS</sub> = -20V
Q <sub>g</sub>	Total Gate Charge	—	150	230	nC	I <sub>D</sub> = 104A
Q <sub>gs</sub>	Gate-to-Source Charge	—	38	57		V <sub>DS</sub> = 44V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	52	78		V <sub>GS</sub> = 10V ④
t <sub>d(on)</sub>	Turn-On Delay Time	—	14	—	ns	V <sub>DD</sub> = 28V
t <sub>r</sub>	Rise Time	—	120	—		I <sub>D</sub> = 104A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	68	—		R <sub>G</sub> = 2.5Ω
t <sub>f</sub>	Fall Time	—	110	—		V <sub>GS</sub> = 10V ④
L <sub>D</sub>	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L <sub>S</sub>	Internal Source Inductance	—	7.5	—		
C <sub>iss</sub>	Input Capacitance	—	5110	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	1190	—		V <sub>DS</sub> = 25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	210	—		f = 1.0MHz, See Fig. 5
C <sub>oss</sub>	Output Capacitance	—	6470	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 1.0V, f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	860	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 44V, f = 1.0MHz
C <sub>oss eff.</sub>	Effective Output Capacitance ⑤	—	1600	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 44V

## Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	175	A	MOSFET symbol showing the integral reverse p-n junction diode.
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	700		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 104A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	80	120	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 104A
Q <sub>rr</sub>	Reverse Recovery Charge	—	290	430	nC	di/dt = 100A/μs ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Starting T<sub>J</sub> = 25°C, L = 0.08mH  
R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 104A. (See Figure 12).
- ③ I<sub>SD</sub> ≤ 104A, di/dt ≤ 240A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>,  
T<sub>J</sub> ≤ 175°C
- ④ Pulse width ≤ 400μs; duty cycle ≤ 2%.

- ⑤ C<sub>oss eff.</sub> is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
- ⑥ Limited by T<sub>Jmax</sub>, see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑦ This value determined from sample failure population. 100% tested to this value in production.

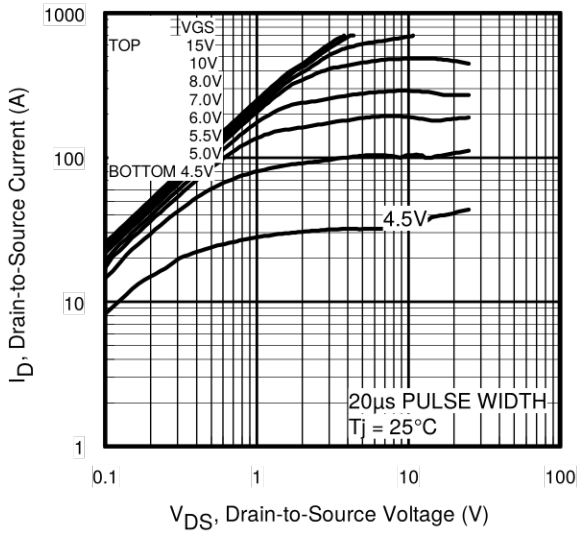


Fig 1. Typical Output Characteristics

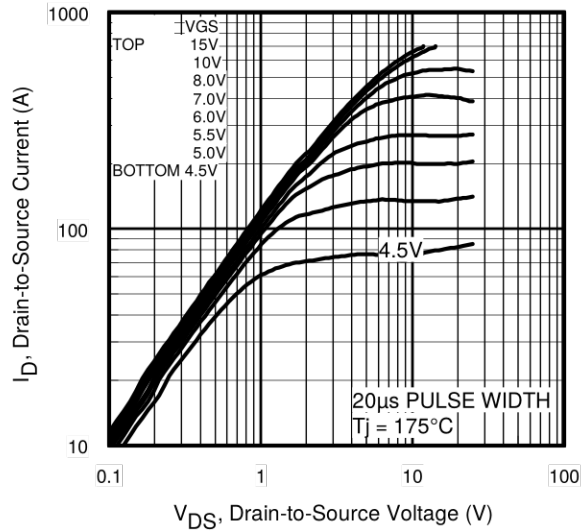


Fig 2. Typical Output Characteristics

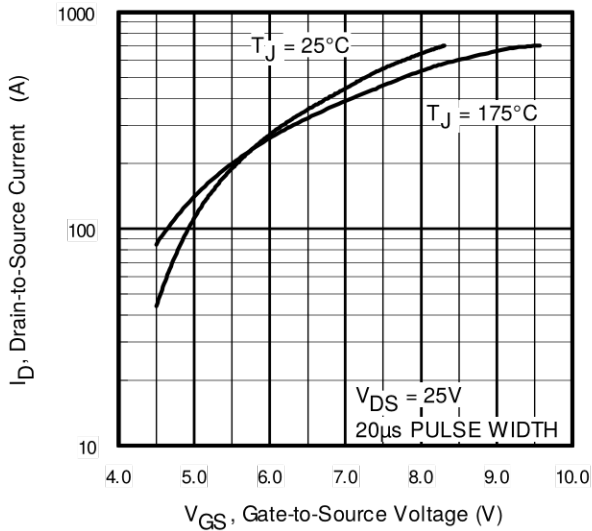


Fig 3. Typical Transfer Characteristics

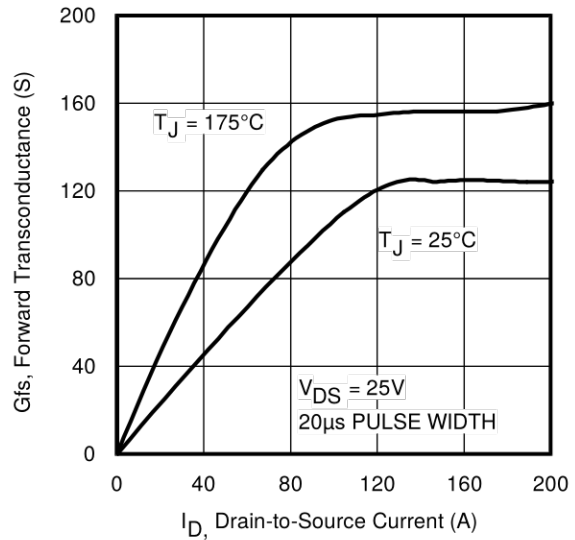
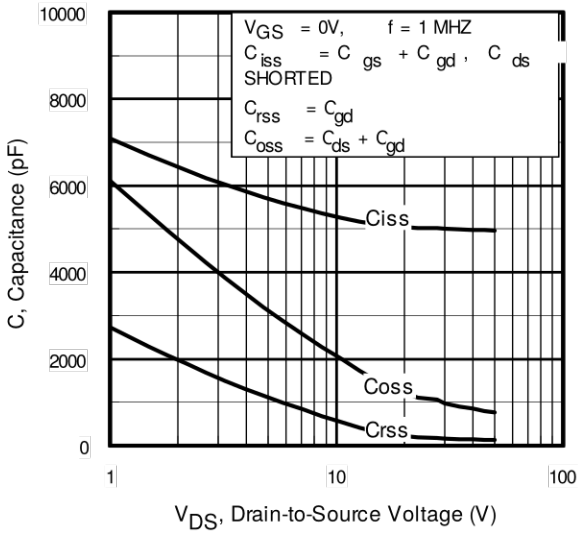
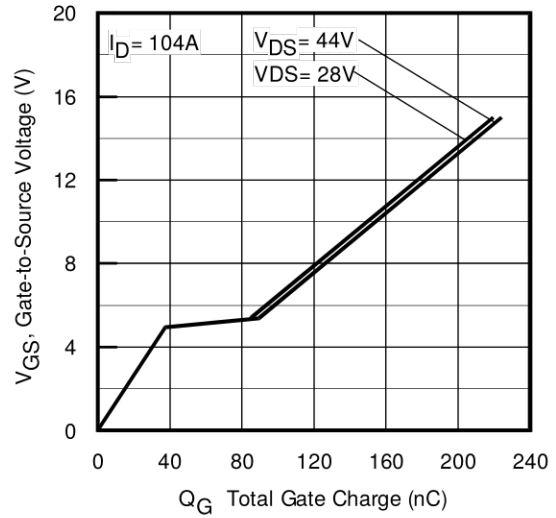


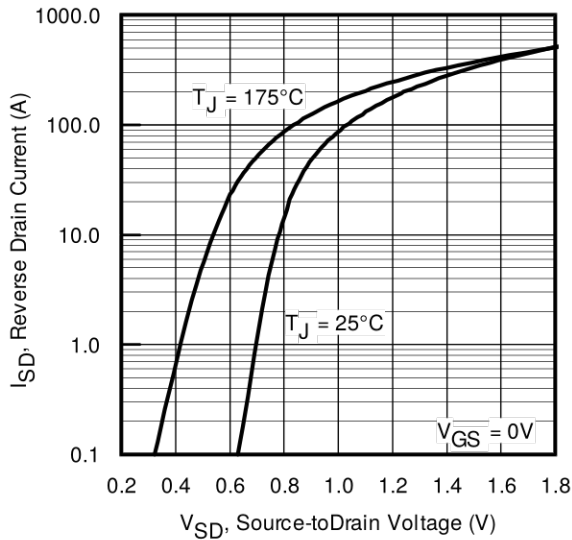
Fig 4. Typical Forward Transconductance Vs. Drain Current



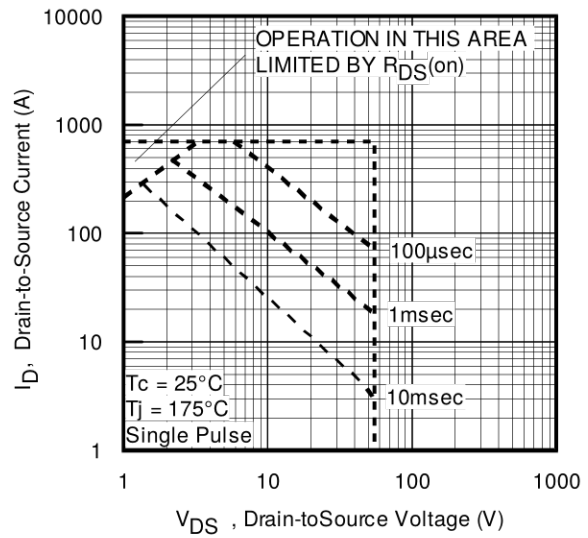
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



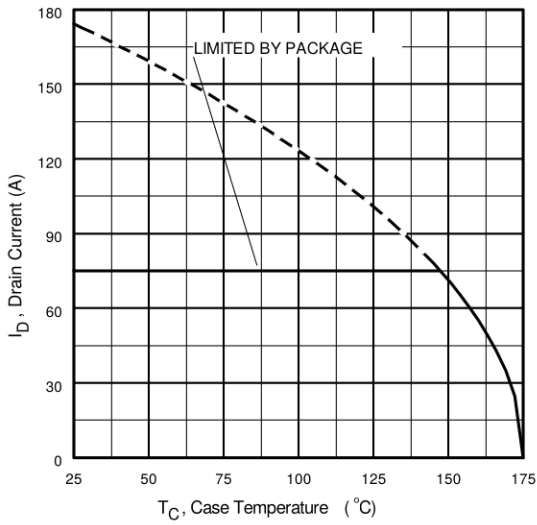
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



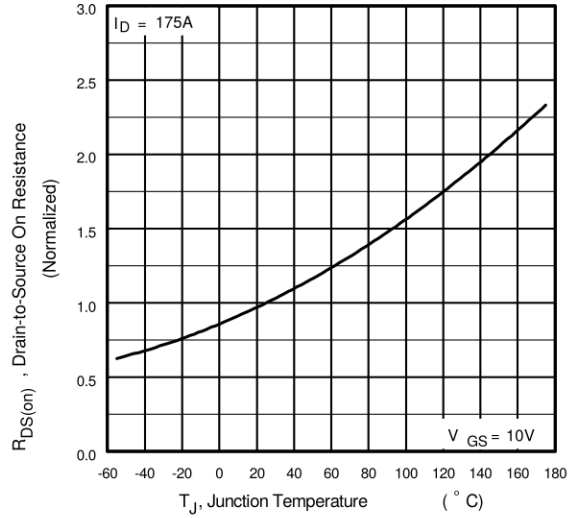
**Fig 7.** Typical Source-Drain Diode Forward Voltage



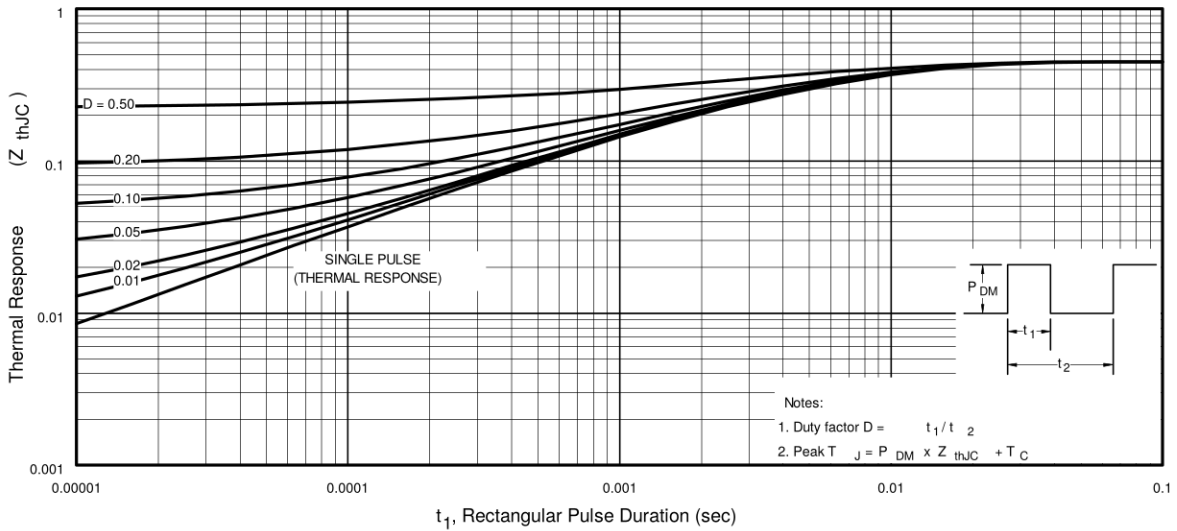
**Fig 8.** Maximum Safe Operating Area



**Fig 9.** Maximum Drain Current Vs. Case Temperature

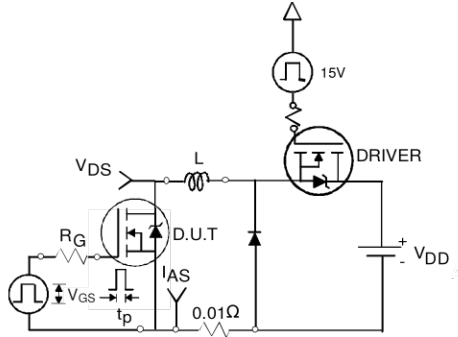


**Fig 10.** Normalized On-Resistance Vs. Temperature

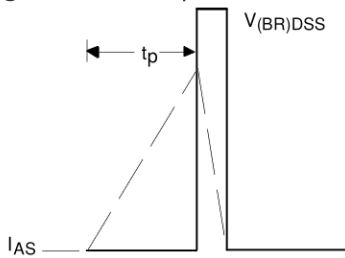


**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

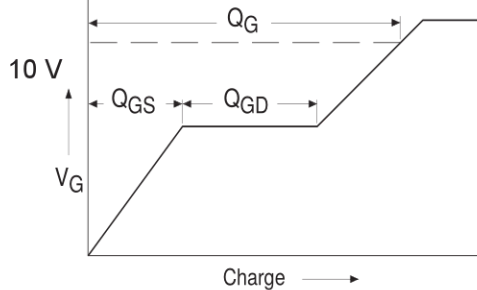
# IRF2805



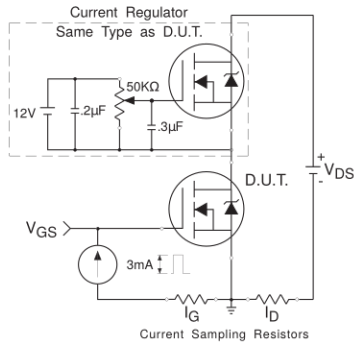
**Fig 12a.** Unclamped Inductive Test Circuit



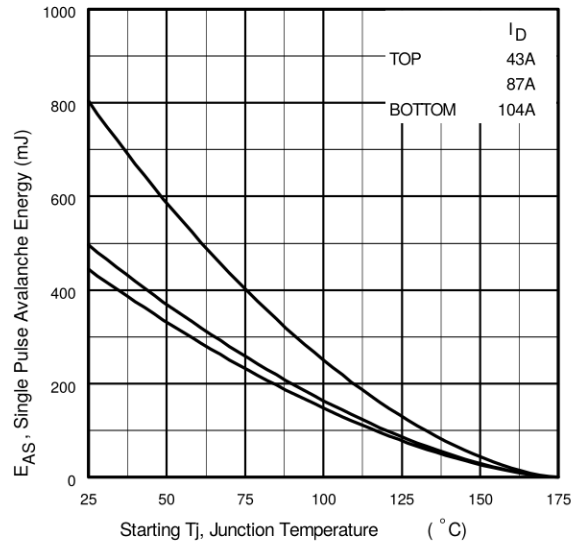
**Fig 12b.** Unclamped Inductive Waveforms



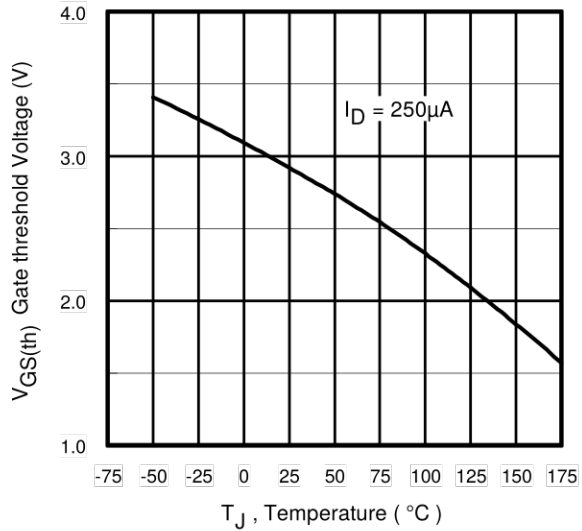
**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 14.** Threshold Voltage Vs. Temperature

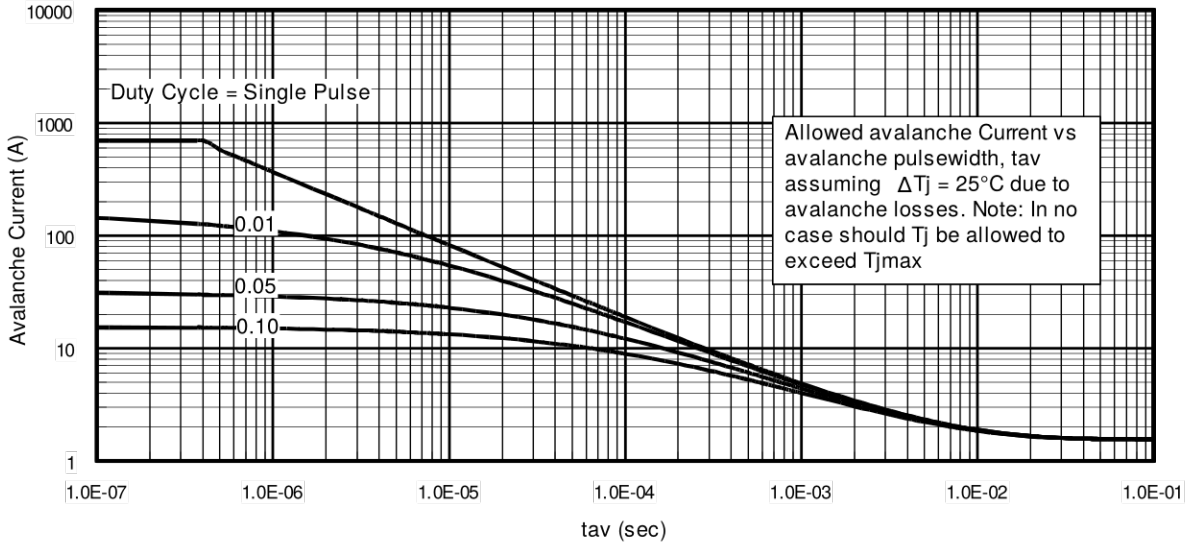


Fig 15. Typical Avalanche Current Vs.Pulsewidth

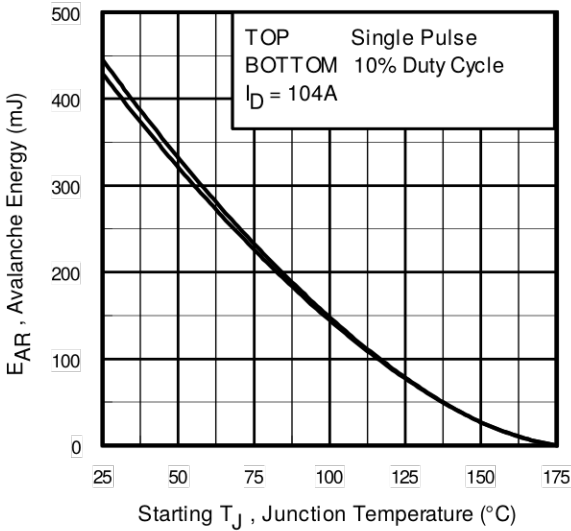


Fig 16. Maximum Avalanche Energy Vs. Temperature

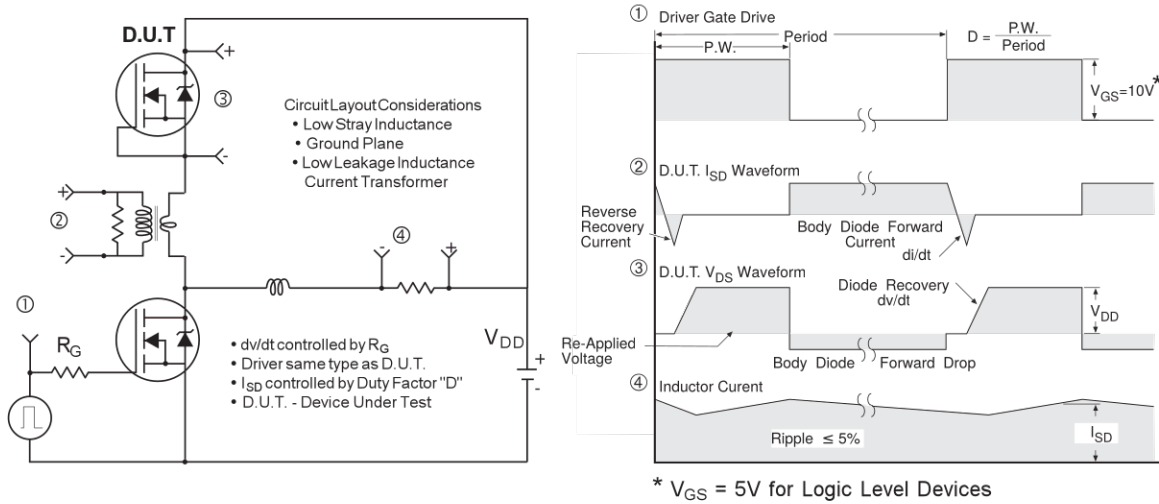
**Notes on Repetitive Avalanche Curves , Figures 15, 16:**  
**(For further info, see AN-1005 at www.irf.com)**

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 15, 16).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see figure 11)

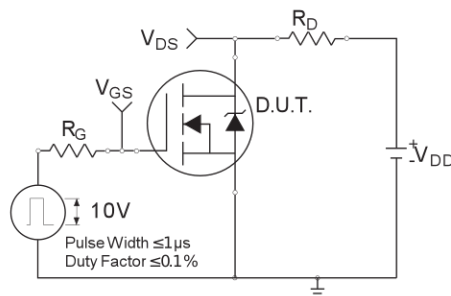
$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$



**Fig 17. Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs**



**Fig 18a. Switching Time Test Circuit**

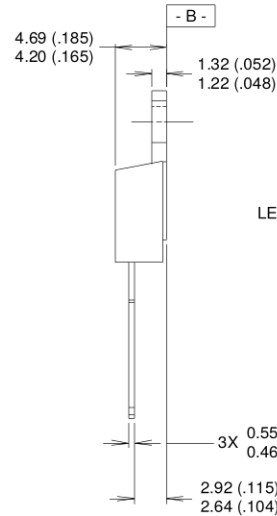
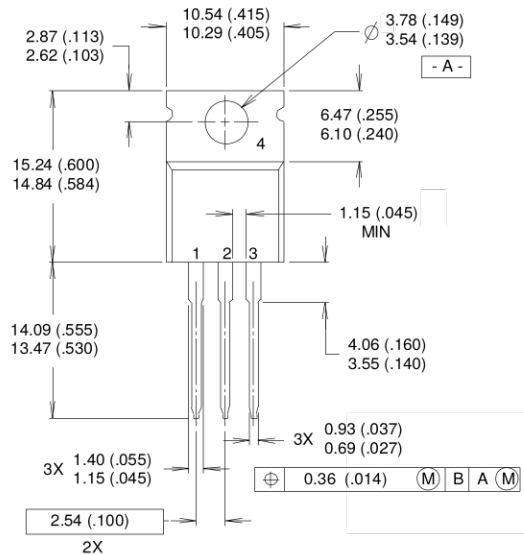


**Fig 18b. Switching Time Waveforms**



## TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



### LEAD ASSIGNMENTS

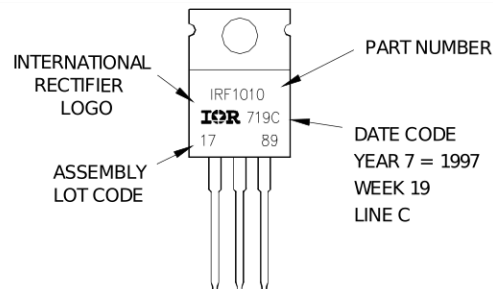
- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE
- 4 - DRAIN

### NOTES:

- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH
- 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
- 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

## TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010  
LOT CODE 1789  
ASSEMBLED ON WW 19, 1997  
IN THE ASSEMBLY LINE "C"



Data and specifications subject to change without notice.  
This product has been designed and qualified for the Automotive [Q101] market.  
Qualification Standards can be found on IR's Web site.

International  
**IR** Rectifier

**IR WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105  
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Note: For the most current drawings please refer to the IR website at:  
<http://www.irf.com/package/>