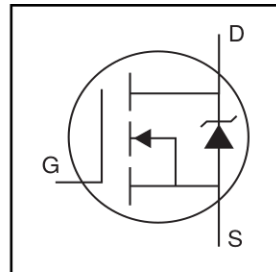


- Advanced Process Technology
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated

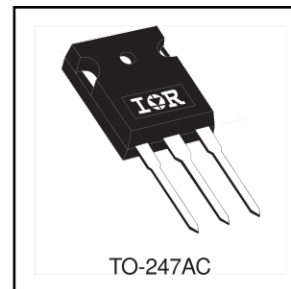


$V_{DSS} = 100V$
$R_{DS(on)} = 0.036\Omega$
$I_D = 42A$

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole.



Absolute Maximum Ratings

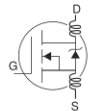
	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	42	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	30	
I_{DM}	Pulsed Drain Current ①⑤	140	
$P_D @ T_C = 25^\circ C$	Power Dissipation	160	W
	Linear Derating Factor	1.1	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②⑤	420	mJ
I_{AR}	Avalanche Current①⑤	22	A
E_{AR}	Repetitive Avalanche Energy①	16	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑤	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.95	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	40	

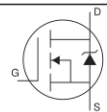
Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS/ΔT_J}	Breakdown Voltage Temp. Coefficient	—	0.11	—	V/°C	Reference to 25°C, I _D = 1mA ^⑤
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.036	Ω	V _{GS} = 10V, I _D = 23A ^④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
g _{fs}	Forward Transconductance	14	—	—	S	V _{DS} = 25V, I _D = 22A ^⑤
I _{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V _{DS} = 100V, V _{GS} = 0V
		—	—	250		V _{DS} = 80V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -20V
Q _g	Total Gate Charge	—	—	110	nC	I _D = 22A
Q _{gs}	Gate-to-Source Charge	—	—	15		V _{DS} = 80V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	58		V _{GS} = 10V, See Fig. 6 and 13 ^{④⑤}
t _{d(on)}	Turn-On Delay Time	—	11	—	ns	V _{DD} = 50V
t _r	Rise Time	—	56	—		I _D = 22A
t _{d(off)}	Turn-Off Delay Time	—	45	—		R _G = 3.6Ω
t _f	Fall Time	—	40	—		R _D = 2.9Ω See Fig. 10 ^{④⑤}
L _D	Internal Drain Inductance	—	5.0	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L _S	Internal Source Inductance	—	13	—		
C _{iss}	Input Capacitance	—	1900	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	450	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	230	—		f = 1.0MHz, See Fig. 5 ^⑤



Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	42	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ^{①⑤}	—	—	140		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 23A, V _{GS} = 0V ^④
t _{rr}	Reverse Recovery Time	—	180	270	ns	T _J = 25°C, I _F = 22A
Q _{rr}	Reverse Recovery Charge	—	1.2	1.8	μC	di/dt = 100A/μs ^{④⑤}
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				



Notes:

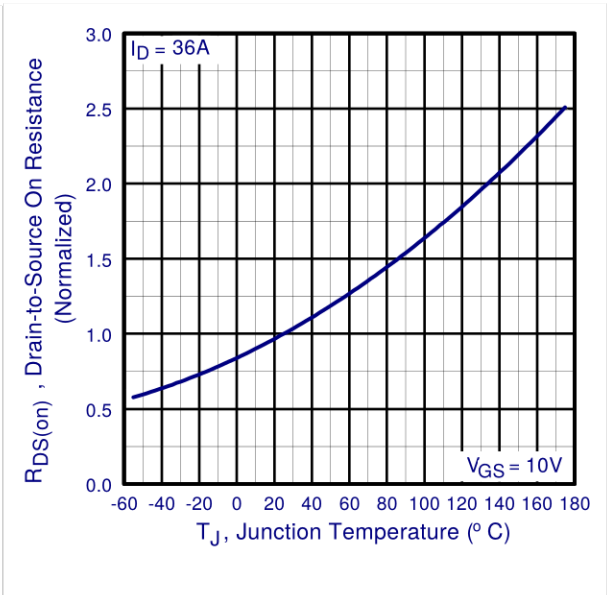
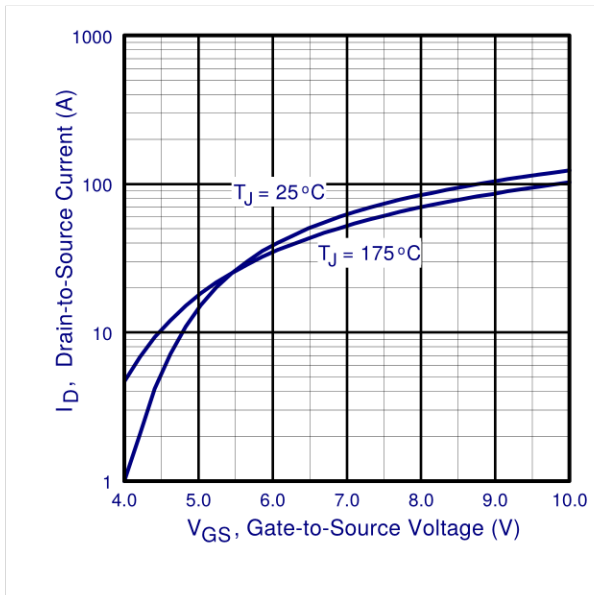
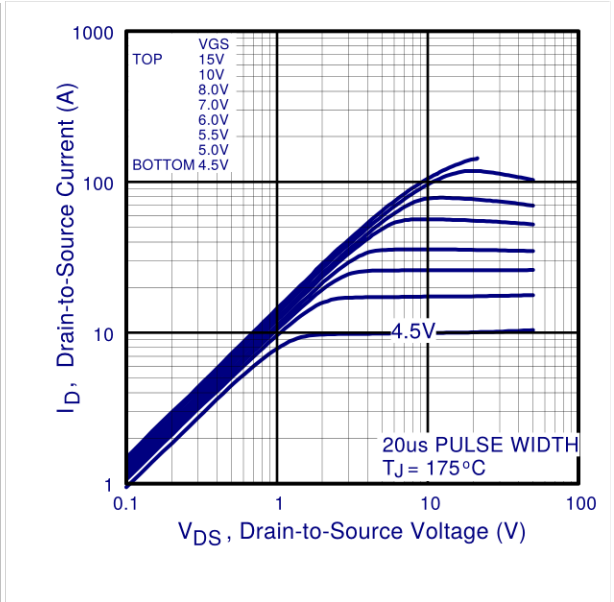
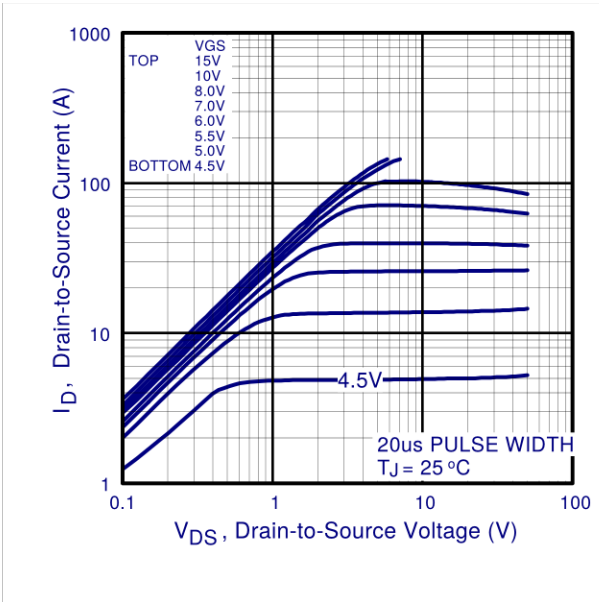
① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting T_J = 25°C, L = 1.7mH
R_G = 25Ω, I_{AS} = 22A. (See Figure 12)

③ I_{SD} ≤ 22A, di/dt ≤ 180A/μs, V_{DD} ≤ V_{(BR)DSS},
T_J ≤ 175°C

④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

⑤ Uses IRF1310N data and test conditions.



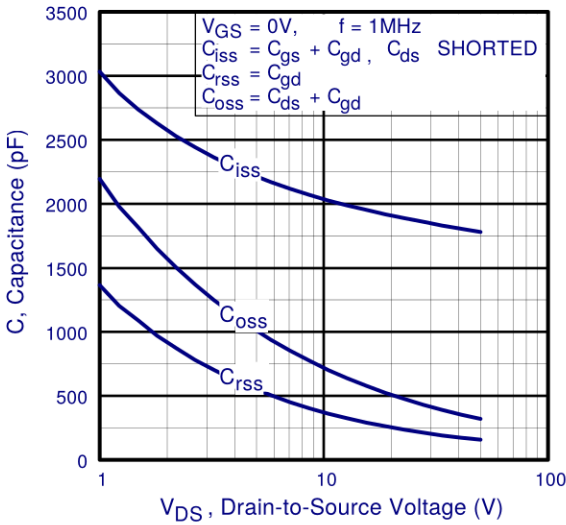


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

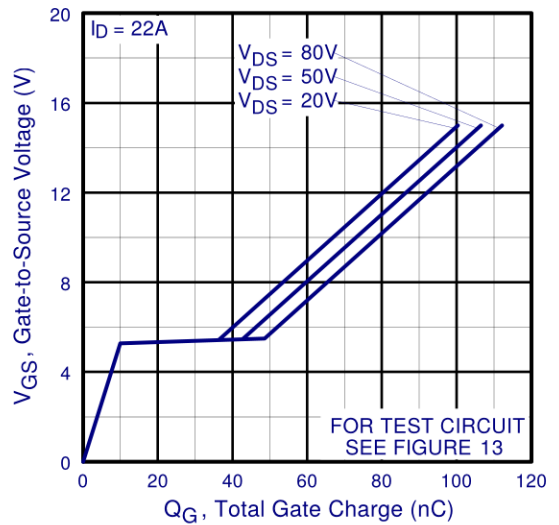


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

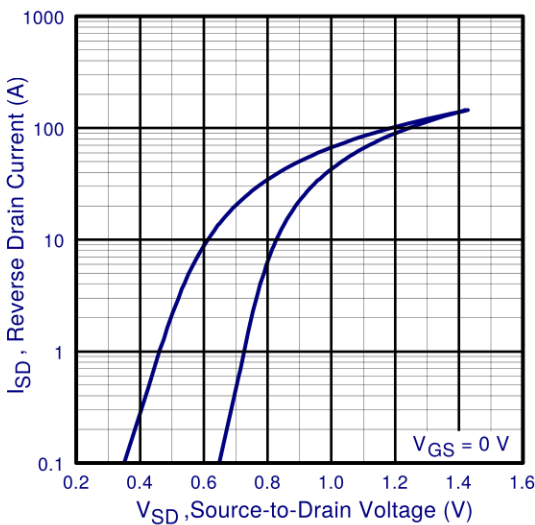


Fig 7. Typical Source-Drain Diode Forward Voltage

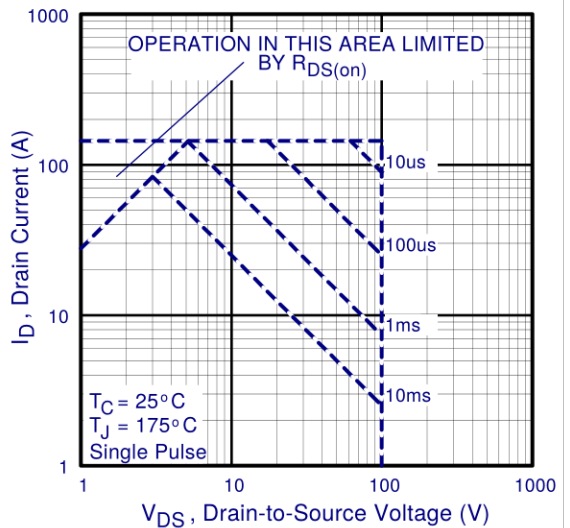


Fig 8. Maximum Safe Operating Area

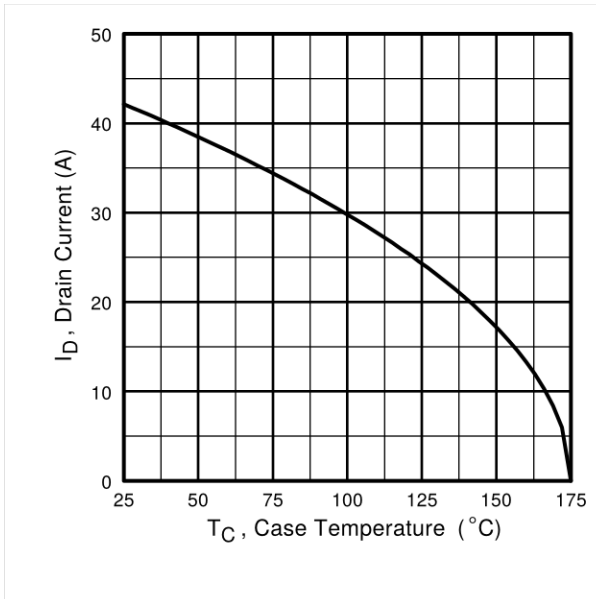


Fig 9. Maximum Drain Current Vs. Case Temperature

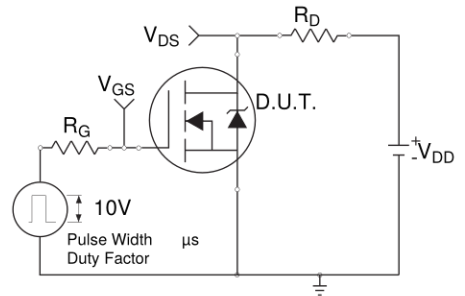


Fig 10a. Switching Time Test Circuit

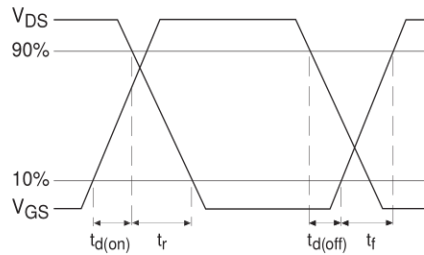


Fig 10b. Switching Time Waveforms

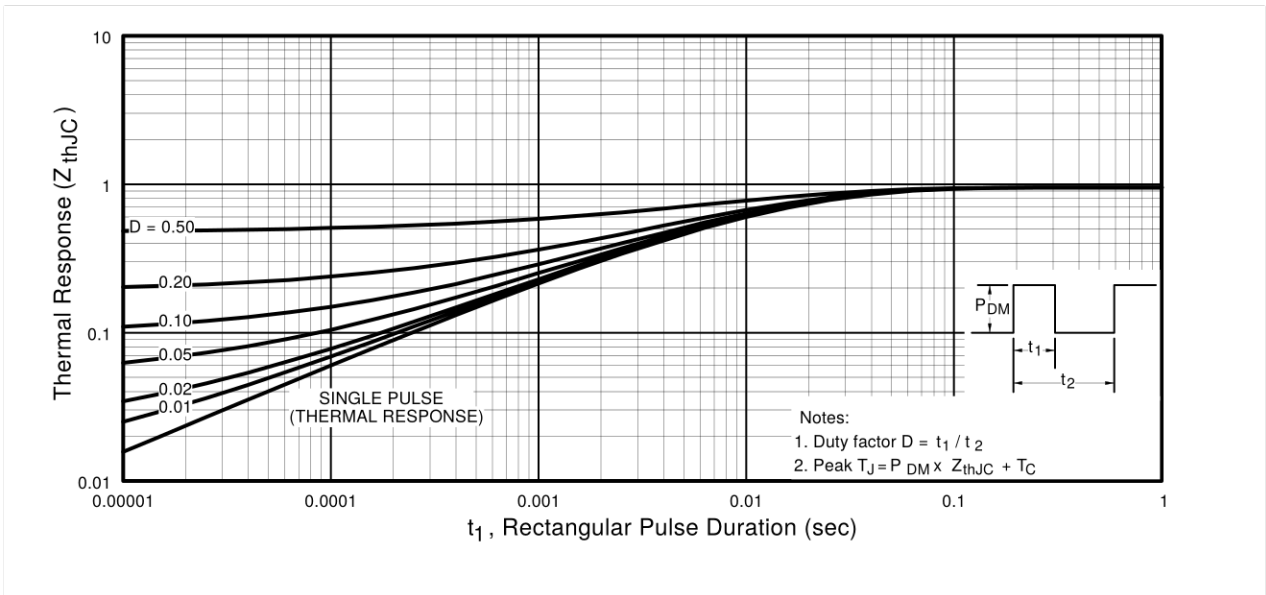


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

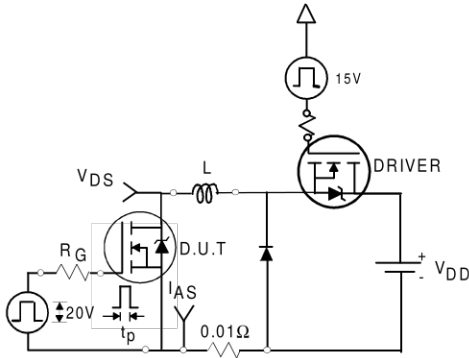


Fig 12a. Unclamped Inductive Test Circuit

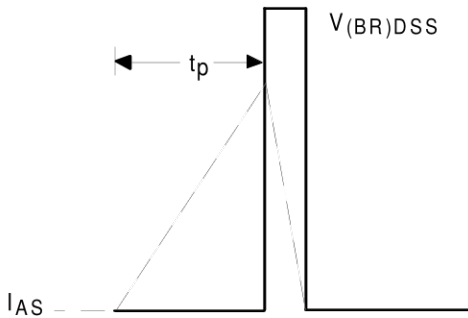


Fig 12b. Unclamped Inductive Waveforms

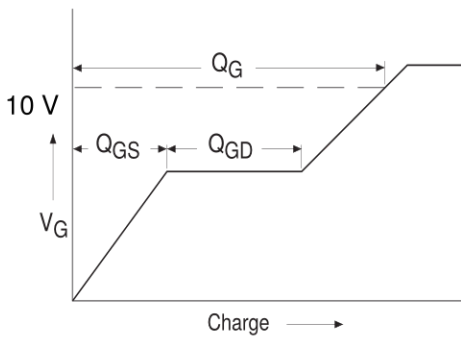


Fig 13a. Basic Gate Charge Waveform

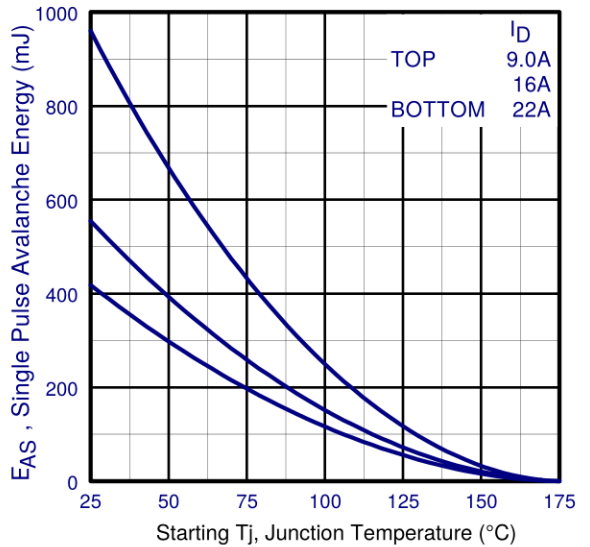


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

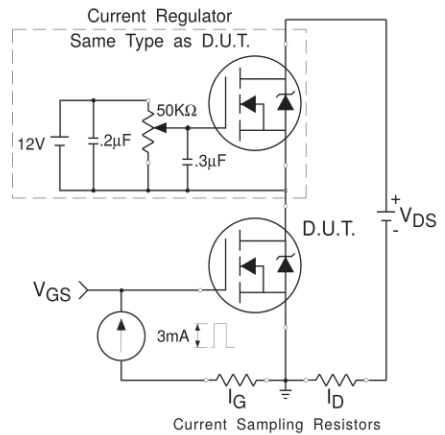
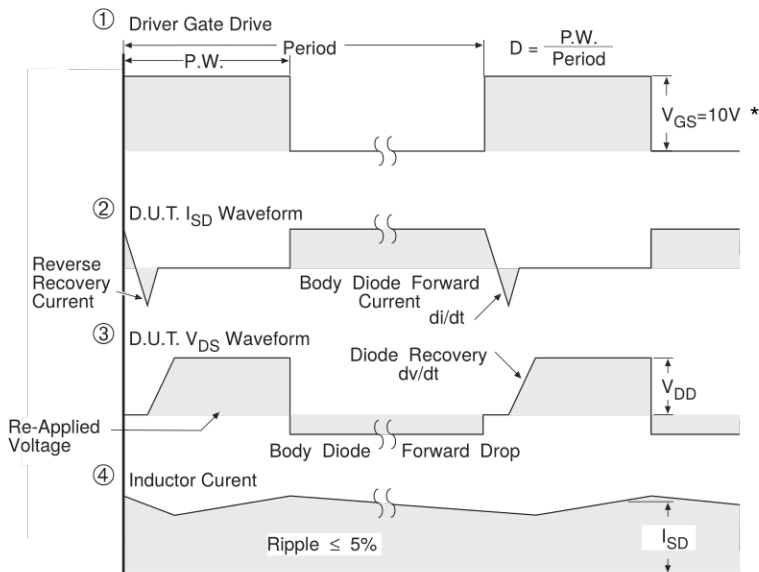
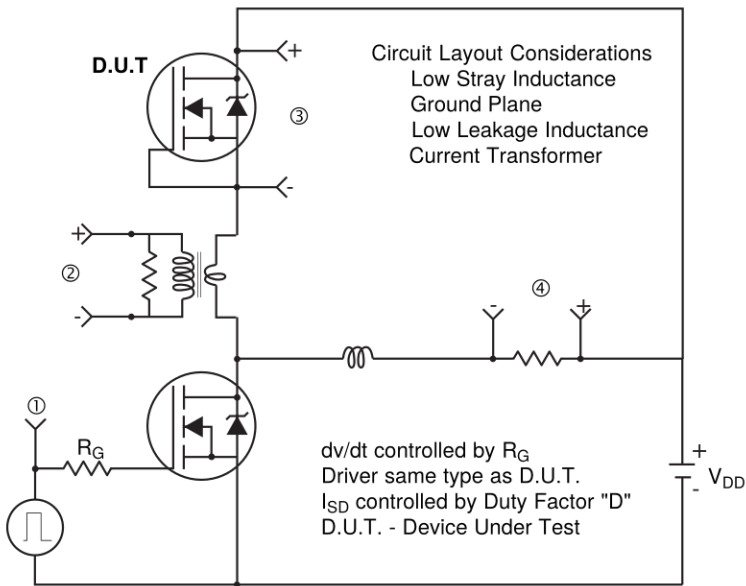


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFETS

Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>