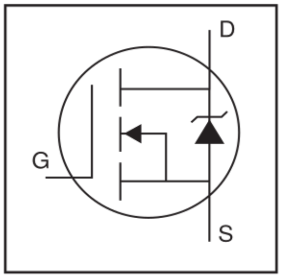
PD-91277A

International
IOR Rectifier

IRFZ46N

HEXFET® Power MOSFET

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated



V_{DSS} = 55V

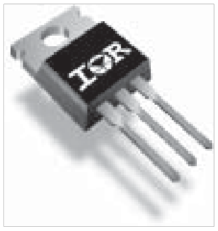
$R_{DS(on)}$ = 16.5mΩ

I_D = 53A⑦

Description

Advanced HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



TO-220AB

Absolute Maximum Ratings

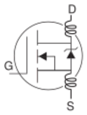
	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	53⑦	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	37	
I_{DM}	Pulsed Drain Current ①	180	
P_D @T_C = 25°C	Power Dissipation	107	W
	Linear Derating Factor	0.71	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
I_{AR}	Avalanche Current①	28	A
E_{AR}	Repetitive Avalanche Energy①	11	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 srew	10 lbf•in (1.1N•m)	

Thermal Resistance

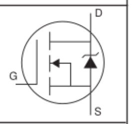
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	1.4	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	——	
$R_{\theta JA}$	Junction-to-Ambient	——	62	

07/15/02

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	——	——	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.057	——	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	——	16.5	mΩ	V_{GS} = 10V, I_D = 28A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
g_{fs}	Forward Transconductance	19	——	——	S	V_{DS} = 25V, I_D = 28A④
I_{DSS}	Drain-to-Source Leakage Current	——	——	25	μA	V_{DS} = 55V, V_{GS} = 0V
		——	——	250		V_{DS} = 44V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -20V
Q_g	Total Gate Charge	——	——	72	nC	I_D = 28A
Q_{gs}	Gate-to-Source Charge	——	——	11		V_{DS} = 44V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	——	26		V_{GS} = 10V, See Fig. 6 and 13
$t_{d(on)}$	Turn-On Delay Time	——	14	——	ns	V_{DD} = 28V
t_r	Rise Time	——	76	——		I_D = 28A
$t_{d(off)}$	Turn-Off Delay Time	——	52	——		R_G = 12Ω
t_f	Fall Time	——	57	——		V_{GS} = 10V, See Fig. 10 ④
L_D	Internal Drain Inductance	——	4.5	——	nH	Between lead, 6mm (0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	——	7.5	——		
C_{iss}	Input Capacitance	——	1696	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	407	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	110	——		ƒ = 1.0MHz, See Fig. 5
E_{AS}	Single Pulse Avalanche Energy②	——	583⑤	152⑥	mJ	I_{AS} = 28A, L = 389μH

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	53	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode)①	——	——	180		
V_{SD}	Diode Forward Voltage	——	——	1.3	V	T_J = 25°C, I_S = 28A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	——	67	101	ns	T_J = 25°C, I_F = 28A
Q_{rr}	Reverse Recovery Charge	——	208	312	nC	di/dt = 100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).

② Starting T_J = 25°C, L = 389μH R_G = 25Ω, I_{AS} = 28A. (See Figure 12).

③ $I_{SD} \leq 28A$, di/dt ≤220A/μs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175°C$.

④ Pulse width ≤400μs; duty cycle ≤2%.

⑤ This is a typical value at device destruction and represents operation outside rated limits.

⑥ This is a calculated value limited to T_J = 175°C.

⑦ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 39A.

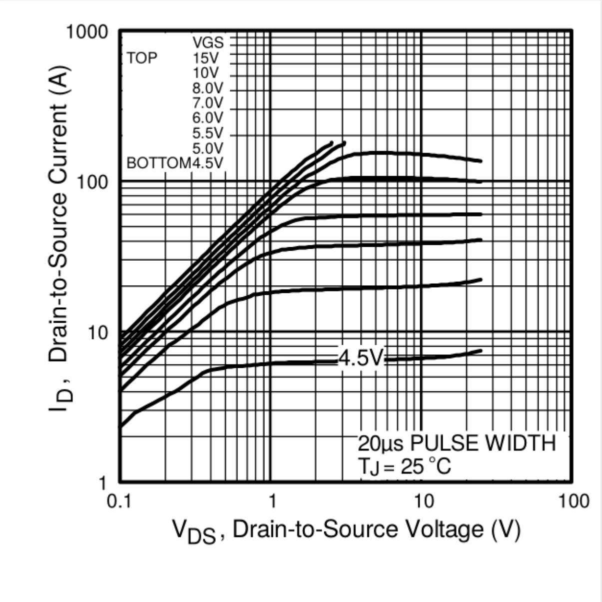


Fig 1. Typical Output Characteristics

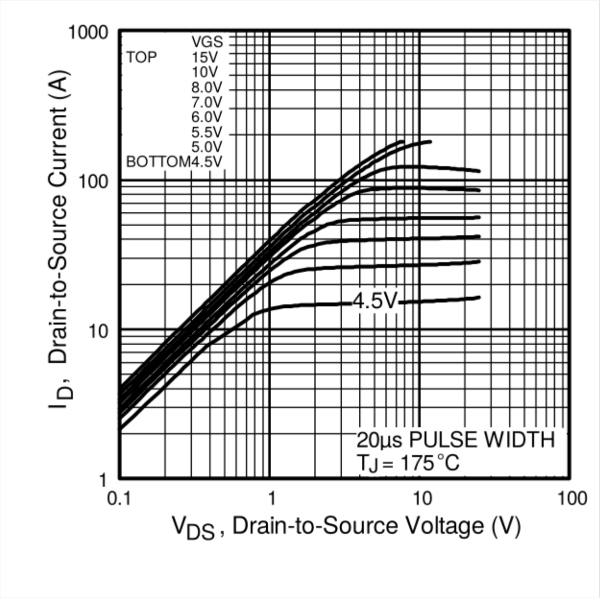


Fig 2. Typical Output Characteristics

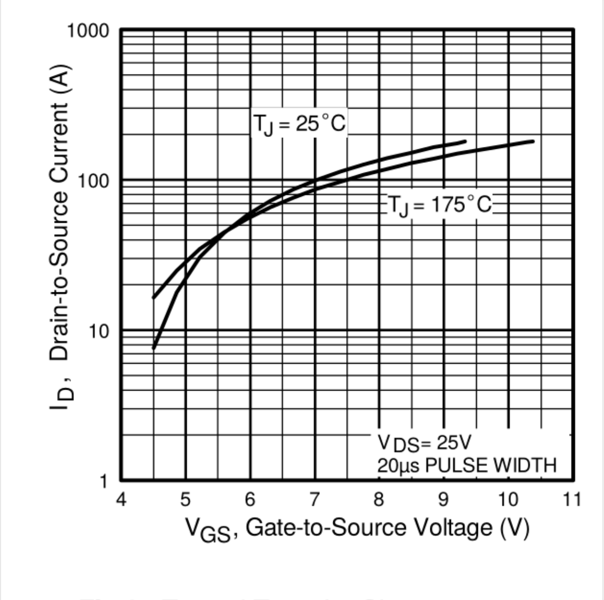


Fig 3. Typical Transfer Characteristics

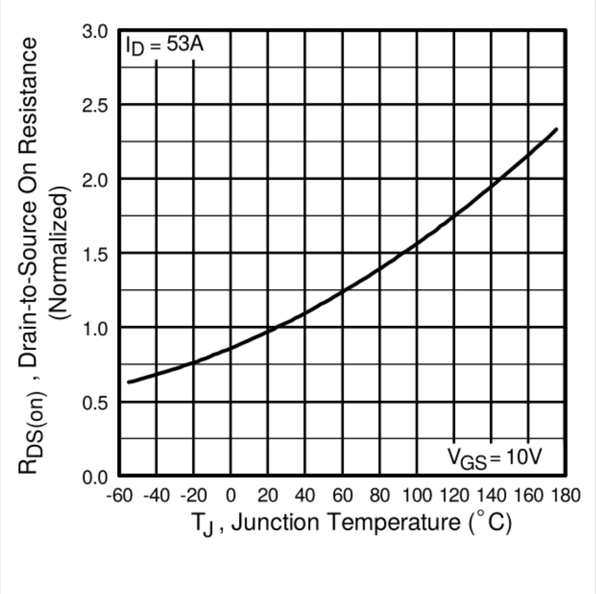


Fig 4. Normalized On-Resistance
Vs. Temperature

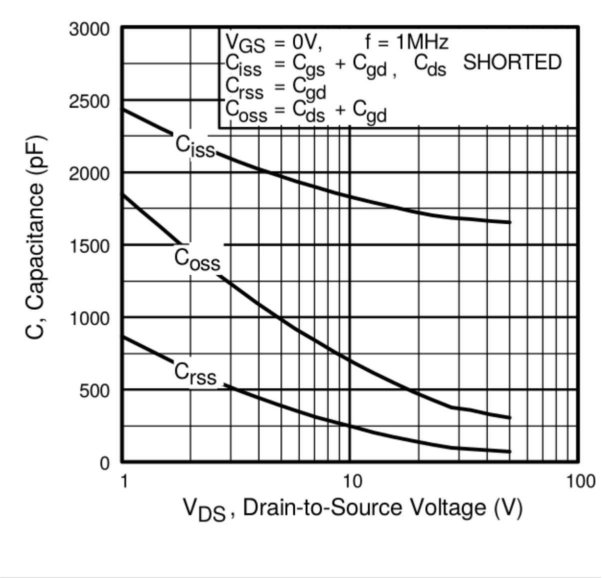


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

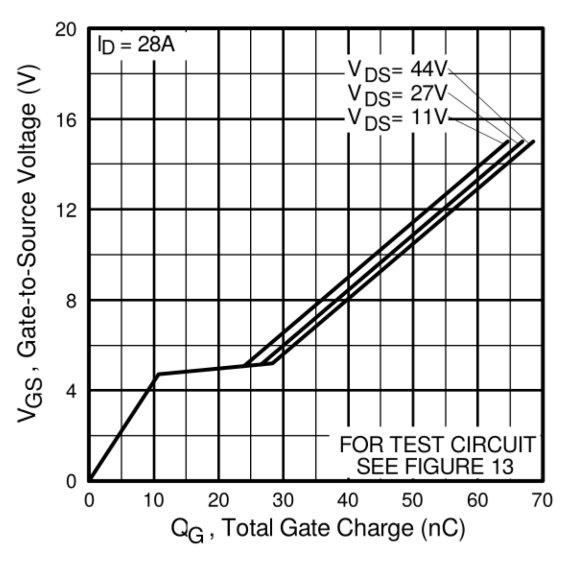


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

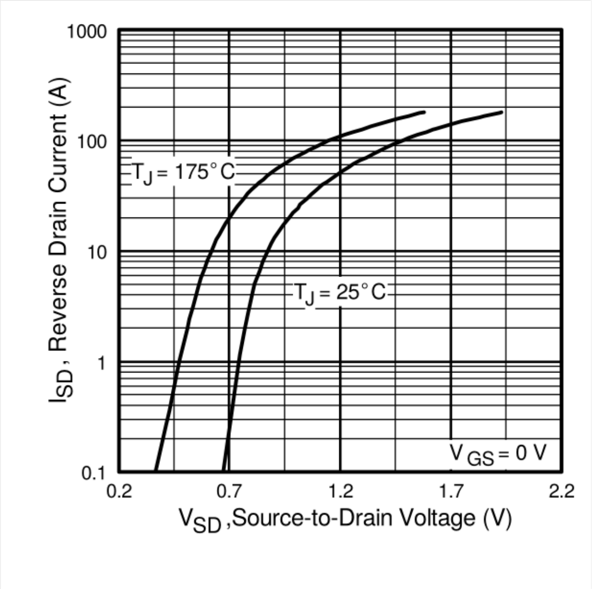


Fig 7. Typical Source-Drain Diode Forward Voltage

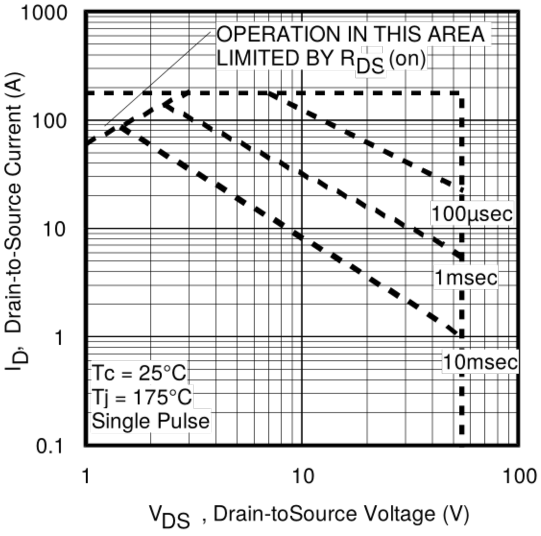


Fig 8. Maximum Safe Operating Area

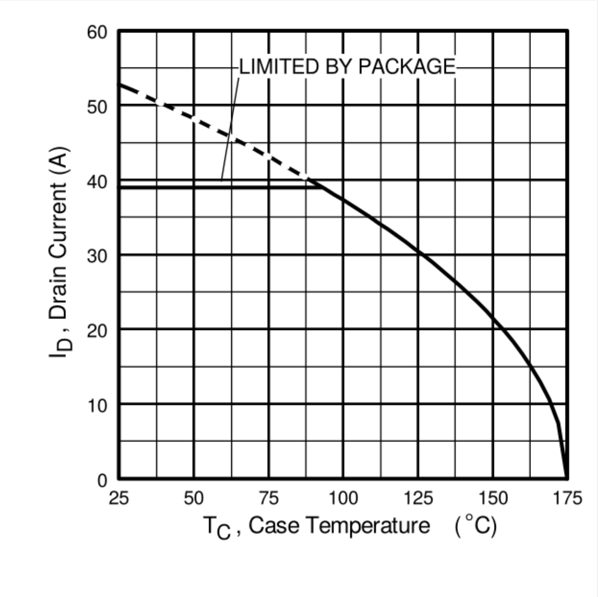


Fig 9. Maximum Drain Current Vs. Case Temperature

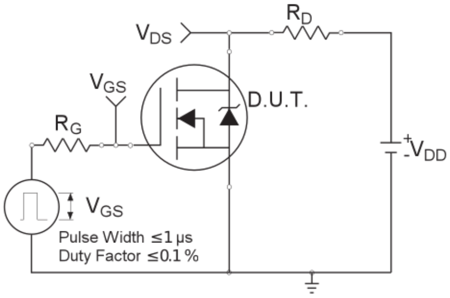


Fig 10a. Switching Time Test Circuit

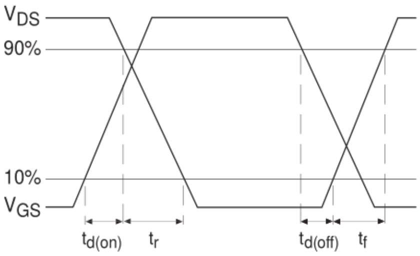


Fig 10b. Switching Time Waveforms

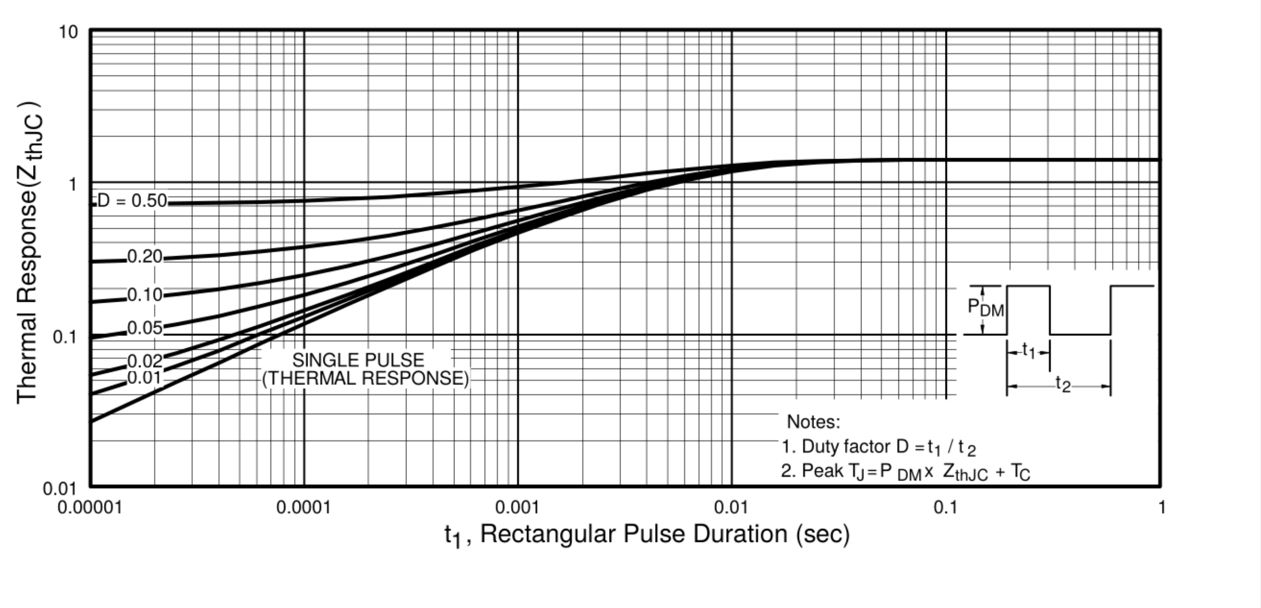


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

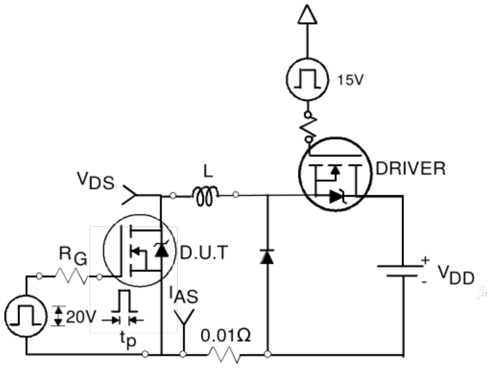


Fig 12a. Unclamped Inductive Test Circuit

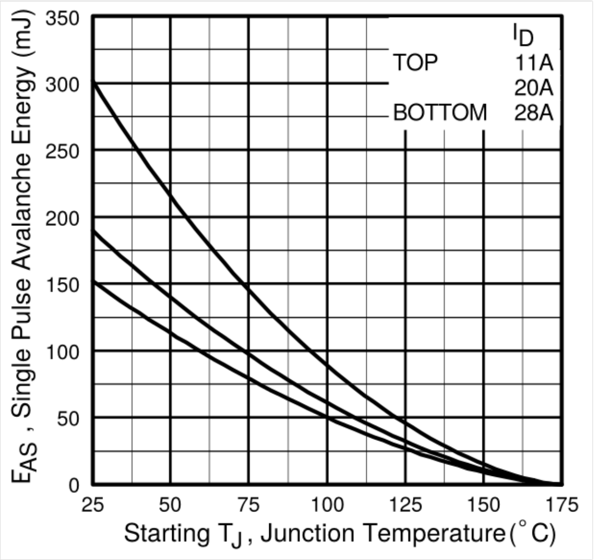


Fig 12c. Maximum Avalanche Energy
Vs. Drain Current

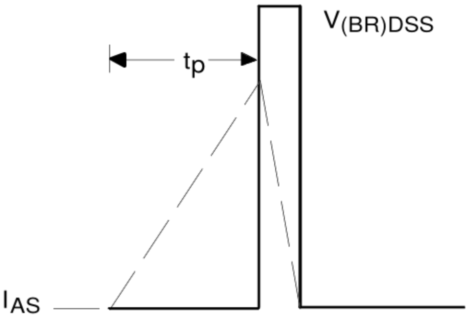


Fig 12b. Unclamped Inductive Waveforms

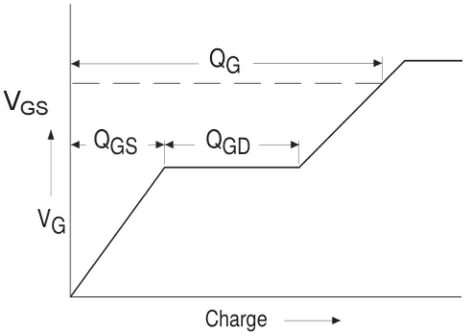


Fig 13a. Basic Gate Charge Waveform

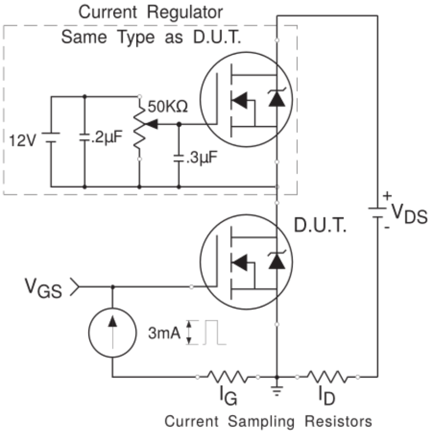
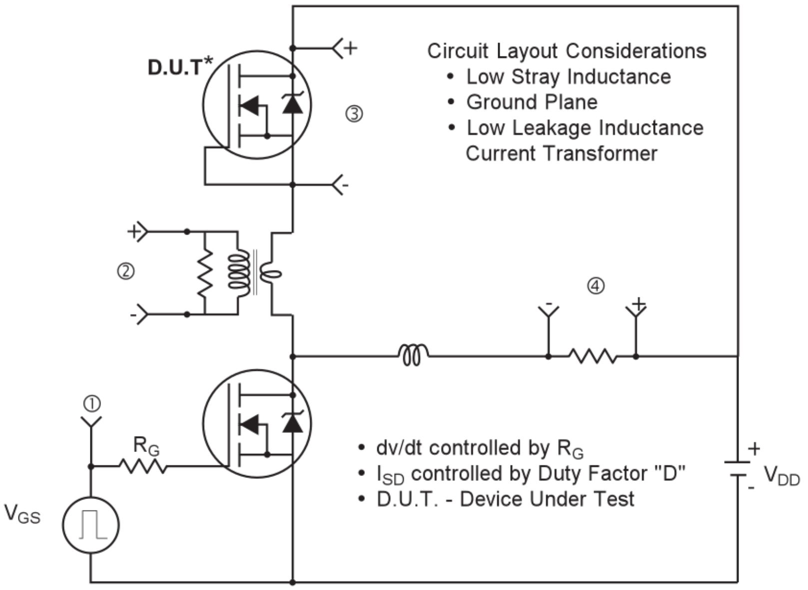


Fig 13b. Gate Charge Test Circuit

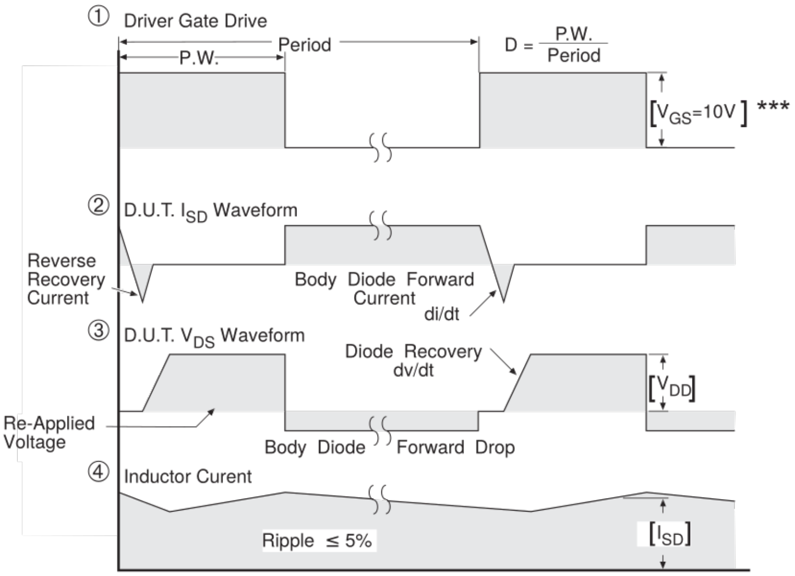
Peak Diode Recovery dv/dt Test Circuit



Circuit Layout Considerations
- Low Stray Inductance
- Ground Plane
- Low Leakage Inductance Current Transformer

- dv/dt controlled by R_G
- I_{SD} controlled by Duty Factor "D"
- D.U.T. - Device Under Test

* Reverse Polarity of D.U.T for P-Channel

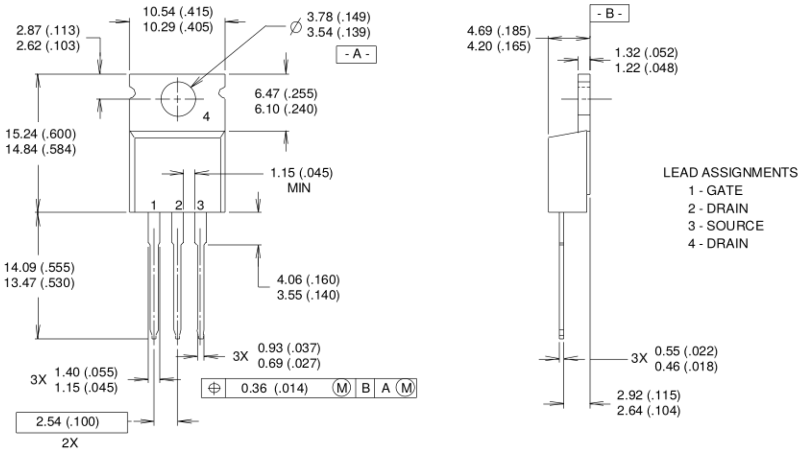


*** V_{GS} = 5.0V for Logic Level and 3V Drive Devices

Fig 14. For N-channel HEXFET® power MOSFETs

TO-220AB Package Outline

Dimensions are shown in millimeters (inches)

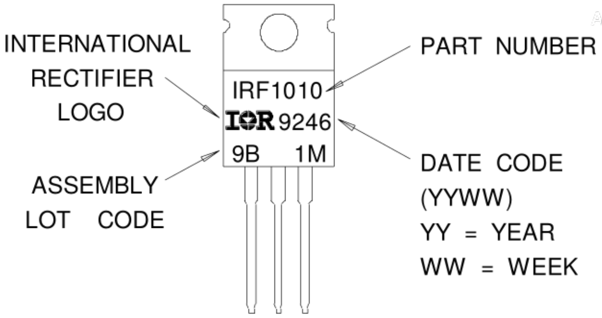


LEAD ASSIGNMENTS
- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE
- 4 - DRAIN

NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION : INCH
3. OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
4. HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

EXAMPLE : THIS IS AN IRF1010
WITH ASSEMBLY
LOT CODE 9B1M



Data and specifications subject to change without notice.
This product has been designed and qualified for the automotive [Q101] market.
Qualification Standards can be found on IR's Web site.

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IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
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Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/