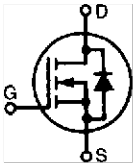
HiPerFET™ Power MOSFETs ISOPLUS247™

(Electrically Isolated Back Surface)

	V_{DSS}	I_{D25}	$R_{DS(on)}$
IXFR 50N50	500 V	43 A	100 mΩ
IXFR 55N50	500 V	48 A	90 mΩ

$t_{rr} \leq 250$ ns

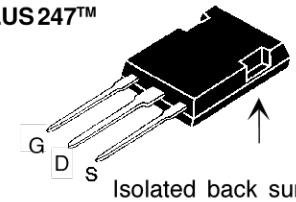
Single Die MOSFET



Symbol	Test Conditions		Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C		500	V
V_{DGR}	T_J = 25°C to 150°C; R_{GS} = 1 MΩ		500	V
V_{GS}	Continuous		±20	V
V_{GSM}	Transient		±30	V
I_{D25}	T_C = 25°C	50N50	43	A
		55N50	48	A
I_{DM}	T_C = 25°C, Pulse width limited by T_{JM}	50N50	200	A
		55N50	220	A
I_{AR}	T_C = 25°C	50N50	50	A
		55N50	55	A
E_{AR}	T_C = 25°C		60	mJ
E_{AS}	T_C = 25°C		3	J
dv/dt	$I_S \leq I_{DM}$, di/dt ≤100 A/µs, $V_{DD} \leq V_{DSS}$ $T_J \leq$150°C, R_G = 2 Ω		5	V/ns
P_D	T_C = 25°C		400	W
T_J			-40 ... +150	°C
T_{JM}			150	°C
T_{stg}			-40 ... +150	°C
T_L	1.6 mm (0.063 in.) from case for 10 s		300	°C
V_{ISOL}	50/60 Hz, RMS t = 1 min		2500	V~
Weight			5	g

Symbol	Test Conditions		Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.
V_{DSS}	V_{GS} = 0 V, I_D = 1mA		500		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 8mA		2.5		4.5 V
I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0				±200 nA
I_{DSS}	$V_{DS} = V_{DSS}$	T_J = 25°C			25 µA
	V_{GS} = 0 V	T_J = 125°C			2 mA
$R_{DS(on)}$	V_{GS} = 10 V, $I_D = I_T$	50N50			100 mΩ
	Note 1	55N50			90 mΩ

ISOPLUS 247™



Isolated back surface*

G = Gate D = Drain
S = Source

* Patent pending

Features

- Silicon chip on Direct-Copper-Bond substrate
  - High power dissipation
  - Isolated mounting surface
  - 2500V electrical isolation
- Low drain to tab capacitance(<50pF)
- Low $R_{DS\ (on)}$ HDMOS™ process
- Rugged polysilicon gate cell structure
- Unclamped Inductive Switching (UIS) rated
- Fast intrinsic Rectifier

Applications

- DC-DC converters
- Battery chargers
- Switched-mode and resonant-mode power supplies
- DC choppers
- AC motor control

Advantages

- Easy assembly
- Space savings
- High power density

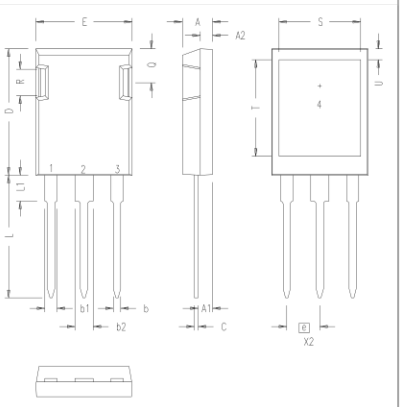
Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
g_{fs}	V_{DS} = 10 V; $I_D = I_T$ Note 1		45		S
C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		9400		pF
C_{oss}			1280		pF
C_{rss}			460		pF
$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 V_{DSS}, $I_D = I_T$ R_G = 1 Ω (External),		45		ns
t_r			60		ns
$t_{d(off)}$			120		ns
t_f			45		ns
$Q_{g(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 V_{DSS}, $I_D = I_T$		330		nC
Q_{gs}			55		nC
Q_{gd}			155		nC
R_{thJC}				0.30	K/W
R_{thCK}			0.15		K/W

Source-Drain Diode

Symbol	Test Conditions		Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
I_S	V_{GS} = 0 V	55N50			55	A
		50N50			50	A
I_{SM}	Repetitive; pulse width limited by T_{JM}	55N50			220	A
		50N50			200	A
V_{SD}	$I_F = I_S$, V_{GS} = 0 V				1.5	V
t_{rr}	I_F = 25A,-di/dt = 100 A/µs, V_R = 100 V				250	ns
Q_{RM}				1.0		µC
I_{RM}				10		A

Note: 1. Pulse test, t ≤300 µs, duty cycle d ≤2 %
2. I_T test current: 50N50 I_T = 25A
55N50 I_T = 27.5A

ISOPLUS 247 OUTLINE



SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b1	.075	.084	1.91	2.13
b2	.115	.123	2.92	3.12
C	.024	.031	0.61	0.80
D	.819	.840	20.80	21.34
E	.620	.635	15.75	16.13
e	.215 BSC		5.45 BSC	
L	.780	.800	19.81	20.32
L1	.150	.170	3.81	4.32
Q	.220	.244	5.59	6.20
R	.170	.190	4.32	4.83
S	.520	.540	13.21	13.72
T	.620	.640	15.75	16.26
U	.065	.080	1.65	2.03

1 – GATE
2 – DRAIN (COLLECTOR)
3 – SOURCE (EMITTER)
4 – NO CONNECTION

NOTE: This drawing will meet all dimensions requirement of JEDEC outline TO-247AD except screw hole.

See IXFK55N50 data sheet for characteristic curves.