MIC4420/9

6A Peak Low-Side MOSFET Driver Bipolar/CMOS/DMOS Process

Features

- CMOS Construction
- Latch-Up Protected: Will Withstand >500 mA Reverse Output Current
- Logic Input Withstands Negative Swing of Up to 5V
- Matched Rise and Fall Times: 25 ns
- High Peak Output Current: 6A Peak
- Wide Operating Range: 4.5V to 18V
- High Capacitive Load Drive: 10,000 pF
- Low Delay Time: 55 ns (typ.)
- Logic High Input for Any Voltage from 2.4V to V_S
- Low Equivalent Input Capacitance: 6 pF (typ.)
- Low Supply Current: 450 µA with Logic 1 Input
- Low Output Impedance: 2.5Ω
- Output Voltage Swing within 25 mV of Ground or V_S

Applications

- Switch Mode Power Supplies
- Motor Controls
- Pulse Transformer Driver
- Class-D Switching Amplifiers

General Description

MIC4420 and MIC4429 MOSFET drivers are tough, efficient, and easy to use. The MIC4429 is an inverting driver, while the MIC4420 is a non-inverting driver.

They are capable of 6A (peak) output and can drive the largest MOSFETs with an improved safe operating margin. The MIC4420/4429 accepts any logic input from 2.4V to V_S without external speed-up capacitors or resistor networks. Proprietary circuits allow the input to swing negative by as much as 5V without damaging the part. Additional circuits protect against damage from electrostatic discharge.

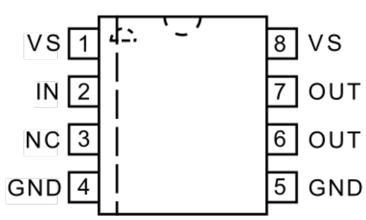
MIC4420/4429 drivers can replace three or more discrete components, reducing PCB area requirements, simplifying product design, and reducing assembly cost.

Modern BiCMOS/DMOS construction guarantees freedom from latch-up. The rail-to-rail swing capability insures adequate gate voltage to the MOSFET during power-up/down sequencing.

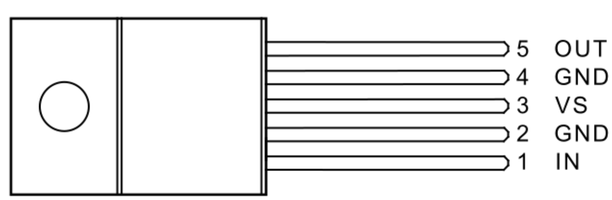
Note: See MIC4120/4129 for high power and narrow pulse applications.

Package Types

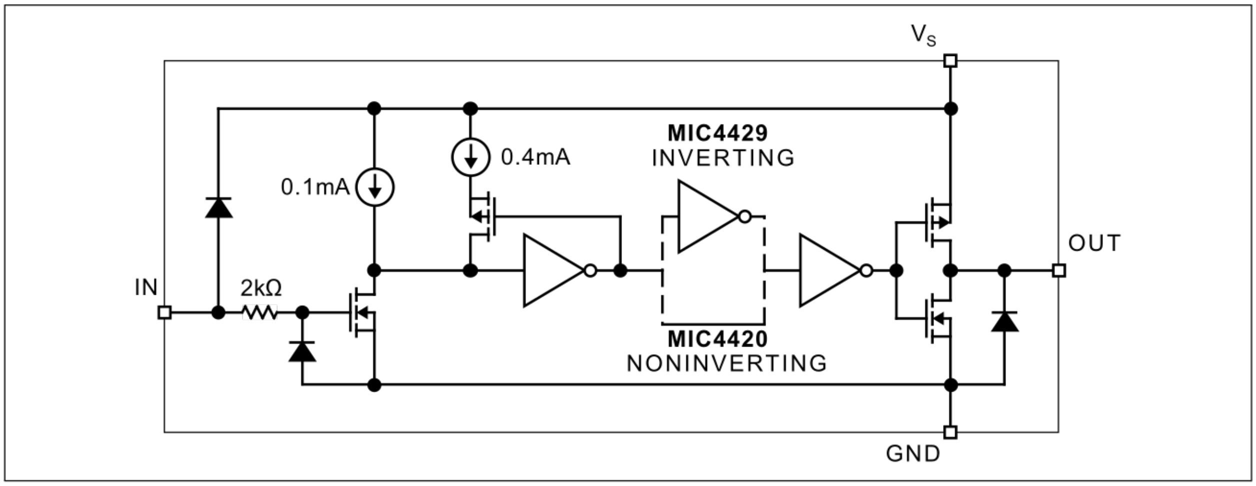
MIC4420/9
8-Lead PDIP (N)
8-Lead SOIC (M)
8-Lead MSOP (MM)



MIC4420/9
5-Lead TO-220 (T)



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage .... +20V
Input Voltage .... V_S + 0.3V to GND – 5.0V
Input Current ($V_{IN} > V_S$) .... 50 mA
Power Dissipation ($T_A \le 25°C$)
PDIP .... 960 mW
SOIC .... 1040 mW
5-Lead TO-220 .... 2W
Power Dissipation ($T_C \le 25°C$)
5-Lead TO-220 .... 12.5W
Derating Factors (to Ambient)
PDIP .... 7.7 mW/°C
SOIC .... 8.3 mW/°C
5-Lead TO-220 .... 17 mW/°C

Operating Ratings ‡

Supply Voltage .... +4.5V to +18V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: T_A = +25°C with 4.5V ≤ V_S ≤ 18V, unless otherwise specified. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
INPUT						
Logic 1 Input Voltage	V_{IH}	2.4	1.4	—	V	—
Logic 0 Input Voltage	V_{IL}	—	1.1	0.8	V	—
Input Voltage Range	V_{IN}	–5	—	V_S + 0.3	V	—
Input Current	I_{IN}	–10	—	10	µA	0V ≤ V_{IN} ≤ V_S
OUTPUT						
Output High Voltage	V_{OH}	V_S – 0.025	—	—	V	See Figure 1-1
Output Low Voltage	V_{OL}	—	—	0.025	V	See Figure 1-1
Output Resistance, Output Low	R_{OL}	—	1.7	2.8	Ω	I_{OUT} = 10 mA, V_S = 18V
Output Resistance, Output High	R_{OH}	—	1.5	2.5	Ω	I_{OUT} = 10 mA, V_S = 18V
Peak Output Current	I_{PK}	—	6	—	A	V_S = 18V (See Figure 4-3)
Latch-Up Protection Withstand Reverse Current	I_R	>500	—	—	mA	—
SWITCHING TIME (Note 2)						
Rise Time	t_R	—	12	35	ns	Figure 1-1, C_L = 2500 pF
Fall Time	t_F	—	13	35	ns	Figure 1-1, C_L = 2500 pF
Delay Time 1	t_{D1}	—	18	75	ns	Figure 1-1
Delay Time 2	t_{D2}	—	48	75	ns	Figure 1-1

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: T_A = +25°C with 4.5V ≤ V_S ≤ 18V, unless otherwise specified. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
POWER SUPPLY						
Power Supply Current	I_S	—	0.45	1.5	mA	V_{IN} = 3V
		—	90	150	µA	V_{IN} = 0V
Operating Input Voltage	V_S	4.5	—	18	V	—

Note 1: Specification for packaged product only.

2: Switching times guaranteed by design.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: T_A = –40°C to +85°C with 4.5V ≤ V_S ≤ 18V, unless otherwise specified. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
INPUT						
Logic 1 Input Voltage	V_{IH}	2.4	—	—	V	—
Logic 0 Input Voltage	V_{IL}	—	—	0.8	V	—
Input Voltage Range	V_{IN}	–5	—	V_S + 0.3	V	—
Input Current	I_{IN}	–10	—	10	µA	0V ≤ V_{IN} ≤ V_S
OUTPUT						
Output High Voltage	V_{OH}	V_S – 0.025	—	—	V	See Figure 1-1
Output Low Voltage	V_{OL}	—	—	0.025	V	See Figure 1-1
Output Resistance, Output Low	R_{OL}	—	3	5	Ω	I_{OUT} = 10 mA, V_S = 18V
Output Resistance, Output High	R_{OH}	—	2.3	5	Ω	I_{OUT} = 10 mA, V_S = 18V
SWITCHING TIME (Note 2)						
Rise Time	t_R	—	32	60	ns	Figure 1-1, C_L = 2500 pF
Fall Time	t_F	—	34	60	ns	Figure 1-1, C_L = 2500 pF
Delay Time 1	t_{D1}	—	50	100	ns	Figure 1-1
Delay Time 2	t_{D2}	—	65	100	ns	Figure 1-1
POWER SUPPLY						
Power Supply Current	I_S	—	0.45	3.0	mA	V_{IN} = 3V
		—	0.06	0.4	µA	V_{IN} = 0V
Operating Input Voltage	V_S	4.5	—	18	V	—

Note 1: Specification for packaged product only.

2: Switching times guaranteed by design.

Test Circuits

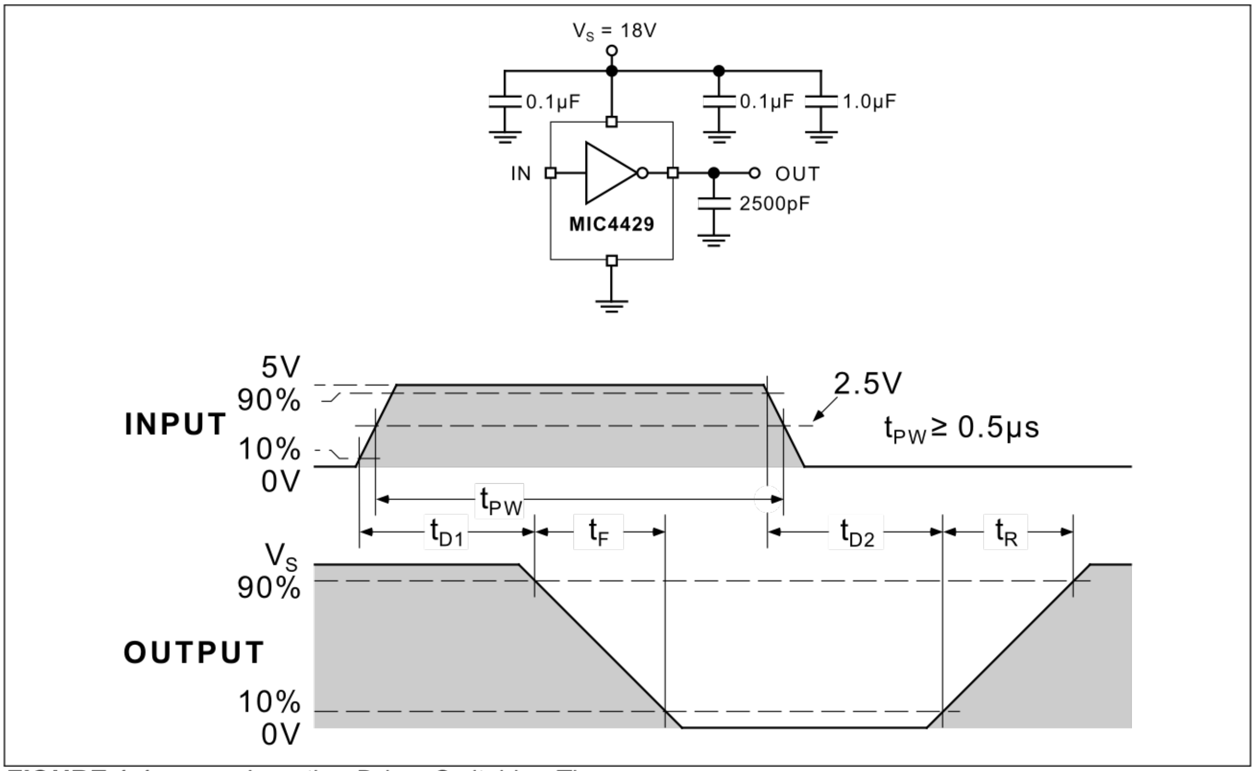


FIGURE 1-1: Inverting Driver Switching Time.

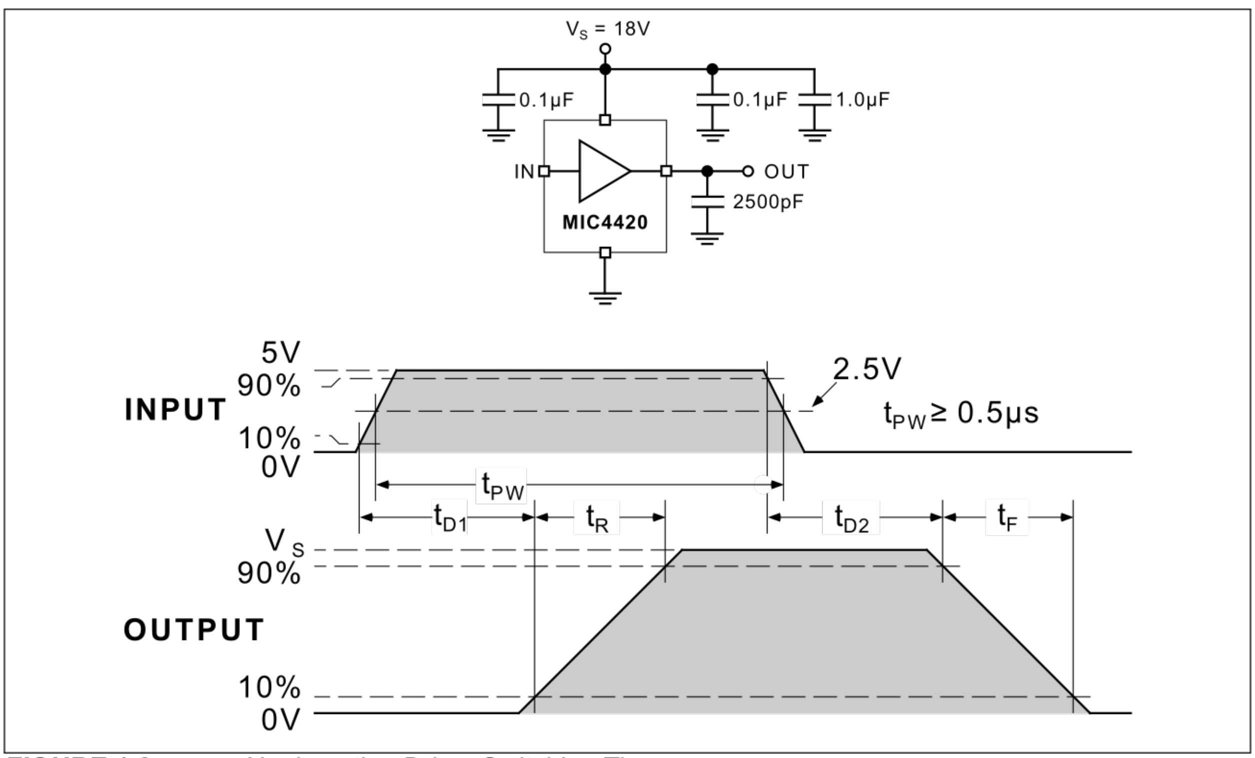


FIGURE 1-2: Noninverting Driver Switching Time.

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Storage Temperature Range	T_S	–65	—	+150	°C	—
Junction Operating Temperature	T_J	—	—	+150	°C	—
Ambient Operating Temperature Range	T_A	–40	—	+85	°C	B Version
		0	—	+70		C Version
Lead Temperature	—	—	—	+300	°C	Soldering, 10s
Package Thermal Resistances						
Thermal Resistance, 8-Lead MSOP	θ_{JA}	—	250	—	°C/W	—
Thermal Resistance, 5-Lead TO-220	θ_{JC}	—	10	—	°C/W	—
Thermal Resistance, 8-Lead PDIP	θ_{JA}	—	125	—	°C/W	—
Thermal Resistance, 8-Lead SOIC	θ_{JA}	—	155	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +150°C rating. Sustained junction temperatures above +150°C can impact the device reliability.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

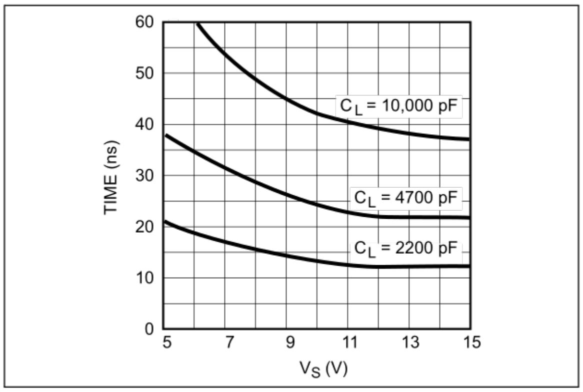


FIGURE 2-1: *Rise Time vs. Supply Voltage.*

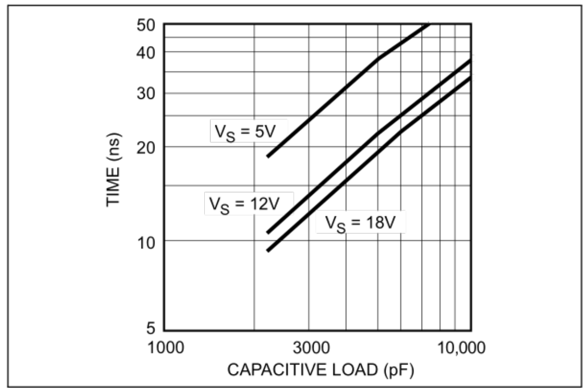


FIGURE 2-4: *Rise Time vs. Capacitive Load.*

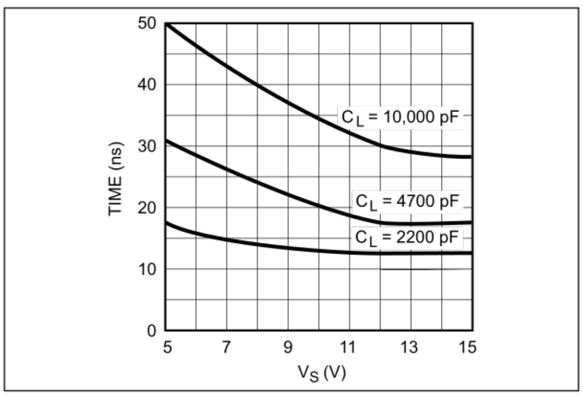


FIGURE 2-2: *Fall Time vs. Supply Voltage.*

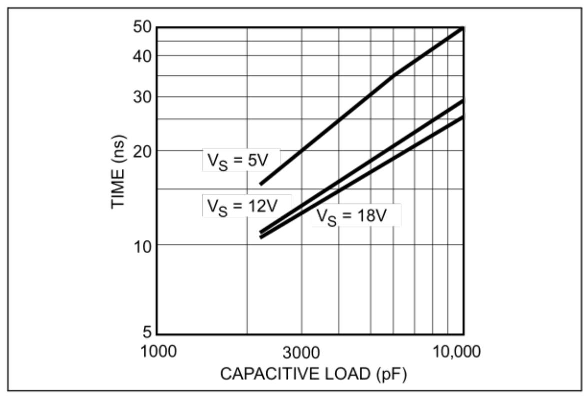


FIGURE 2-5: *Fall Time vs. Capacitive Load.*

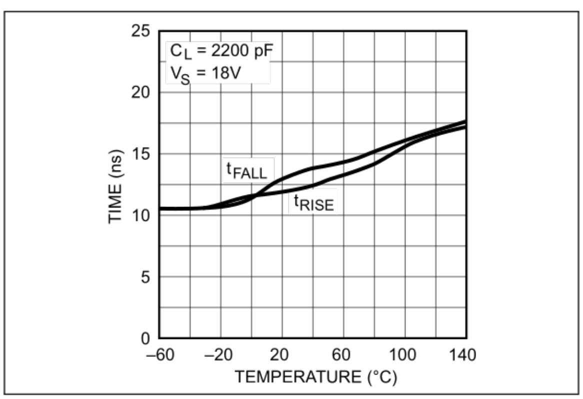


FIGURE 2-3: *Rise and Fall Times vs. Temperature.*

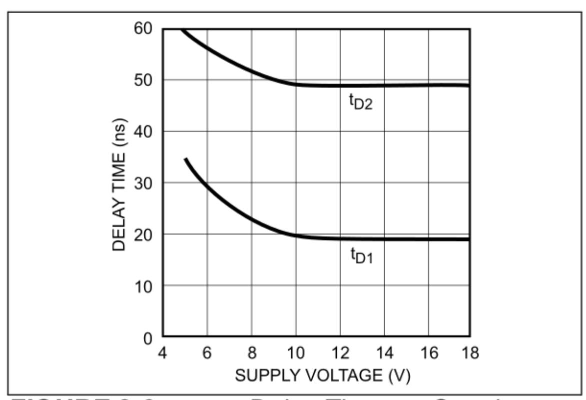


FIGURE 2-6: *Delay Time vs. Supply Voltage.*

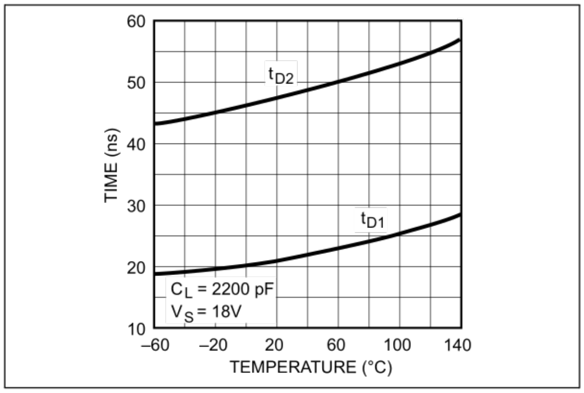


FIGURE 2-7: *Propagation Delay Time vs. Temperature.*

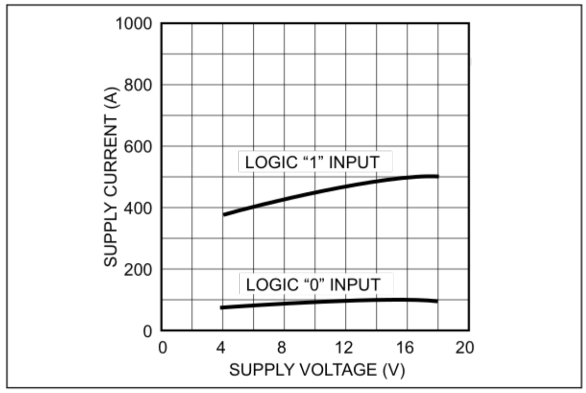


FIGURE 2-10: *Quiescent Power Supply Voltage vs. Supply Current.*

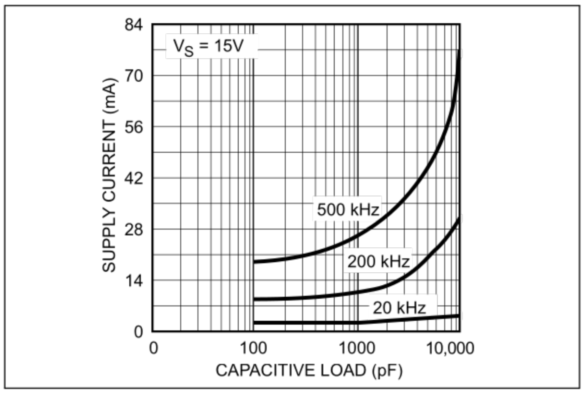


FIGURE 2-8: *Supply Current vs. Capacitive Load.*

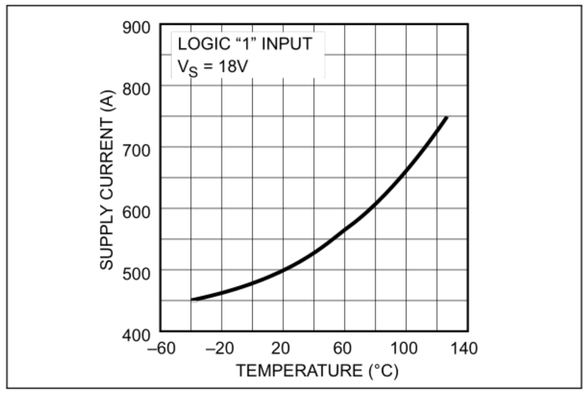


FIGURE 2-11: *Quiescent Power Supply Current vs. Temperature.*

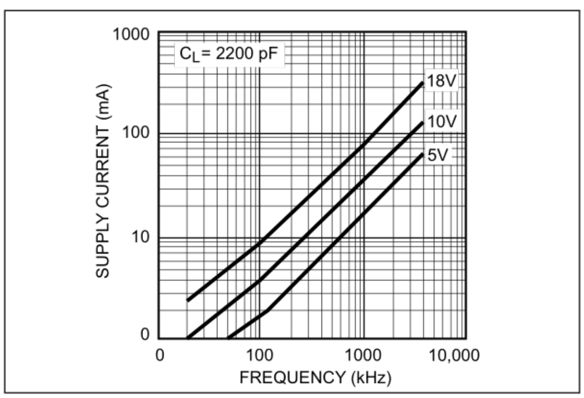


FIGURE 2-9: *Supply Current vs. Frequency.*

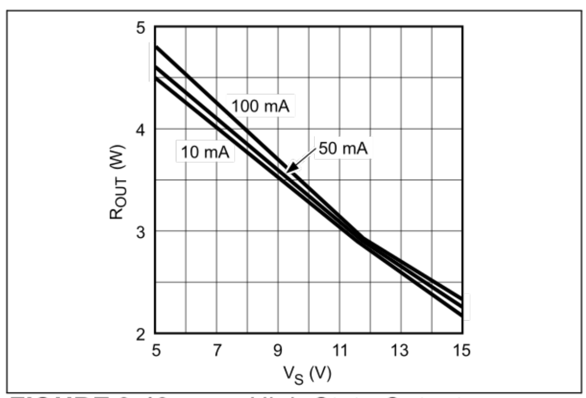


FIGURE 2-12: *High-State Output Resistance.*

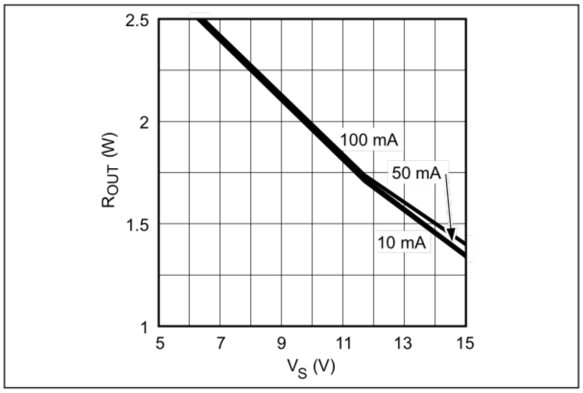


FIGURE 2-13: *Low-State Output Resistance.*

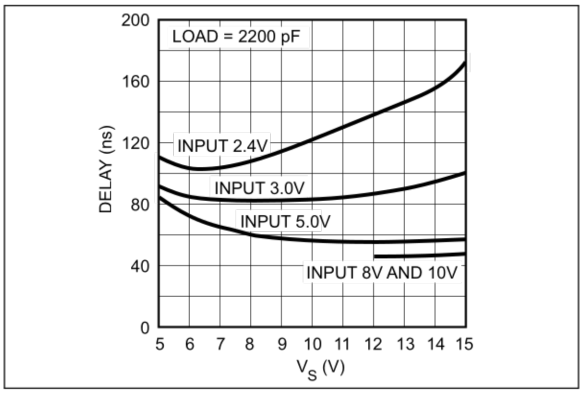


FIGURE 2-14: *Effect of Input Amplitude on Propagation Delay.*

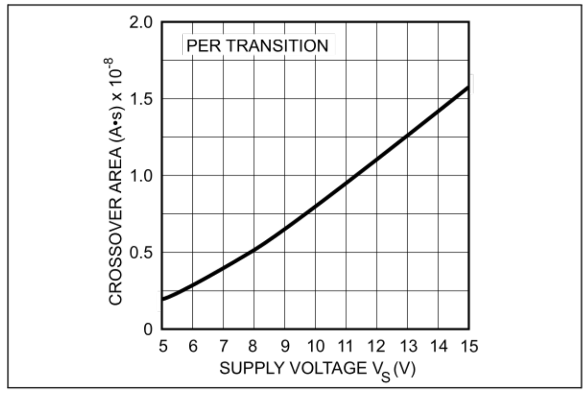


FIGURE 2-15: *Crossover Area vs. Supply Voltage.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number TO-220	Pin Number PDIP, SOIC, MSOP	Pin Name	Description
1	2	IN	Control input.
2, 4	4, 5	GND	Ground: Duplicate pins must be externally connected together.
3, TAB	1, 8	V_S	Supply input: Duplicate pins must be externally connected together.
5	6, 7	OUT	Output: Duplicate pins must be externally connected together.
—	3	NC	Not connected.

4.0 APPLICATION INFORMATION

4.1 Supply Bypassing

Charging and discharging large capacitive loads quickly requires large currents. For example, charging a 2500 pF load to 18V in 25 ns requires a 1.8A current from the device power supply.

The MIC4420/4429 has double bonding on the supply pins, the ground pins and output pins This reduces parasitic lead inductance. Low inductance enables large currents to be switched rapidly. It also reduces internal ringing that can cause voltage breakdown when the driver is operated at or near the maximum rated voltage.

Internal ringing can also cause output oscillation due to feedback. This feedback is added to the input signal because it is referenced to the same ground.

To guarantee low supply impedance over a wide frequency range, a parallel capacitor combination is recommended for supply bypassing. Low inductance ceramic disk capacitors with short lead lengths (less than 0.5 inch) should be used. A 1 µF low ESR film capacitor in parallel with two 0.1 µF low ESR ceramic capacitors, (such as AVX RAM GUARD®), provides adequate bypassing. Connect one ceramic capacitor directly between pins 1 and 4. Connect the second ceramic capacitor directly between pins 8 and 5.

4.2 Grounding

The high current capability of the MIC4420/4429 demands careful PC board layout for best performance Because the MIC4429 is an inverting driver, any ground lead impedance will appear as negative feedback which can degrade switching speed. Feedback is especially noticeable with slow-rise time inputs. The MIC4429 input structure includes 300 mV of hysteresis to ensure clean transitions and freedom from oscillation, but attention to layout is still recommended.

Figure 4-1 shows the feedback effect in detail. As the MIC4429 input begins to go positive, the output goes negative and several amperes of current flow in the ground lead. As little as 0.05Ω of PC trace resistance can produce hundreds of millivolts at the MIC4429 ground pins. If the driving logic is referenced to power ground, the effective logic input level is reduced and oscillation may result.

To ensure optimum performance, separate ground traces should be provided for the logic and power connections. Connecting the logic ground directly to the MIC4429 GND pins will ensure full logic drive to the input and ensure fast output switching. Both of the MIC4429 GND pins should, however, still be connected to power ground.

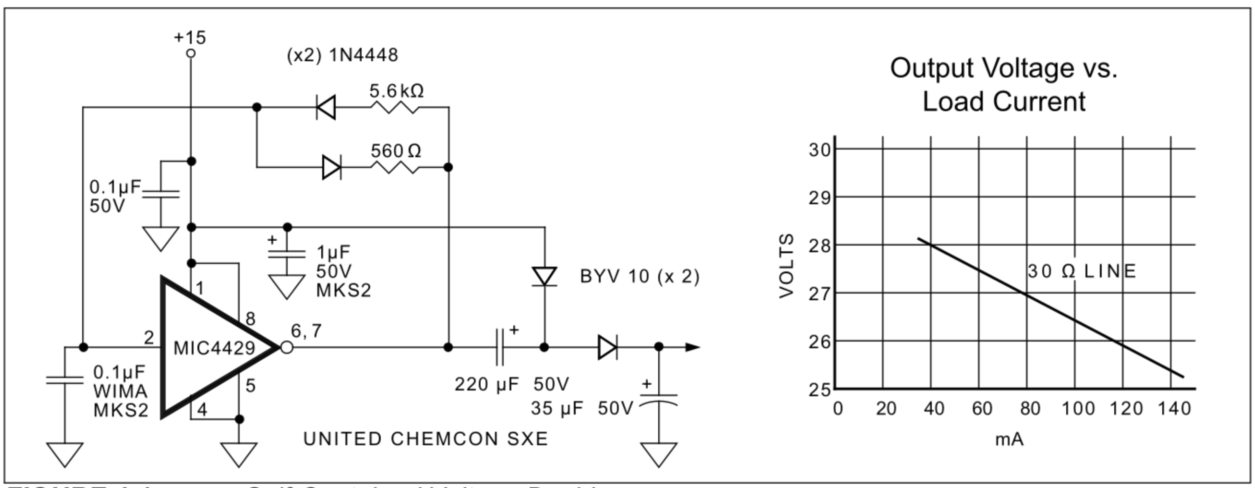


FIGURE 4-1: *Self-Contained Voltage Doubler.*

4.3 Input Stage

The input voltage level of the 4429 changes the quiescent supply current. The N channel MOSFET input stage transistor drives a 450 µA current source load. With a logic "1" input, the maximum quiescent supply current is 450 µA. Logic "0" input level signals reduce quiescent current to 55 µA maximum.

The MIC4420/4429 input is designed to provide 300 mV of hysteresis. This provides clean transitions, reduces noise sensitivity, and minimizes output stage current spiking when changing states. Input voltage threshold level is approximately 1.5V, making the device TTL compatible over the 4.5V to 18V operating supply voltage range. Input current is less than 10 µA over this range.

The MIC4429 can be directly driven by the TL494, SG1526/1527, SG1524, TSC170, MIC38HC42, and similar switch mode power supply integrated circuits. By offloading the power-driving duties to the

MIC4420/4429, the power supply controller can operate at lower dissipation. This can improve performance and reliability.

The input can be greater than the $+V_S$ supply, however, current will flow into the input lead. The propagation delay for t_{D2} will increase to as much as 400 ns at room temperature. The input currents can be as high as 30 mA peak-to-peak (6.4 mA_{RMS}) with the input, 6 V greater than the supply voltage. No damage will occur to MIC4420/4429 however, and it will not latch.

The input appears as a 7 pF capacitance, and does not change even if the input is driven from an AC source. Care should be taken so that the input does not go more than 5 volts below the negative rail.

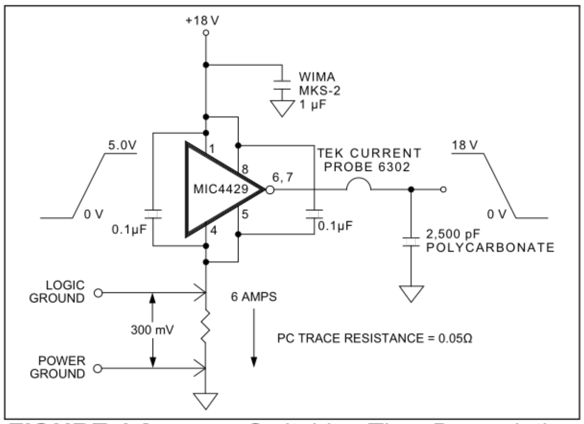


FIGURE 4-2: *Switching Time Degradation Due to Negative Feedback.*

4.4 Power Dissipation

CMOS circuits usually permit the user to ignore power dissipation. Logic families such as 4000 and 74C have outputs which can only supply a few milliamperes of current, and even shorting outputs to ground will not force enough current to destroy the device. The MIC4420/4429 on the other hand, can source or sink several amperes and drive large capacitive loads at high frequency. The package power dissipation limit can easily be exceeded. Therefore, some attention should be given to power dissipation when driving low impedance loads and/or operating at high frequency.

The supply current vs. frequency and supply current vs. capacitive load characteristic curves aid in determining power dissipation calculations. Table 4-1 lists the maximum safe operating frequency for several power supply voltages when driving a 2500 pF load. More accurate power dissipation figures can be obtained by summing the three dissipation sources.

Given the power dissipation in the device, and the thermal resistance of the package, junction operating temperature for any ambient is easy to calculate. For example, the thermal resistance of the 8-pin MSOP package, from the data sheet, is 250°C/W. In a 25°C ambient, then, using a maximum junction temperature of 150°C, this package will dissipate 500 mW.

Accurate power dissipation numbers can be obtained by summing the three sources of power dissipation in the device:

- Load power dissipation (P_L)
- Quiescent power dissipation (P_Q)
- Transition power dissipation (P_T)

Calculation of load power dissipation differs depending on whether the load is capacitive, resistive or inductive.

TABLE 4-1: MIC4429 MAX. OPERATING FREQUENCY

V_S	Maximum Frequency
18V	500 kHz
15V	700 kHz
10V	1.6 MHz

Note 1: Conditions: DIP package (θ_{JA} = 130°C/W), T_A = 25°C, C_L = 2500 pF.

4.4.1 RESISTIVE LOAD POWER DISSIPATION

Dissipation caused by a resistive load can be calculated as:

EQUATION 4-1:

$$P_L = I^2 \times R_O \times D$$

Where:

I = The current drawn by the load.

R_O = The output resistance of the driver when the output is high, at the power supply voltage used.

D = Fraction of the time the load is conducting (duty cycle).

4.4.2 CAPACITIVE LOAD DISSIPATION

Dissipation caused by a capacitive load is simply the energy placed in, or removed from, the load capacitance by the driver. The energy stored in a capacitor is described by Equation 4-2:

EQUATION 4-2:

$$E = 1/2C \times V^2$$

As this energy is lost in the driver each time the load is charged or discharged, for power dissipation calculations the 1/2 is removed. This equation also shows that it is good practice not to place more voltage on the capacitor than is necessary, as dissipation increases as the square of the voltage applied to the capacitor. For a driver with a capacitive load:

EQUATION 4-3:

$$P_L = f \times C \times V_S^2$$

Where:

f	= Operating frequency.
C	= Load capacitance.
V_S	= Driver supply voltage.

4.4.3 INDUCTIVE LOAD POWER DISSIPATION

For inductive loads the situation is more complicated. For the part of the cycle in which the driver is actively forcing current into the inductor, the situation is the same as it is in the resistive case:

EQUATION 4-4:

$$P_{L1} = I^2 \times R_O \times D$$

However, in this instance the R_O required may be either the on resistance of the driver when its output is in the high state, or its on resistance when the driver is in the low state, depending on how the inductor is connected, and this is still only half the story. For the part of the cycle when the inductor is forcing current through the driver, dissipation is best described in Equation 4-5 in which V_D is the forward drop of the clamp diode in the driver (generally around 0.7V).

EQUATION 4-5:

$$P_{L2} = I \times V_D \times (1 - D)$$

The two parts of the load dissipation must be summed in to produce P_L.

EQUATION 4-6:

$$P_L = P_{L1} + P_{L2}$$

4.4.4 QUIESCENT POWER DISSIPATION

Quiescent power dissipation (P_Q, as described in the Input Stage section) depends on whether the input is high or low. A low input will result in a maximum current drain (per driver) of ≤0.2 mA; a logic high will result in a current drain of ≤2.0 mA. Quiescent power can therefore be found from:

EQUATION 4-7:

$$P_Q = V_S \times (D \times I_H + (1 - D) \times I_L)$$

Where:

I_H	= Quiescent current with input high.
I_L	= Quiescent current with input low.
D	= Duty cycle.
V_S	= Power supply voltage.

4.4.5 TRANSITION POWER DISSIPATION

Transition power is dissipated in the driver each time its output changes state, because during the transition, for a very brief interval, both the N- and P-channel MOSFETs in the output totem-pole are ON simultaneously, and a current is conducted through them from $+V_S$ to ground. The transition power dissipation is approximately:

EQUATION 4-8:

$$P_T = 2 \times f \times V_S \times (A \bullet s)$$

Where:

A•s = A time-current factor derived from the typical characteristic curves.

Total power dissipation (PD), then, as previously described, is:

EQUATION 4-9:

$$P_D = P_L + P_Q + P_T$$

4.4.6 DEFINITIONS

- C_L = Load Capacitance in Farads.
- D = Duty Cycle expressed as the fraction of time the input to the driver is high.
- f = Operating Frequency of the driver in Hertz.
- I_H = Power supply current drawn by a driver when both inputs are high and neither output is loaded.
- I_L = Power supply current drawn by a driver when both inputs are low and neither output is loaded.
- I_D = Output current from a driver in Amps.
- P_D = Total power dissipated in a driver in Watts.
- P_L = Power dissipated in the driver due to the driver's load in Watts.
- P_Q = Power dissipated in a quiescent driver in Watts.
- PT = Power dissipated in a driver when the output changes states ("shoot-through current") in Watts. Please note that the "shoot-through" current from a dual transition (once up, once down) for both drivers is shown by Figure 2-15 and is in ampere-seconds. This figure must be multiplied by the number of repetitions per second (frequency) to find Watts.
- R_O = Output resistance of a driver in Ohms.
- V_S = Power supply voltage to the IC in Volts.

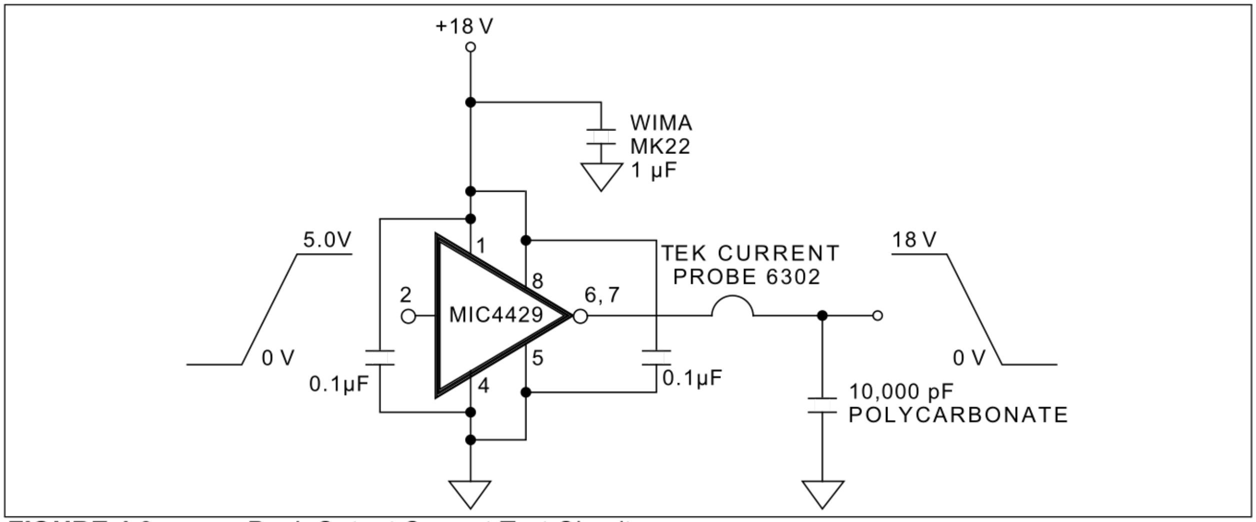
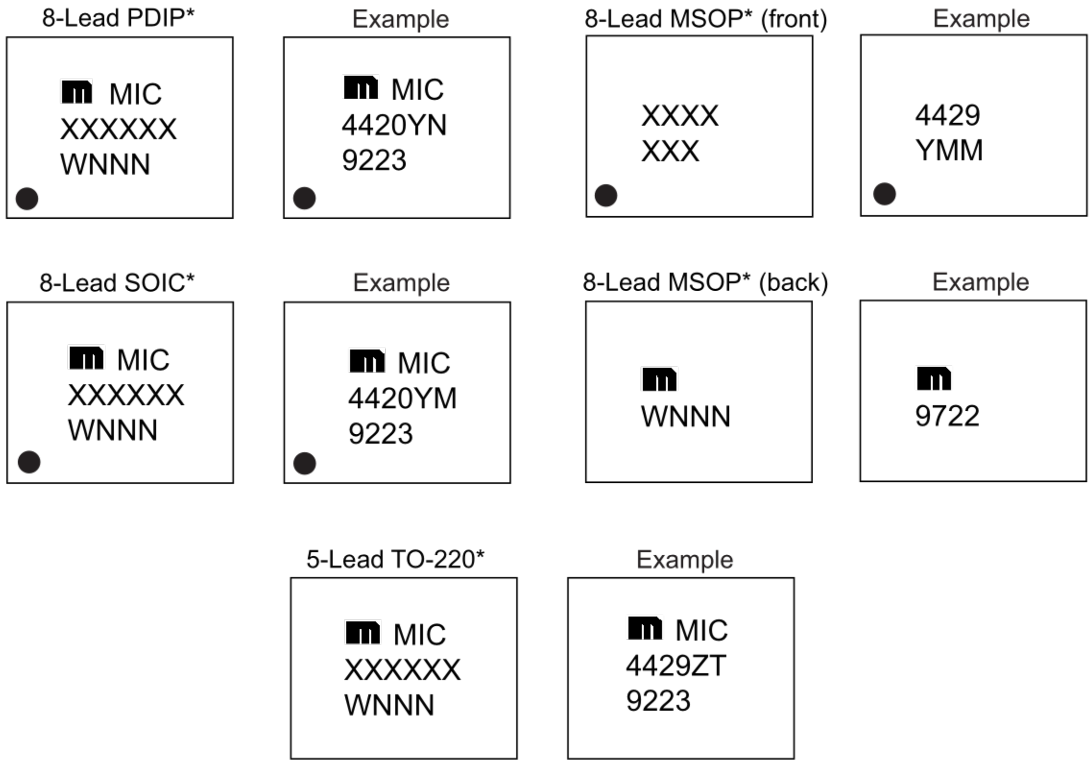


FIGURE 4-3: *Peak Output Current Test Circuit.*

5.0 PACKAGING INFORMATION

5.1 Package Marking Information



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

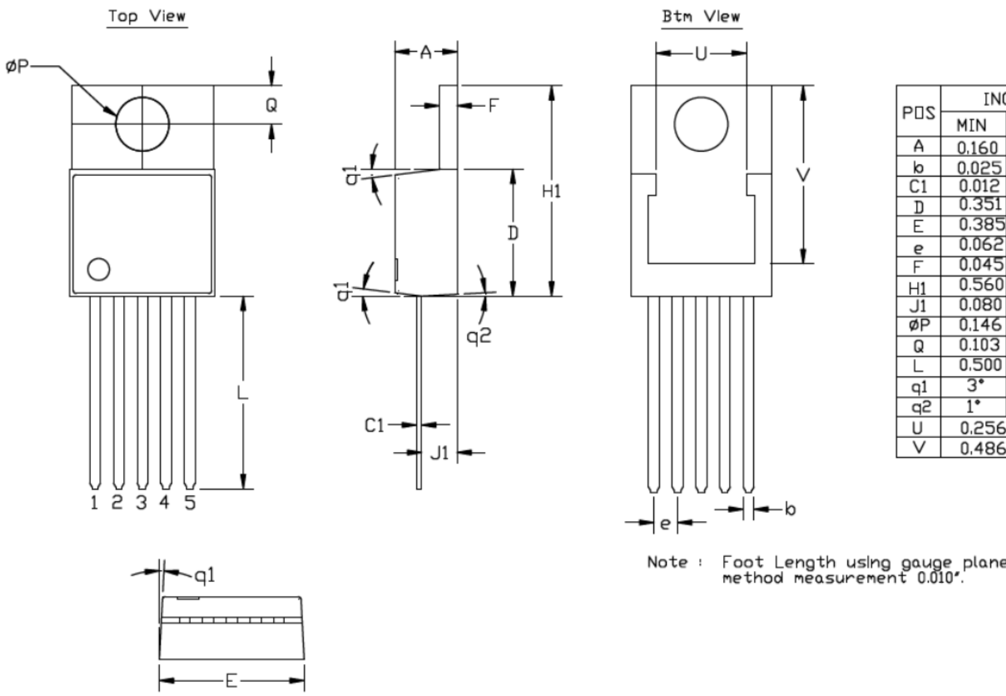
Underbar (_) and/or Overbar (‾) symbol may not be to scale.

Note: If the full seven-character YYWWNNN code cannot fit on the package, the following truncated codes are used based on the available marking space:
6 Characters = YWWNNN; 5 Characters = WWNNN; 4 Characters = WNNN; 3 Characters = NNN; 2 Characters = NN; 1 Character = N

5-Lead TO-220 Package Outline and Recommended Land Pattern

TITLE
5 LEAD TO220 PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	TO220-5LD-PL-1	**UNIT**	INCH
Lead Frame	Copper Alloy	**Lead Finish**	Matte Tin



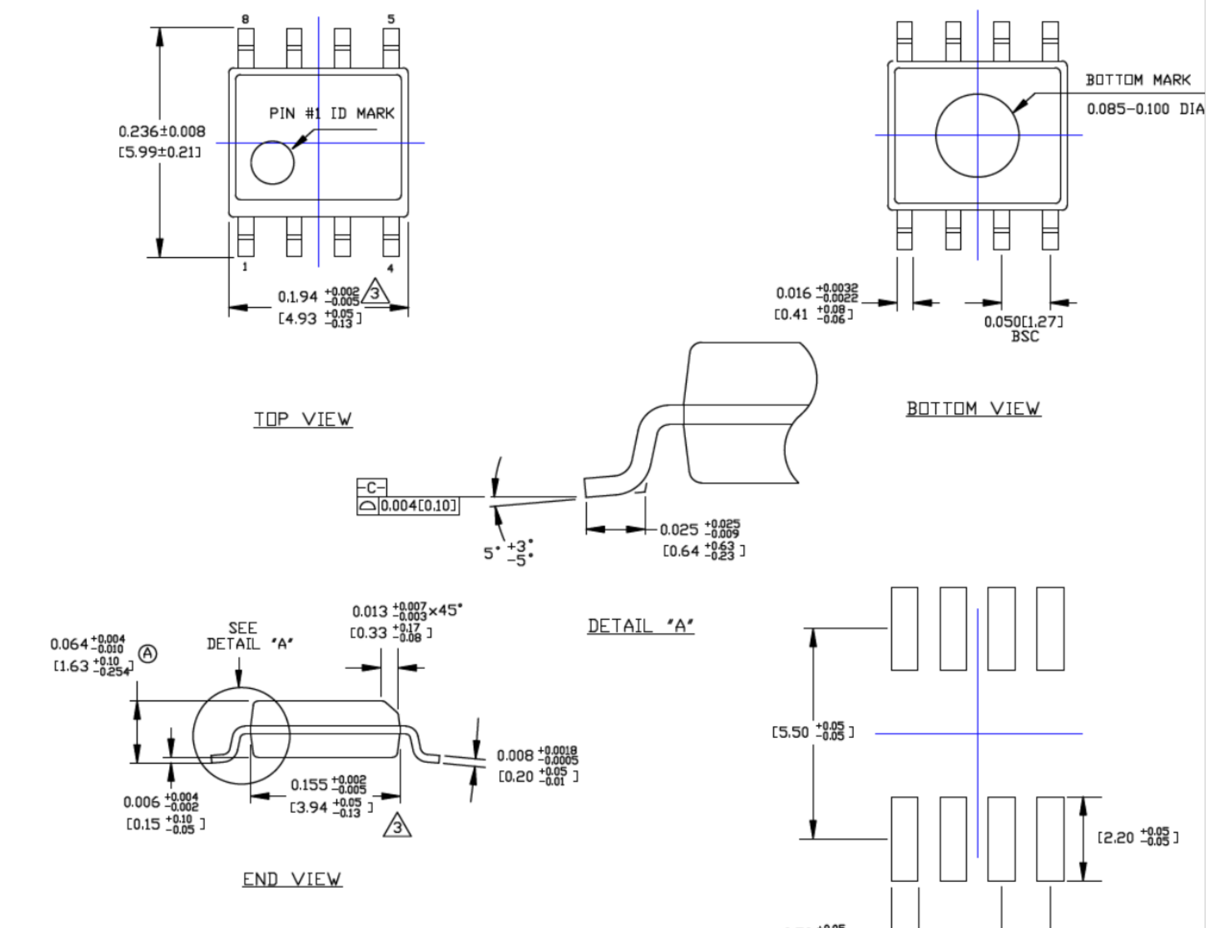
POS	INCH MIN	INCH MAX
A	0.160	0.190
b	0.025	0.040
C1	0.012	0.022
D	0.351	0.361
E	0.385	0.420
e	0.062	0.072
F	0.045	0.055
H1	0.560	0.619
J1	0.080	0.120
øP	0.146	0.156
Q	0.103	0.113
L	0.500	0.580
q1	3°	10°
q2	1°	7°
U	0.256 Ref.	
V	0.486 Ref.	

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

8-Lead SOIC Package Outline and Recommended Land Pattern

TITLE
8 LEAD SOICN PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	SOICN-8LD-PL-1	**UNIT**	INCH [MM]



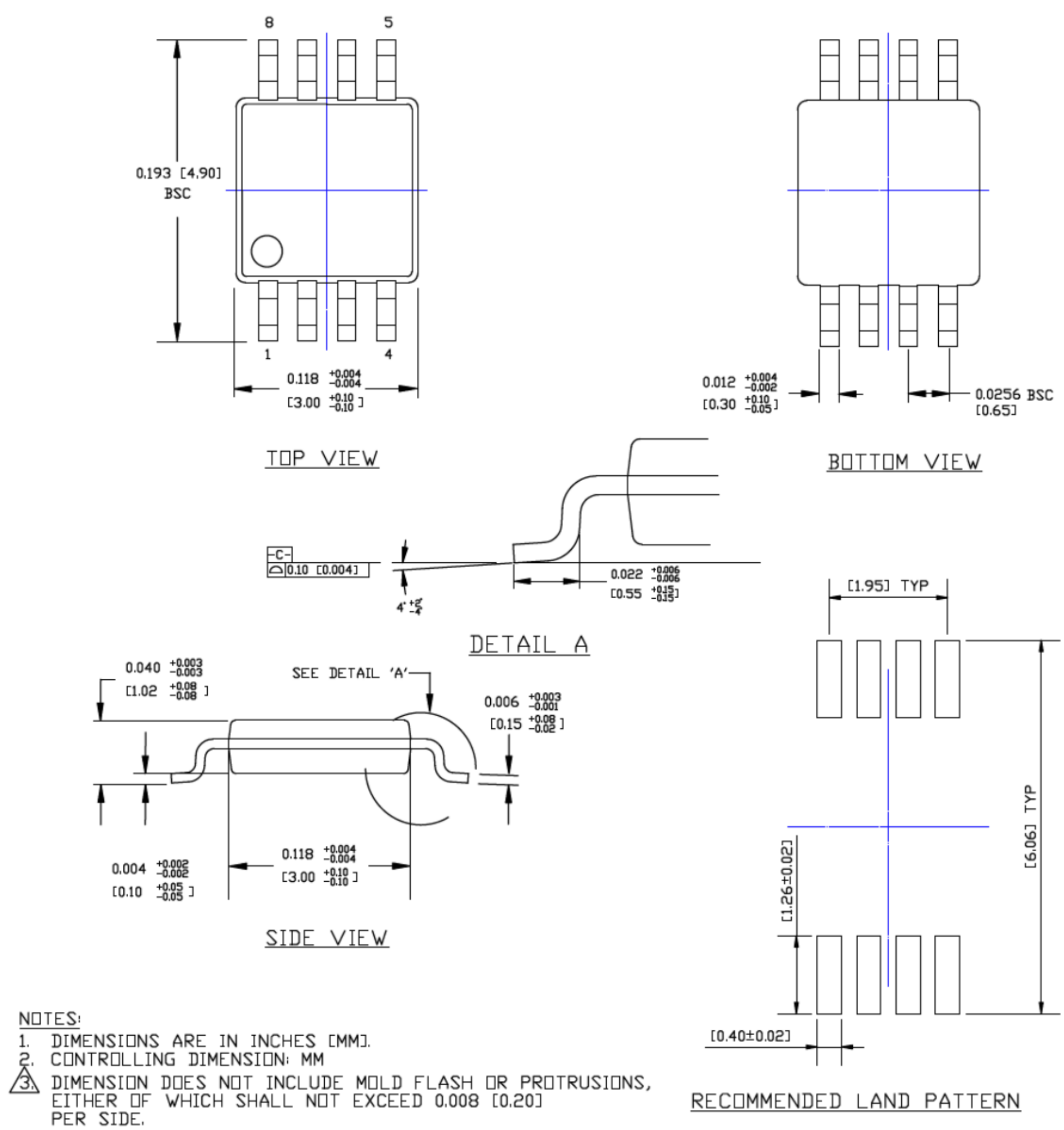
NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.010[0.25] PER SIDE.

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

8-Lead MSOP Package Outline and Recommended Land Pattern

TITLE
8 LEAD MSOP PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	MSOP-8LD-PL-1	UNIT	INCH [MM]

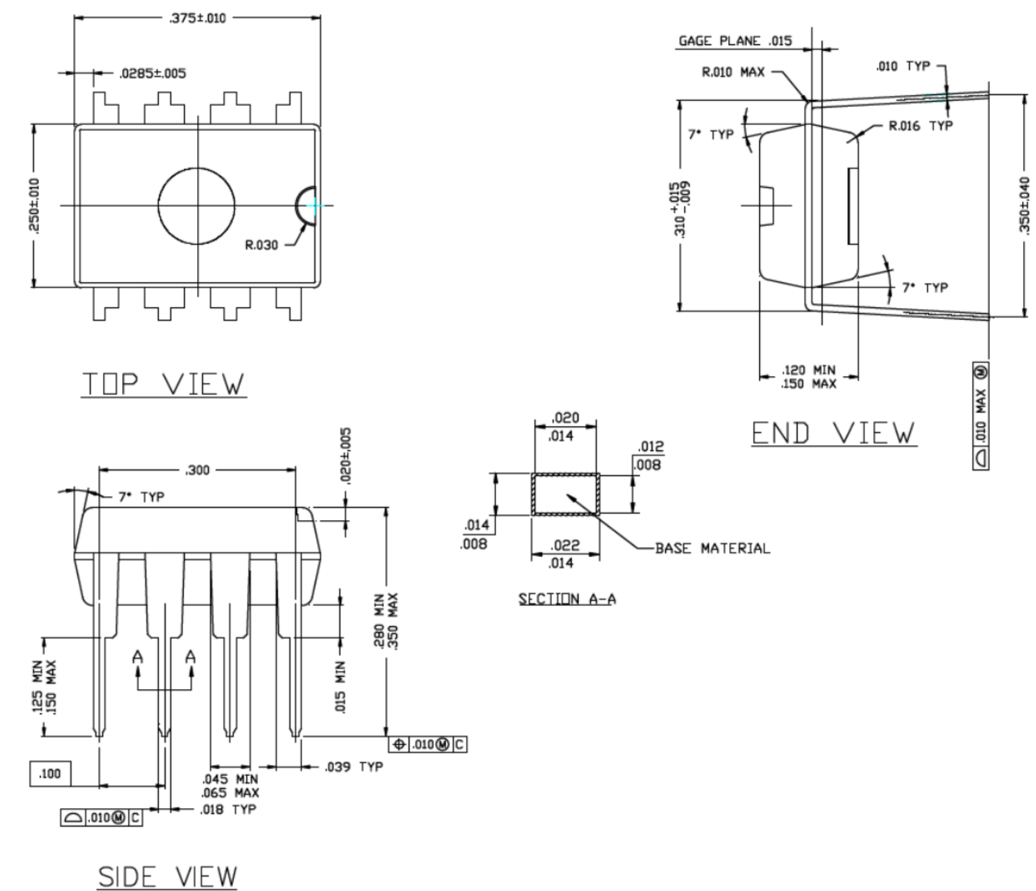


Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

8-Lead PDIP Package Outline and Recommended Land Pattern

TITLE
8 LEAD PDIP PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	PDIP-8LD-PL-1	**UNIT**	INCH
Lead Frame	Copper	**Lead Finish**	Matte Tin



Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (October 2018)

- Converted Micrel document MIC4420/9 to Microchip data sheet DS20006092B.
- Minor text changes throughout.

Revision B (January 2022)

- Corrected **Section 5.1 “Package Marking Information”** device marking specification.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Device	X	XX	-XX
Part No.	Junction Temp. Range	Package	Media Type

Device:	MIC4420:	6A Peak Low-Side Non-Inverting MOSFET Driver, Bipolar/CMOS/DMOS Process
	MIC4429:	6A Peak Low-Side Inverting MOSFET Driver, Bipolar/CMOS/DMOS Process
Junction Temperature Range:	Y =	–40°C to +85°C, RoHS-Compliant
	Z =	0°C to +70°C, RoHS-Compliant
Package:	N =	8-Lead PDIP
	M =	8-Lead SOIC
	MM =	8-Lead MSOP
	T =	5-Lead TO-220
Media Type:	<blank>=	95/Tube (M, SOIC)
	<blank>=	100/Tube (MM, MSOP)
	<blank>=	50/Tube (N, PDIP & T, TO-220)
	TR =	2,500/Reel (SOIC, MSOP)

Examples:

a) MIC4420: 6A Peak Low-Side Non-Inverting MOSFET Driver, Industrial Grade –40°C to +85°C Junction Temperature Range, RoHS-Compliant.

- MIC4420YM: 8-Lead SOIC, 95/Tube
- MIC4420YM-TR: 8-Lead SOIC, 2,500/Reel
- MIC4420YMM: 8-Lead MSOP, 100/Tube
- MIC4420YMM-TR: 8-Lead MSOP, 2,500/Reel
- MIC4420YN: 8-Lead PDIP, 50/Tube

b) MIC4420: 6A Peak Low-Side Non-Inverting MOSFET Driver, Commercial Grade 0°C to +70°C Junction Temperature Range, RoHS-Compliant.

- MIC4420ZM: 8-Lead SOIC, 95/Tube
- MIC4420ZM-TR: 8-Lead SOIC, 2,500/Reel
- MIC4420ZN: 8-Lead PDIP, 50/Tube
- MIC4420ZT: 5-Lead TO-220, 50/Tube

c) MIC4429: 6A Peak Low-Side Inverting MOSFET Driver, Industrial Grade –40°C to +85°C Junction Temperature Range, RoHS-Compliant.

- MIC4429YM: 8-Lead SOIC, 95/Tube
- MIC4429YM-TR: 8-Lead SOIC, 2,500/Reel
- MIC4429YMM: 8-Lead MSOP, 100/Tube
- MIC4429YMM-TR: 8-Lead MSOP, 2,500/Reel
- MIC4429YN: 8-Lead PDIP, 50/Tube

d) MIC4429: 6A Peak Low-Side Inverting MOSFET Driver, Commercial Grade 0°C to +70°C Junction Temperature Range, RoHS-Compliant.

- MIC4429ZM: 8-Lead SOIC, 95/Tube
- MIC4429ZM-TR: 8-Lead SOIC, 2,500/Reel
- MIC4429ZN: 8-Lead PDIP, 50/Tube
- MIC4429ZT: 5-Lead TO-220, 50/Tube

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

For information regarding Microchip’s Quality Management Systems, please visit www.microchip.com/quality.

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