SLCS008A - OCTOBER 1979 - REVISED OCTOBER 1991

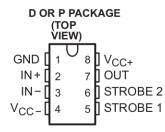
- Fast Response Times
- Improved Gain and Accuracy
- Fanout to 10 Series 54/74 TTL Loads
- Strobe Capability
- Short-Circuit and Surge Protection
- Designed to Be Interchangeable With National Semiconductor LM306

description

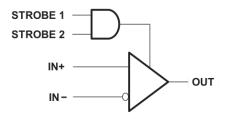
The LM306 is a high-speed voltage comparator with differential inputs, a low-impedance high-sink-current (100 mA) output, and two strobe inputs. This device detects low-level analog or digital signals and can drive digital logic or lamps and relays directly. Short-circuit protection and surge-current limiting is provided.

A low-level input at either strobe causes the output to remain high regardless of the differential input. When both strobe inputs are either open or at a high logic level, the output voltage is controlled by the differential input voltage. The circuit will operate with any negative supply voltage between -3 V and -12 V with little difference in performance.

The LM306 is characterized for operation from 0°C to 70°C.



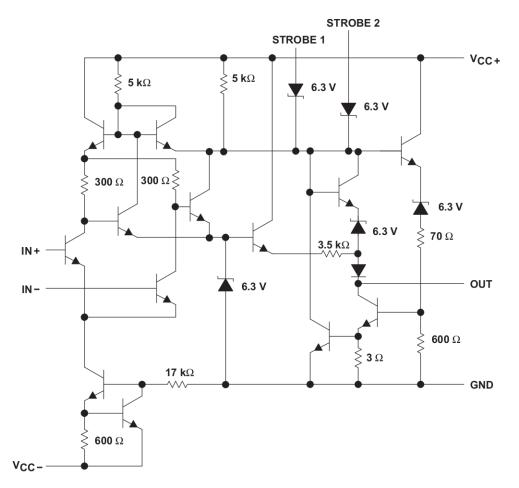
functional block diagram



AVAILABLE OPTIONS

	V	PACKAGE				
TA	V _{IO} max at 25°C	SMALL OUTLINE (D)	PLASTIC DIP (P)			
0°C to 70°C	5 mV	LM306D	LM306P			

schematic



Resistor values are nominal.

LM306 DIFFERENTIAL COMPARATOR WITH STROBES

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V _{CC+} (see Note 1)	15 V
Supply voltage, V _{CC} – (see Note 1)	
Differential input voltage, V _{ID} (see Note 2)	±5 V
Input voltage, V _I (either input, see Notes 1 and 3)	±7 V
Strobe voltage range (see Note 1)	0 V to V _{CC+}
Output voltage, VO (see Note 1)	24 V
Voltage from output to V _{CC} - · · · · · · · · · · · · · · · · · · ·	30 V
Duration of output short circuit to ground (see Note 4)	10 s
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T _A	0°C to 70°C
Storage temperature range	65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages and the voltage from the output to V_{CC} -, are with respect to the network ground.
 - 2. Differential voltages are at IN+ with respect to IN -.
 - 3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 7 V, whichever is less.
 - 4. The output may be shorted to ground or either power supply.

DISSIPATION RATING TABLE

PACKAGE	$T_{\mbox{\scriptsize A}} \le 25^{\circ}\mbox{\scriptsize C}$ POWER RATING	DERATING FACTOR	DERATE ABOVE T _A	T _A = 70°C POWER RATING
D	600 mW	5.8 mW/°C	46°C	464 mW
P	600 mW	8.0 mW/°C	75°C	600 mW

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electrical characteristics at specified free-air temperature, $V_{CC+} = 12 \text{ V}$, $V_{CC-} = -3 \text{ V}$ to -12 V (unless otherwise noted)

	PARAMETER	TEST CON	TEST CONDITIONS†			TYP	MAX	UNIT	
.,				25°C		1.6§	5	.,	
VIO	Input offset voltage	$R_S \le 200 \Omega$	Full range			6.5	mV		
αVIO	Average temperature coefficient of input offset voltage	$R_S = 50 \Omega$,	See Note 5	Full range		5	20	μV/°C	
				25°C		1.8	5		
ΙΙΟ	Input offset current	See Note 5		MIN		1	7.5	μΑ	
				MAX		0.5	5		
	Average temperature coefficient of	See Note 5		MIN to 25°C		24	100	1.100	
αΙΙΟ	input offset current	See Note 5		25°C to MAX		15	50	nA/°C	
	land him adment	V = 0.5 V to 5 V	.,				40	μА	
I _{IB}	Input bias current	$V_{O} = 0.5 \text{ V to } 5 \text{ V}$	25°C to MAX		16	25			
I _{IL(S)}	Low-level strobe current	V _(strobe) = 0.4 V		Full range		-1.7	-3.2	mA	
V _{IH(S)}	High-level strobe voltage			Full range	2.2			V	
V _{IL(S)}	Low-level strobe voltage			Full range			0.9	V	
VICR	Common-mode input voltage range	$V_{CC} = -7 \text{ V to } -1$	12 V	Full range	±5			V	
V _{ID}	Differential input voltage range			Full range	±5			V	
AVD	Large-signal differential voltage amplification	V _O = 0.5 V to 5 V,	No load	25°C		40		V/mV	
Vон	High-level output voltage	I _{OH} = -400 μA	V_{ID} = 8 mV	Full range	2.5		5.5	V	
		I _{OL} = 100 mA	$V_{ID} = -7 \text{ mV}$	25°C		0.8	2		
VOL	Low-level output voltage	I _{OL} = 50 mA	$V_{ID} = -7 \text{ mV}$	Full range			1	V	
		I _{OL} = 16 mA	$V_{ID} = -8 \text{ mV}$	Full range			0.4		
1.	I link lavel autout valta a	V = 0.V t= 0.4.V	$V_D = 7 \text{ mV}$	MIN to 25°C		0.02	2		
ІОН	High-level output voltage	V _{OH} = 8 V to 24 V	V _{ID} = 8 mV	25°C to MAX			100	μΑ	
ICC+	Supply current from V _{CC+}	V _{ID} = −5 mV,	No load	Full range		6.6	10	mA	
ICC-	Supply current from V _{CC} -	No load		Full range		-1.9	-3.6	mA	

[†] Unless otherwise noted, all characteristics are measured with both strobes open.

NOTE 5: The offset voltages and offset currents given are the maximum values required to drive the output down to the low range (V_{OL}) or up to the high range (V_{OH}). These parameters actually define an error band and take into account the worst-case effects of voltage gain and input impedance.

switching characteristics, $V_{CC+} = 12 \text{ V}$, $V_{CC-} = -6 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
Response time, low-to-high-level output	R_L = 390 Ω to 5 V, C_L = 15 pF, See Note 6		28	40	ns

[†] All characteristics are measured with both strobes open.

NOTE 6: The response time specified is for a 100-mV input step with 5-mV overdrive and is the interval between the input step function and the instant when the output crosses 1.4 V.



[‡] Full range is 0°C to 70°C. MIN is 0°C. MAX is 70°C.

[§] This typical value is at $V_{CC+} = 12 \text{ V}$, $V_{CC-} = -6 \text{ V}$.

Table of Graphs

			FIGURE
I _{IB}	Input bias current	vs Free-air temperature	1
lιο	Input offset current	vs Free-air temperature	2
Vон	High-level output voltage	vs Free-air temperature	3
VOL	Low-level output voltage	vs Free-air temperature	4
VO	Output voltage	vs Differential input voltage	5
lo	Output current	vs Differential input voltage	6
AVD	Large-signal differential voltage amplification	vs Free-air temperature	7
los	Short-circuit output current	vs Free-air temperature	8
	Output response	vs Time	9, 10
ICC+	Positive supply current	vs Positive supply voltage	11
ICC-	Negative supply current	vs Negative supply voltage	12
PD	Total power dissipation	vs Free-air temperature	13

INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

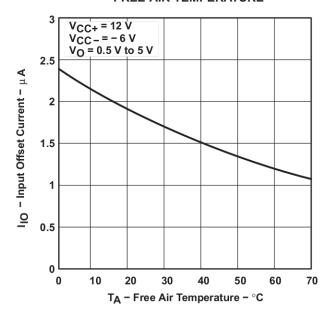


Figure 1

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

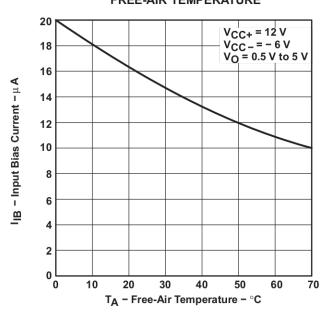


Figure 2

HIGH-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

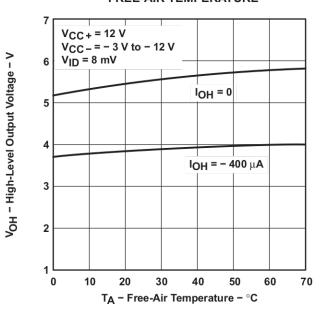


Figure 3

OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

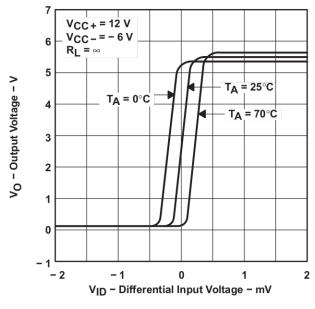


Figure 5

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

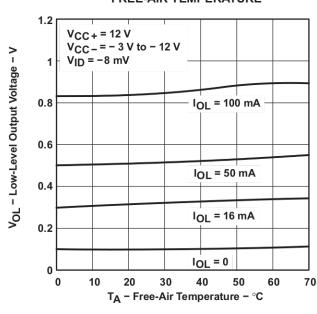


Figure 4

OUTPUT CURRENT vs DIFFERENTIAL INPUT VOLTAGE

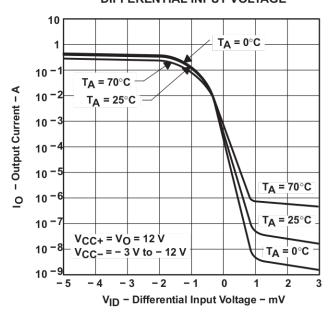
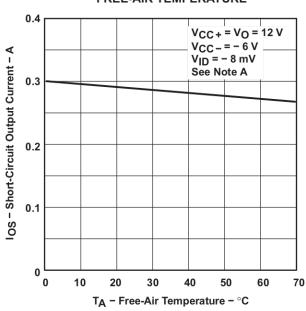


Figure 6

LARGE-SIGNAL DIFFERENTIAL **VOLTAGE AMPLIFICATION** vs FREE-AIR TEMPERATURE 80,000 $V_{CC} = -3 V \text{ to } -12 V$ $V_0 = 1 \text{ to } 2 \text{ V}$ $R_L = \infty$ A_{VD} - Large-Signal Differential Voltage Amplification 60,000 V_{CC+} = 15 V 40,000 $V_{CC+} = 10 V$ V_{CC+} = 15 V 20,000 0 0 10 20 30 40 50 60 70

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

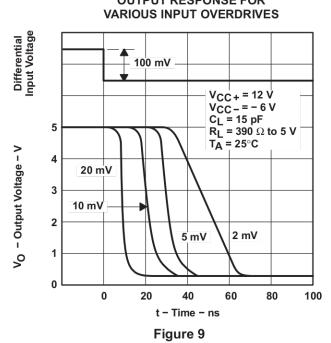


NOTE A: This parameter was measured using a single 5-ms pulse.

Figure 8

Figure 7 OUTPUT RESPONSE FOR

TA - Free-Air Temperature - °C



OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVES

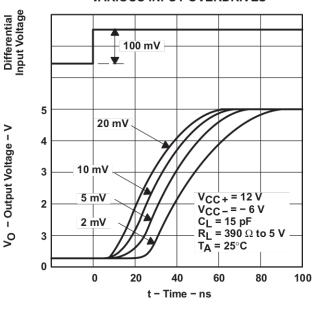
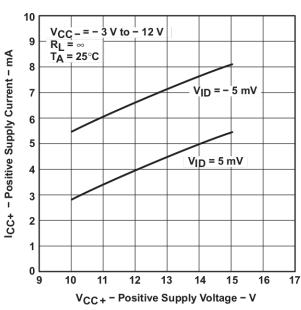


Figure 10

POSITIVE SUPPLY CURRENT vs POSITIVE SUPPLY VOLTAGE



NEGATIVE SUPPLY CURRENT vs
NEGATIVE SUPPLY VOLTAGE

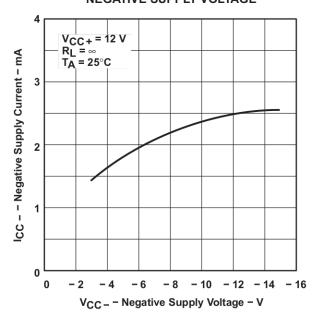


Figure 11 Figure 12

TOTAL POWER DISSIPATION vs FREE-AIR TEMPERATURE

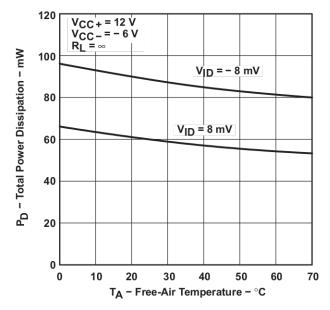


Figure 13



PACKAGE OPTION ADDENDUM

10-Dec-2020

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead finish/ Ball material	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
LM306D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM306	Samples
LM306P	ACTIVE	PDIP	Р	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	LM306P	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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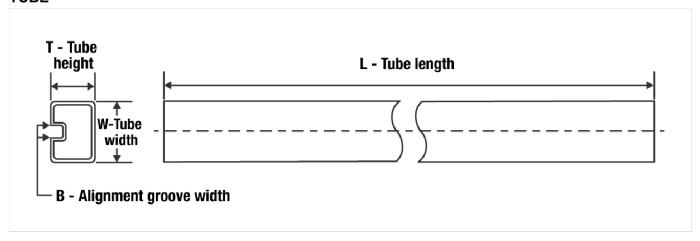
PACKAGE OPTION ADDENDUM

10-Dec-2020

PACKAGE MATERIALS INFORMATION

www.ti.com 5-Jan-2022

TUBE

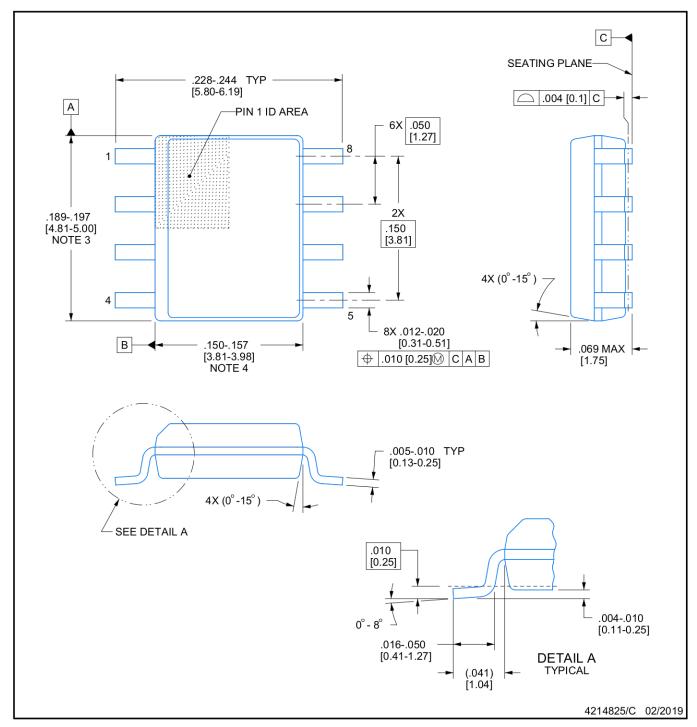


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM306D	D	SOIC	8	75	507	8	3940	4.32
LM306P	Р	PDIP	8	50	506	13.97	11230	4.32



SMALL OUTLINE INTEGRATED CIRCUIT

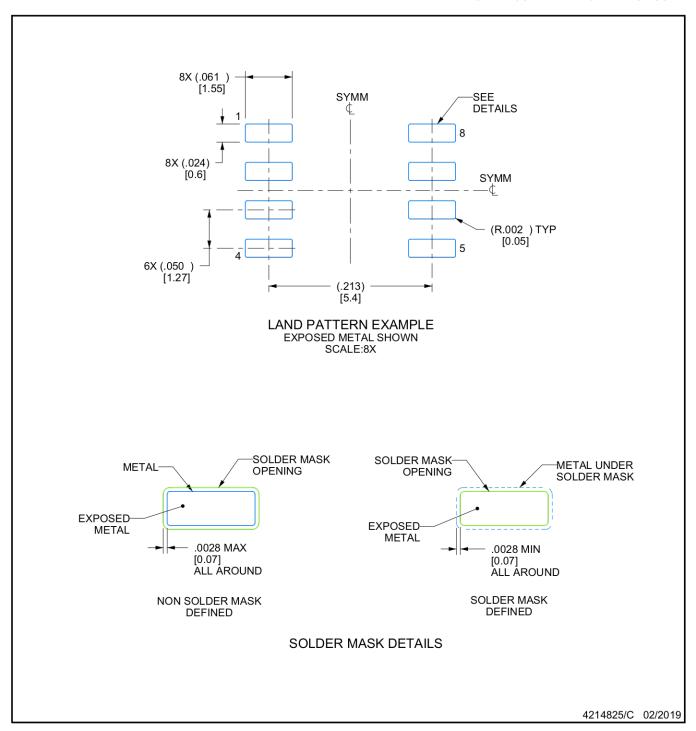


NOTES:

- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.



SMALL OUTLINE INTEGRATED CIRCUIT



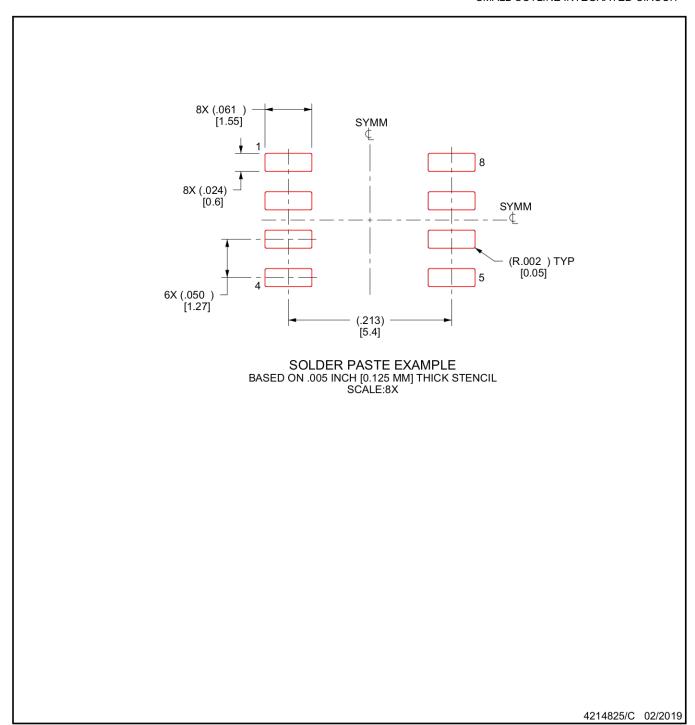
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



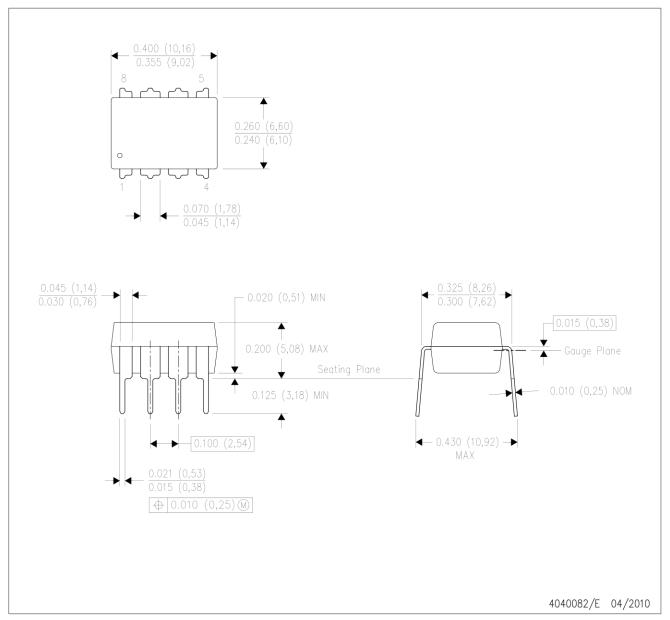
NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001 variation BA.



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