

Description

The μ PD446 is a high-speed, low-power, 2048-word by 8-bit static CMOS RAM fabricated with advanced silicon-gate CMOS technology. A unique circuitry technique makes the μ PD446 a very low operating power device which requires no clock or refreshing to operate. Minimum standby power current is drawn by this device when \overline{CS} equals V_{CC} independently of the other input levels. Data retention is guaranteed at a power supply voltage as low as 2V.

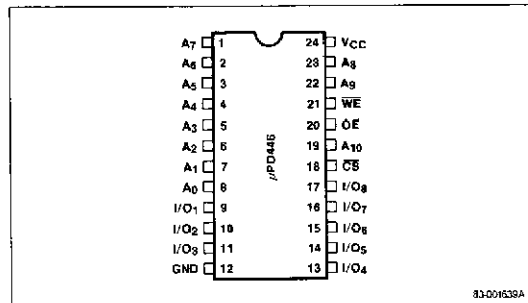
The μ PD446 has a standard 24-pin dual-in-line package and is plug-in compatible with 16K EPROMs.

The μ PD446 is also packaged in a miniflat package providing high density application.

Features

- Single +5V supply
- Fully static operation — no clock or refreshing required
- TTL compatible — all inputs and outputs
- Common I/O using three-state output
- \overline{OE} eliminates need for external bus buffers
- Max access/min cycle times down to 150 ns
- Low power dissipation
 - Active: 38 mA max
 - Standby: 10 μ A max
- Data retention voltage: 2V min
- Operating temperature range: -40°C to $+85^{\circ}\text{C}$
- Standard 24-pin plastic package (μ PD446C)
- Plug-in compatible with 16K EPROMs (μ PD446C)
- Miniflat package for high density application (μ PD446G)
- L version
 - Standby current 1.0 μ A max at 60°C for battery backup operation

Pin Configuration



Pin Identification

No.	Symbol	Function
1-8, 19, 22, 23	A_7 - A_{10}	Address input
9-11, 13-17	I/O_1 - I/O_8	Data input / output
18	\overline{CS}	Chip select
20	\overline{OE}	Output enable
21	\overline{WE}	Write enable
24	V_{CC}	Power (+5V)
12	GND	GND

Performance Ranges

Device	Access Time (Max)	Cycle Time (Min)	Power Supply (Max)	
			Active	Standby
μ PD446C-3, 446G-15	150 ns	150 ns	38 mA	(Note 1)
μ PD446C-2, 446G-20	200 ns	200 ns	30 mA	(Note 1)
μ PD446C-1, 446G-25	250 ns	250 ns	26 mA	(Note 1)
μ PD446C, 446G-45	450 ns	450 ns	18 mA	(Note 1)

Note:

(1) μ PD446C-L/-1L/-2L/-3L, μ PD446G-45L/25L/20L/15L

$T_A = 25^{\circ}\text{C}$, 0.2 μ A

$T_A = 60^{\circ}\text{C}$, 1.0 μ A

$T_A = 85^{\circ}\text{C}$, 10 μ A

μ PD446C/-1/-2/-3, μ PD446G-45/25/20/15

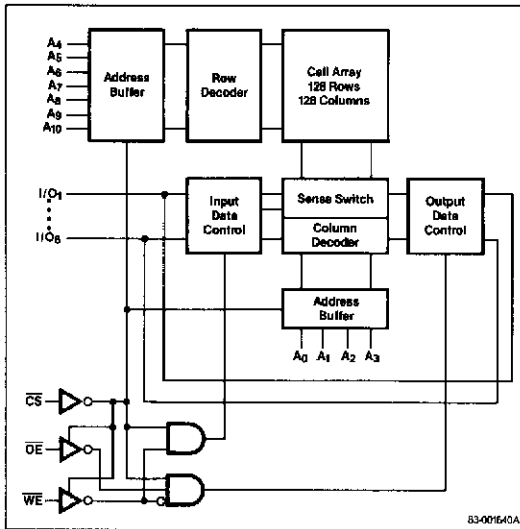
$T_A = 25^{\circ}\text{C}$, 1.0 μ A

$T_A = 60^{\circ}\text{C}$, 5.0 μ A

$T_A = 85^{\circ}\text{C}$, 10 μ A

μPD446

Block Diagram



Absolute Maximum Ratings

Power supply voltage, V_{CC}	7.0 V
Input voltage, V_{IN}	-0.3 to $V_{CC} + 0.3$ V
Output voltage, V_{OUT}	-0.3 to $V_{CC} + 0.3$ V
Operating temperature, T_{OPR}	-40 to 85°C
Storage temperature, T_{STG}	-55 to 125°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

$T_A = 25^\circ\text{C}$, $f = 1\text{MHz}$

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Input capacitance	C_{IN}			6	pF	$V_{IN} = 0\text{V}$
Input/output capacitance	$C_{I/O}$			8	pF	$V_{I/O} = 0\text{V}$

Recommended DC Operating Conditions

$T_A = -40$ to $+85^\circ\text{C}$

Parameter	Symbol	Limits			Unit
		Min	Typ	Max	
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage low	V_{IL}	-0.3		0.8	V
Input voltage high	V_{IH}	2.2		$V_{CC} + 0.3$	V

DC Characteristics

$T_A = -40$ to 85°C , $V_{CC} = 5\text{V} \pm 10\%$

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Input leakage current	I_{LI}			1	μA	$V_{IN} = 0\text{V}$ to V_{CC}
I/O leakage current	I_{LO}			1	μA	$V_{I/O} = 0\text{V}$ to V_{CC} $\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
Operating supply current	I_{CCA1}		(1)	(1)	mA	$\overline{CS} = V_{IL}$, $I_{I/O} = 0\text{V}$ min cycle
Operating supply current	I_{CCA2}		5	10	mA	$\overline{CS} = V_{IL}$, $I_{I/O} = 0\text{V}$ DC current
Standby supply current	I_{CCS}		0.02	(2)	μA	$\overline{CS} = V_{CC} - 0.2\text{V}$, $V_{IN} = 0\text{V}$ to V_{CC}
Output voltage low	V_{OL}			0.4	V	$I_{OL} = 2.0\text{mA}$
Output voltage high	V_{OH}	2.4			V	$I_{OH} = -1.0\text{mA}$

Notes:

- (1) $\mu\text{PD446C-3/3L}$, $\mu\text{PD446G-15/15L}$: 25 mA typ, 38 mA max
 $\mu\text{PD446C-2/2L}$, $\mu\text{PD446G-20/20L}$: 20 mA typ, 30 mA max
 $\mu\text{PD446C-1/1L}$, $\mu\text{PD446G-25/25L}$: 18 mA typ, 26 mA max
 $\mu\text{PD446C/-L}$, $\mu\text{PD446G-45/45L}$: 12 mA typ, 18 mA max
 (2) $\mu\text{PD446C-L/-1L/-2L/-3L}$, $\mu\text{PD446G-45L/25L/20L/15L}$

$T_A = 25^\circ\text{C}$, 0.2 μA

$T_A = 60^\circ\text{C}$, 1.0 μA

$T_A = 85^\circ\text{C}$, 10 μA

$\mu\text{PD446C-1/-2/-3}$, $\mu\text{PD446G-45/25/20/15}$

$T_A = 25^\circ\text{C}$, 1.0 μA

$T_A = 60^\circ\text{C}$, 5.0 μA

$T_A = 85^\circ\text{C}$, 10 μA

AC Characteristics

 $T_A = -40 \text{ to } 85^\circ\text{C}$, $V_{CC} = 5 \text{ V} \pm 10\%$

Parameter	Symbol	μPD446C-3 μPD446G-15		μPD446C-2 μPD446G-20		μPD446C-1 μPD446G-25		μPD446C μPD446G-45		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle										
Read cycle time	t_{RC}	150		200		250		450		ns
Address access time	t_{AA}		150		200		250		450	ns
Chip select access time	t_{ACS}		150		200		250		450	ns
Output enable to output valid	t_{OE}		75		100		120		150	ns
Output hold from address change	t_{OH}	15		15		15		15		ns
Chip select to output in Lo-Z	t_{CLZ}	10		10		10		10		ns
Output enable to output in Lo-Z	t_{OLZ}	5		5		5		5		ns
Chip deselect to output in Hi-Z	t_{CHZ}		50		60		80		100	ns
Output disable to output in Hi-Z	t_{OHZ}		50		60		80		100	ns
Write Cycle										
Write cycle time	t_{WC}	150		200		250		450		ns
Chip select to end of write	t_{CW}	120		150		180		210		ns
Address valid to end of write	t_{AW}	120		150		180		210		ns
Address setup time	t_{AS}	0		0		0		0		ns
Write pulse width	t_{WP}	90		120		150		180		ns
Write recovery time	t_{WR}	0		0		0		0		ns
Data valid to end of write	t_{DW}	50		60		80		100		ns
Data hold time	t_{DH}	0		0		0		0		ns
Write enable to output in Hi-Z	t_{WHZ}		50		60		80		100	ns
Output active from end of write	t_{OW}	10		10		10		10		ns

AC Test Conditions

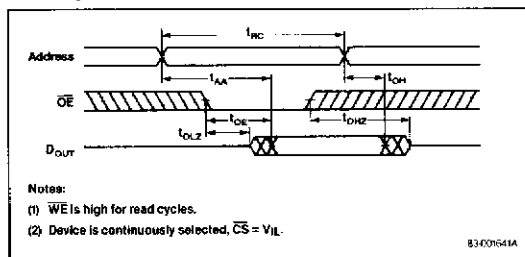
Input pulse levels	0.8 to 2.2 V
Input pulse rise and fall time	10 ns
Timing reference levels	1.5 V
Output load	1 TTL + 100 pF

Truth Table

CS	OE	WE	MODE	I/O	I_{CC}
H	X	X	Not selected	Hi-Z	Standby
L	H	H	Not selected	Hi-Z	Active
L	L	H	Read	D_{OUT}	Active
L	X	L	Write	D_{IN}	Active

Timing Waveforms

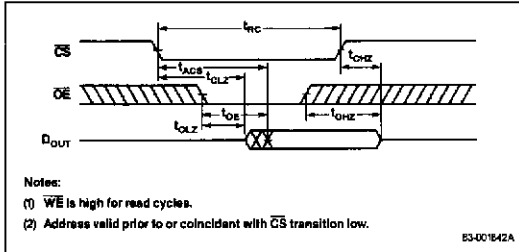
Read Cycle No. 1



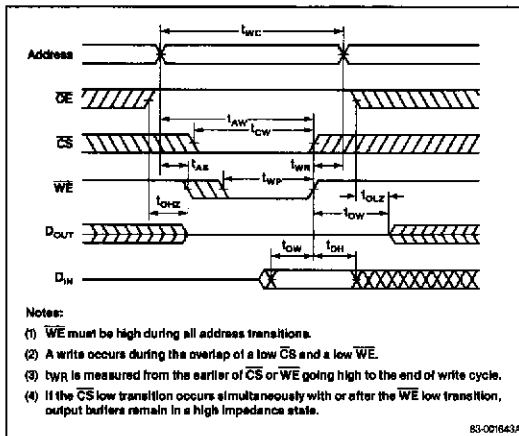
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Timing Waveforms (cont)

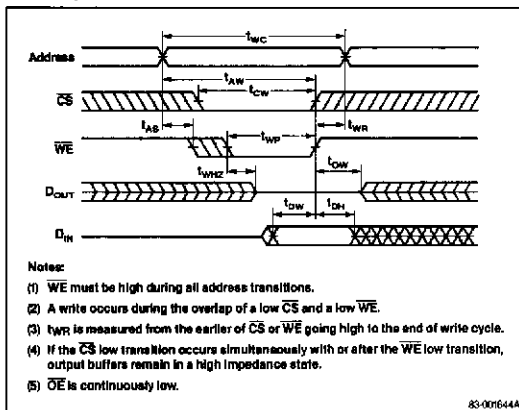
Read Cycle No. 2



Write Cycle No. 1



Write Cycle No. 2



Low V_{CC} Data Retention Characteristics

$T_A = -40$ to 85°C

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Data retention supply voltage	V_{CCDR}	2.0			V	$V_{IN} = 0\text{V to }V_{CC}$, $CS = V_{CC}$
Data retention supply current	I_{CCDR}		0.01	(1)	μA	$V_{IN} = 0\text{V to }V_{CC}$, $CS = V_{CC}$, $V_{CC} = 3.0\text{V}$
Chip deselection to data retention mode	t_{CDR}	0			ns	
Operation recovery time	t_R		t_{RC}		ns	

Note:

(1) $\mu\text{PD446C-LJ-1LJ-2LJ-3L}$, $\mu\text{PD446G-45L/25L/20L/15L}$

$T_A = 25^\circ\text{C}$, $0.2\ \mu\text{A}$

$T_A = 60^\circ\text{C}$, $1.0\ \mu\text{A}$

$T_A = 85^\circ\text{C}$, $10\ \mu\text{A}$

$\mu\text{PD446CJ-1J-2J-3J}$, $\mu\text{PD446G-45J/25J/20J/15J}$

$T_A = 25^\circ\text{C}$, $1.0\ \mu\text{A}$

$T_A = 60^\circ\text{C}$, $5.0\ \mu\text{A}$

$T_A = 85^\circ\text{C}$, $10\ \mu\text{A}$

Low V_{CC} Data Retention

