74HC4002; 74HCT4002

Dual 4-input NOR gate Rev. 5 — 26 May 2016

Product data sheet

General description 1.

The 74HC4002; 74HCT4002 is a dual 4-input NOR gate. Inputs also include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of $V_{CC}. \\$

Features and benefits 2.

- Complies with JEDEC standard JESD7A
- Low-power dissipation
- Input levels:
 - ◆ For 74HC4002: CMOS level
 - ◆ For 74HCT4002: TTL level
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ♦ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +80 °C and from -40 °C to +125 °C.

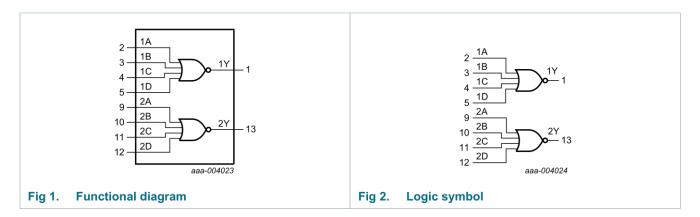
Ordering information 3.

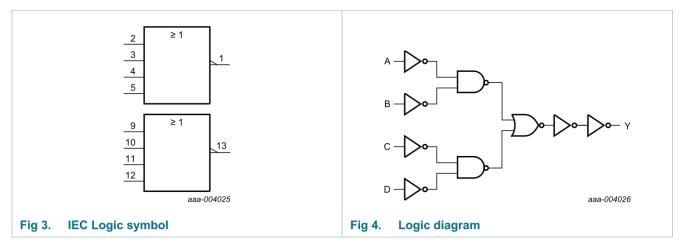
Table 1. **Ordering information**

| Type number | Package | | | | | | | | | | | |
|-------------|-------------------|---------|--|----------|--|--|--|--|--|--|--|--|
| | Temperature range | Name | Description | Version | | | | | | | | |
| 74HC4002D | –40 °C to +125 °C | SO14 | plastic small outline package; 14 leads; body width | SOT108-1 | | | | | | | | |
| 74HCT4002D | | | 3.9 mm | | | | | | | | | |
| 74HC4002DB | –40 °C to +125 °C | SSOP14 | plastic shrink small outline package; 14 leads; body | SOT337-1 | | | | | | | | |
| 74HCT4002DB | | | width 5.3 mm | | | | | | | | | |
| 74HC4002PW | –40 °C to +125 °C | TSSOP14 | plastic thin shrink small outline package; 14 leads; body width 4.4 mm | SOT402-1 | | | | | | | | |



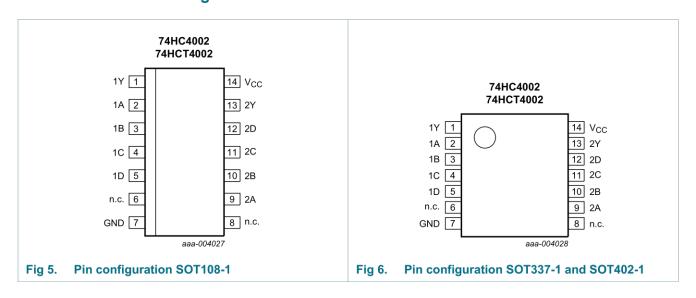
4. Functional diagram





5. Pinning information

5.1 Pinning



74HC_HCT4002

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5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|-----------------|---------------|----------------|
| 1Y | 1 | data output |
| 1A, 1B, 1C, 1D | 2, 3, 4, 5 | data input |
| n.c. | 6, 8 | not connected |
| GND | 7 | ground (0 V) |
| 2Y | 13 | data output |
| 2A, 2B, 2C, 2D | 9, 10, 11, 12 | data input |
| V _{CC} | 14 | supply voltage |

6. Functional description

Table 3. Function table[1]

| Input | nput | | | | | | | | | |
|-------|------|----|----|----|--|--|--|--|--|--|
| nA | nB | nC | nD | nY | | | | | | |
| L | L | L | L | Н | | | | | | |
| Н | X | X | Х | L | | | | | | |
| X | Н | X | X | L | | | | | | |
| X | X | Н | X | L | | | | | | |
| X | X | X | Н | L | | | | | | |

^[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|------------------|-------------------------|---|------------|------|------|------|
| V _{CC} | supply voltage | | | -0.5 | +7 | V |
| I _{IK} | input clamping current | $V_{I} < -0.5 \text{ V or } V_{I} > V_{CC} + 0.5 \text{ V}$ | <u>[1]</u> | - | ±20 | mA |
| I _{OK} | output clamping current | $V_{O} < -0.5 \text{ V or } V_{O} > V_{CC} + 0.5 \text{ V}$ | <u>[1]</u> | - | ±20 | mA |
| Io | output current | $-0.5 \text{ V} < \text{V}_{\text{O}} < \text{V}_{\text{CC}} + 0.5 \text{ V}$ | | - | ±25 | mA |
| I _{CC} | supply current | | | - | 50 | mA |
| I _{GND} | ground current | | | -50 | - | mA |
| T _{stg} | storage temperature | | | -65 | +150 | °C |
| P _{tot} | total power dissipation | SO14, and (T)SSOP14 packages | [2] | - | 500 | mW |

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

^[2] For SO14 package: P_{tot} derates linearly with 8 mW/K above 70 °C. For (T)SSOP14 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

| Symbol | Parameter | Conditions | 7 | 4HC400 | 2 | 74 |)2 | Unit | |
|------------------|-------------------------------------|-------------------------|-----|--------|-----------------|-----|------|-----------------|------|
| | | | Min | Тур | Max | Min | Тур | Max | |
| V _{CC} | supply voltage | | 2.0 | 5.0 | 6.0 | 4.5 | 5.0 | 5.5 | V |
| VI | input voltage | | 0 | - | V _{CC} | 0 | - | V _{CC} | V |
| Vo | output voltage | | 0 | - | V _{CC} | 0 | - | V _{CC} | V |
| T _{amb} | ambient temperature | | -40 | +25 | +125 | -40 | +25 | +125 | °C |
| Δt/ΔV | input transition rise and fall rate | V _{CC} = 2.0 V | - | - | 625 | - | - | - | ns/V |
| | | V _{CC} = 4.5 V | - | 1.67 | 139 | - | 1.67 | 139 | ns/V |
| | | V _{CC} = 6.0 V | - | - | 83 | _ | - | - | ns/V |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | | 25 °C | | -40 °C t | o +85 °C | -40 °C t | o +125 °C | Unit |
|-----------------|--------------------------|--|------|-------|------|----------|----------|----------|-----------|------|
| | | | Min | Тур | Max | Min | Max | Min | Max | |
| 74HC40 | 02 | | | | | | | | | |
| V _{IH} | HIGH-level | V _{CC} = 2.0 V | 1.5 | 1.2 | - | 1.5 | - | 1.5 | - | V |
| | input voltage | V _{CC} = 4.5 V | 3.15 | 2.4 | - | 3.15 | - | 3.15 | - | V |
| | | V _{CC} = 6.0 V | 4.2 | 3.2 | - | 4.2 | - | 4.2 | - | V |
| V_{IL} | LOW-level | V _{CC} = 2.0 V | - | 0.8 | 0.5 | - | 0.5 | - | 0.5 | V |
| input voltage | | V _{CC} = 4.5 V | - | 2.1 | 1.35 | - | 1.35 | - | 1.35 | V |
| | V _{CC} = 6.0 V | - | 2.8 | 1.8 | - | 1.8 | - | 1.8 | V | |
| V _{OH} | HIGH-level | $V_I = V_{IH}$ or V_{IL} | | | | | | | | |
| output v | output voltage | $I_{O} = -20 \mu A; V_{CC} = 2.0 V$ | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | $I_{O} = -20 \mu A$; $V_{CC} = 4.5 V$ | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | $I_{O} = -20 \mu A; V_{CC} = 6.0 V$ | 5.9 | 6.0 | - | 5.9 | - | 5.9 | - | V |
| | | $I_O = -4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$ | 3.98 | 4.32 | - | 3.84 | - | 3.7 | - | V |
| | | $I_{O} = -5.2 \text{ mA}; V_{CC} = 6.0 \text{ V}$ | 5.48 | 5.81 | - | 5.34 | - | 5.2 | - | V |
| V_{OL} | LOW-level | $V_I = V_{IH}$ or V_{IL} | | | | | | | | |
| | output voltage | $I_O = 20 \mu A; V_{CC} = 2.0 V$ | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O = 20 \mu A; V_{CC} = 4.5 V$ | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O = 20 \mu A; V_{CC} = 6.0 V$ | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O = 4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$ | - | 0.15 | 0.26 | - | 0.33 | - | 0.4 | V |
| | | $I_O = 5.2 \text{ mA}; V_{CC} = 6.0 \text{ V}$ | - | 0.16 | 0.26 | - | 0.33 | - | 0.4 | V |
| lı | input leakage current | $V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$ | - | - | ±0.1 | - | ±1 | - | ±1 | μА |
| I _{CC} | supply current | $V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0 \text{ V}$ | - | - | 2 | - | 20 | - | 40 | μΑ |

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | | 25 °C | | –40 °C t | o +85 °C | –40 °C t | o +125 °C | Unit |
|------------------|---------------------------|---|------|-------|------|----------|----------|----------|-----------|------|
| | | | Min | Тур | Max | Min | Max | Min | Max | |
| Cı | input capacitance | | - | 3.5 | - | - | - | - | - | pF |
| 74HCT4 | 002 | | | | | | | | | |
| V_{IH} | HIGH-level input voltage | V _{CC} = 4.5 V to 5.5 V | 2.0 | 1.6 | - | 2.0 | - | 2.0 | - | V |
| V_{IL} | LOW-level input voltage | V _{CC} = 4.5 V to 5.5 V | - | 1.2 | 8.0 | - | 0.8 | - | 8.0 | V |
| V _{OH} | HIGH-level | $V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$ | | | | | | | | |
| | output voltage | $I_{O} = -20 \mu A$ | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | $I_{O} = -4.0 \text{ mA}$ | 3.84 | 4.32 | - | 3.84 | - | 3.7 | - | V |
| V _{OL} | LOW-level | $V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$ | | | | | | | | |
| | output voltage | I _O = 20 μA | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 5.2 mA | - | 0.15 | 0.26 | - | 0.33 | - | 0.4 | V |
| l _l | input leakage current | $V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$ | - | - | ±0.1 | - | ±1 | - | ±1 | μΑ |
| I _{CC} | supply current | $V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V | - | - | 2 | - | 20 | - | 40 | μΑ |
| Δl _{CC} | additional supply current | per input pin; $V_I = V_{CC} - 2.1 \text{ V}; I_O = 0 \text{ A};$ other inputs at V_{CC} or GND; $V_{CC} = 4.5 \text{ V}$ to 5.5 V | - | 45 | 162 | - | 203 | - | 221 | μА |
| Cı | input capacitance | | - | 3.5 | - | - | - | - | - | pF |

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; C_L = 50 pF; for load circuit see Figure 8.

| Symbol | Parameter | Conditions | | | 25 °C | | -40 °C to | o +125 °C | Unit |
|-----------------|-------------------------------|---|-----|-----|-------|----------------|-----------------|-----------|------|
| | | | Min | Тур | Max | Max (85 °C) | Max (125 °C) | | |
| 74HC400 |)2 | | | | | | | | |
| t _{pd} | propagation delay | nA, nB, nC or nD to nY; see Figure 7 | [1] | | | | | | |
| | | V _{CC} = 2.0 V | | - | 30 | 100 | 125 | 150 | ns |
| | | V _{CC} = 4.5 V | | - | 11 | 20 | 25 | 30 | ns |
| | | V _{CC} = 6.0 V | | - | 9 | 17 | 21 | 26 | ns |
| | | $V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$ | | - | 9 | - | - | - | ns |
| t _t | transition time | see Figure 7 | [2] | | | | | | |
| | | V _{CC} = 2.0 V | | - | 19 | 75 | 95 | 110 | ns |
| | | V _{CC} = 4.5 V | | - | 7 | 15 | 19 | 22 | ns |
| | | V _{CC} = 6.0 V | | - | 6 | 13 | 16 | 19 | ns |
| C_{PD} | power dissipation capacitance | per package; V _I = GND to V _{CC} | [3] | - | 16 | - | - | - | pF |
| 74HCT40 | 002 | | | | | | | | |
| t _{pd} | propagation delay | nA, nB, nC or nD to nY; see Figure 7 | [1] | | | | | | |
| | | V _{CC} = 4.5 V | | - | 13 | 22 | 28 | 33 | ns |
| | | V _{CC} = 5.0 V; C _L = 15 pF | | - | 11 | - | - | - | ns |
| t _t | transition time | V _{CC} = 4.5 V; see Figure 7 | [2] | - | 7 | 15 | 19 | 22 | ns |
| C_{PD} | power dissipation capacitance | per package; $V_I = GND \text{ to } V_{CC} - 1.5 \text{ V}$ | | - | 22 | - | - | - | pF |

^[1] t_{pd} is the same as t_{PHL} and t_{PLH} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

 P_D = $C_{PD} \times V_{CC}{}^2 \times f_i \times N$ + \sum ($C_L \times V_{CC}{}^2 \times f_o$) where:

f_i = input frequency in MHz;

fo = output frequency in MHz;

C_L = output load capacitance in pF;

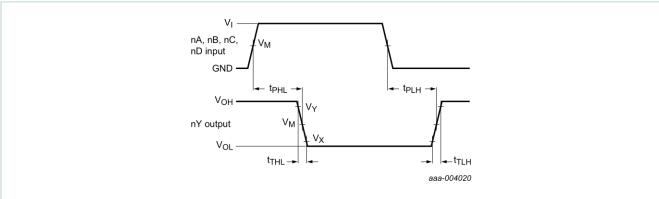
V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

^[2] t_t is the same as t_{THL} and t_{TLH} .

11. Waveforms



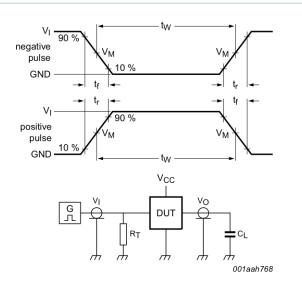
Measurement points are given in Table 8.

 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 7. Waveforms showing the input (nA, nB, nC, nD) to output (nY) propagation delays and the output transition times

Table 8. Measurement points

| Туре | Input | Output | | | | | | | |
|-----------|--------------------|--------------------|--------------------|--------------------|--|--|--|--|--|
| | V _M | V _M | V_X | V_Y | | | | | |
| 74HC4002 | 0.5V _{CC} | 0.5V _{CC} | 0.1V _{CC} | 0.9V _{CC} | | | | | |
| 74HCT4002 | 1.3 V | 1.3 V | 0.1V _{CC} | 0.9V _{CC} | | | | | |



Test data is given in Table 9.

Definitions test circuit:

 R_T = termination resistance should be equal to output impedance Z_0 of the pulse generator.

 $\ensuremath{C_L}$ = load capacitance including jig and probe capacitance.

Fig 8. Test circuit for measuring switching times

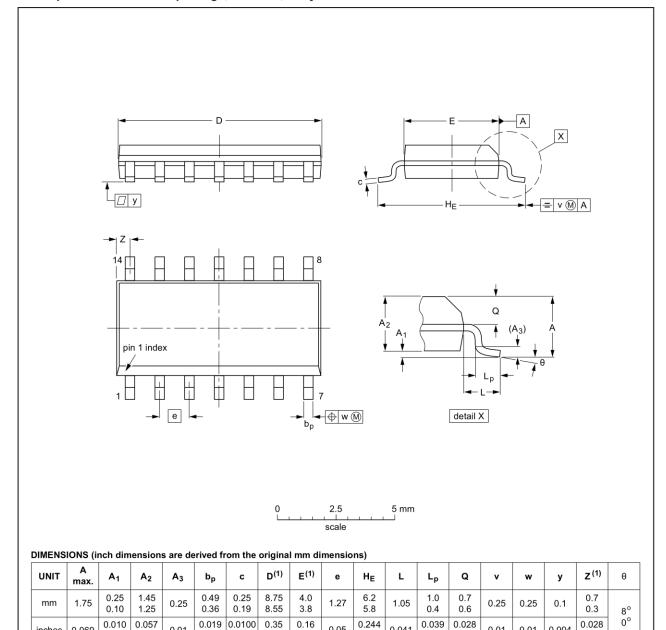
Table 9. Test data

| Туре | Input | | Load | Test |
|-----------|------------------|--------|--------------|-------------------------------------|
| | V_1 t_r, t_f | | CL | |
| 74HC4002 | V _{CC} | 6.0 ns | 15 pF, 50 pF | t _{PLH} , t _{PHL} |
| 74HCT4002 | 3.0 V | 6.0 ns | 15 pF, 50 pF | t _{PLH} , t _{PHL} |

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



inches

0.069

0.004

0.049

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

0.014 0.0075

0.34

0.15

0.01

| OUTLINE | | REFER | EUROPEAN | ISSUE DATE | | |
|-------------------------|--------|--------|----------|------------|------------|---------------------------------|
| VERSION IEC JEDEC JEITA | | | | | PROJECTION | ISSUE DATE |
| SOT108-1 | 076E06 | MS-012 | | | | 99-12-27 03-02-19 |

0.05

0.041

0.016

0.024

0.228

Package outline SOT108-1 (SO14) Fig 9.

74HC HCT4002

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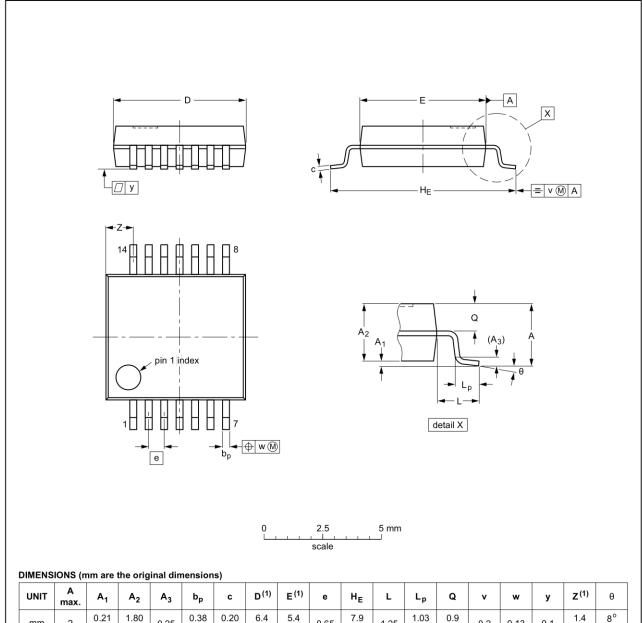
0.01

0.004

0.012

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



| UNIT | A max. | A ₁ | A ₂ | A ₃ | bp | С | D ⁽¹⁾ | E ⁽¹⁾ | е | HE | L | Lp | Q | v | w | у | Z ⁽¹⁾ | θ |
|------|-----------|----------------|----------------|----------------|--------------|--------------|------------------|------------------|------|------------|------|--------------|------------|-----|------|-----|------------------|----------|
| mm | 2 | 0.21 0.05 | 1.80 1.65 | 0.25 | 0.38 0.25 | 0.20 0.09 | 6.4 6.0 | 5.4 5.2 | 0.65 | 7.9 7.6 | 1.25 | 1.03 0.63 | 0.9 0.7 | 0.2 | 0.13 | 0.1 | 1.4 0.9 | 8° 0° |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | | REFER | EUROPEAN | ICCUE DATE | | |
|--------------------|-----|--------|----------|------------|------------|---------------------------------|
| | IEC | JEDEC | JEITA | | PROJECTION | ISSUE DATE |
| SOT337-1 | | MO-150 | | | | 99-12-27 03-02-19 |

Fig 10. Package outline SOT337-1 (SSOP14)

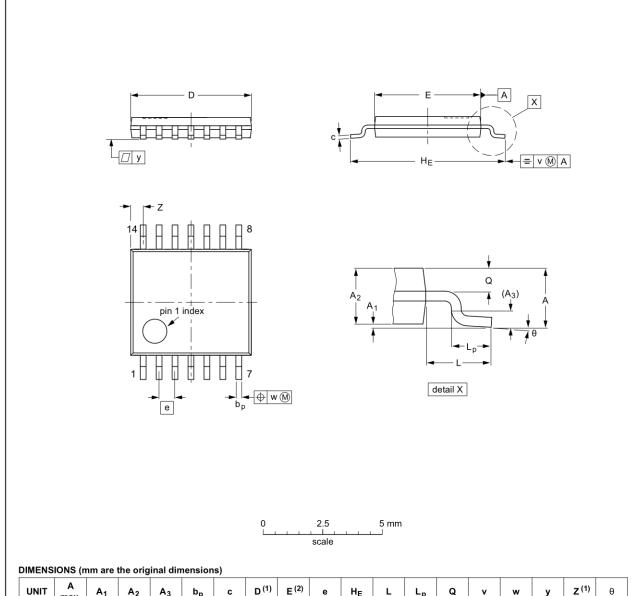
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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



| UNIT | A max. | A ₁ | A ₂ | A ₃ | bp | С | D ⁽¹⁾ | E ⁽²⁾ | e | HE | L | Lp | Q | v | w | у | Z ⁽¹⁾ | θ |
|------|-----------|----------------|----------------|----------------|--------------|------------|------------------|------------------|------|------------|---|--------------|------------|-----|------|-----|------------------|----------|
| mm | 1.1 | 0.15 0.05 | 0.95 0.80 | 0.25 | 0.30 0.19 | 0.2 0.1 | 5.1 4.9 | 4.5 4.3 | 0.65 | 6.6 6.2 | 1 | 0.75 0.50 | 0.4 0.3 | 0.2 | 0.13 | 0.1 | 0.72 0.38 | 8° 0° |

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| | REFER | EUROPEAN | ISSUE DATE | | |
|-----|--------|-----------|------------|-----------------|---------------------------------|
| IEC | JEDEC | JEITA | | PROJECTION | ISSUE DATE |
| | MO-153 | | | | 99-12-27 03-02-18 |
| | IEC | IEC JEDEC | | IEC JEDEC JEITA | IEC JEDEC JEITA PROJECTION |

Fig 11. Package outline SOT402-1 (TSSOP14)

74HC_HCT4002

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13. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|---|
| CMOS | Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| НВМ | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

14. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes | | | |
|----------------------|--|-------------------------|----------------------|----------------------|--|--|--|
| 74HC_HCT4002 v.5 | 20160526 | Product data sheet | - | 74HC_HCT4002 v.4 | | | |
| Modifications: | Type number | ers 74HC4002N and 74HC | Г4002N (SOT27-1) ren | noved. | | | |
| 74HC_HCT4002 v.4 | 20120917 | Product data sheet | - | 74HC_HCT4002 v.3 | | | |
| Modifications: | • <u>Table 1</u> : Typ | pe number 74HC20DB char | nged into 74HC4002DE | 3. | | | |
| 74HC_HCT4002 v.3 | 20120904 | Product data sheet | - | 74HC_HCT4002_CNV v.2 | | | |
| Modifications: | guidelines of NXP Semiconductors. | | | | | | |
| | Legal texts have been adapted to the new company name where appropriate. | | | | | | |
| 74HC_HCT4002_CNV v.2 | 19970829 | Product specification | - | - | | | |

15. Legal information

15.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|--------------------------------|-------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
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