HEF4069UB

Hex inverter
Rev. 8 — 16 November 2011

Product data sheet

1. **General description**

The HEF4069UB is a general purpose hex inverter. Each inverter has a single stage.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to $V_{DD},\,V_{SS},\,$ or another input.

Features and benefits 2.

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from -40 °C to +85 °C and -40 °C to +125 °C
- Complies with JEDEC standard JESD 13-B

3. Applications

Oscillator

Ordering information

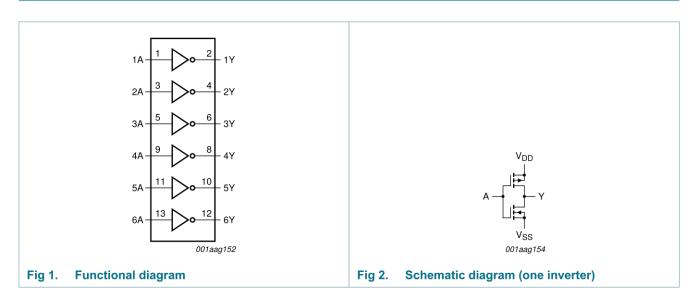
Table 1. Ordering information

All types operate from -40 °C to +125 °C.

Type number	Package		
	Name	Description	Version
HEF4069UBP	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
HEF4069UBT	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
HEF4069UBTT	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

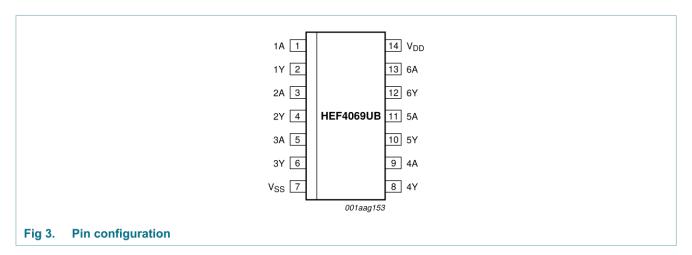


5. Functional diagram



6. Pinning information

6.1 Pinning



6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A to 6A	1, 3, 5, 9, 11, 13	input
1Y to 6Y	2, 4, 6, 8, 10, 12	output
V _{SS}	7	ground (0 V)
V_{DD}	14	supply voltage

7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+18	V
I _{IK}	input clamping current	$V_I < -0.5 \text{ V or } V_I > V_{DD} + 0.5 \text{ V}$	-	±10	mA
V_{I}	input voltage		-0.5	$V_{DD} + 0.5$	V
I _{OK}	output clamping current	$V_O < -0.5 \text{ V or } V_O > V_{DD} + 0.5 \text{ V}$	-	±10	mA
I _{I/O}	input/output current		-	±10	mA
I_{DD}	supply current		-	50	mA
T _{stg}	storage temperature		-65	+150	°C
T _{amb}	ambient temperature		-40	+125	°C
P _{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C			
		DIP14	[1] _	750	mW
		SO14	[2] _	500	mW
		TSSOP14	[3]	500	mW
Р	power dissipation	per output	-	100	mW

^[1] For DIP14 packages: above T_{amb} = 70 °C, P_{tot} derates linearly with 12 mW/K.

8. Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{DD}	supply voltage		3	-	15	V
V_{I}	input voltage		0	-	V_{DD}	V
T_{amb}	ambient temperature	in free air	-40	-	+125	°C

^[2] For SO14 packages: above T_{amb} = 70 °C, P_{tot} derates linearly with 8 mW/K.

^[3] For TSSOP14 packages: above T_{amb} = 60 °C, P_{tot} derates linearly with 5.5 mW/K.

9. Static characteristics

Table 5. Static characteristics

 $V_{SS} = 0 \ V$; $V_{I} = V_{SS} \ or \ V_{DD}$; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T _{amb} =	–40 °C	T _{amb} =	+25 °C	T _{amb} =	+85 °C	T _{amb} = -	+125 °C	Unit	
				Min	Max	Min	Max	Min	Max	Min	Max		
V_{IH}	HIGH-level	$ I_{O} < 1 \mu A$	5 V	4	-	4	-	4	-	4	-	V	
	input voltage		10 V	8	-	8	-	8	-	8	-	V	
			15 V	12.5	-	12.5	-	12.5	-	12.5	-	V	
V _{IL}	LOW-level	$ I_{O} < 1 \mu A$	5 V	-	1	-	1	-	1	-	1	V	
	input voltage		10 V	-	2	-	2	-	2	-	2	V	
			15 V	-	2.5	-	2.5	-	2.5	-	2.5	V	
V_{OH}	HIGH-level	$ I_{O} < 1 \mu A$	5 V	4.95	-	4.95	-	4.95	-	4.95	-	V	
	output voltage		10 V	9.95	-	9.95	-	9.95	-	9.95	-	V	
			15 V	14.95	-	14.95	-	14.95	-	14.95	-	V	
V _{OL}	LOW-level	$ I_{O} < 1 \mu A$	5 V	-	0.05	-	0.05	-	0.05	-	0.05	V	
	output voltage		10 V	-	0.05	-	0.05	-	0.05	-	0.05	V	
			15 V	-	0.05	-	0.05	-	0.05	-	0.05	V	
I _{OH}	HIGH-level		$V_0 = 2.5 V$	5 V	-	-1.7	-	-1.4	-	-1.1	-	-1.1	mA
	output current	$V_0 = 4.6 \text{ V}$	5 V	-	-0.64	-	-0.5	-	-0.36	-	-0.36	mA	
		$V_{O} = 9.5 \ V$	10 V	-	-1.6	-	-1.3	-	-0.9	-	-0.9	mΑ	
		V _O = 13.5 V	15 V	-	-4.2	-	-3.4	-	-2.4	-	-2.4	mA	
I _{OL}	LOW-level	$V_0 = 0.4 \ V$	5 V	0.64	-	0.5	-	0.36	-	0.36	-	mΑ	
	output current	$V_{O} = 0.5 \ V$	10 V	1.6	-	1.3	-	0.9	-	0.9	-	mA	
		V _O = 1.5 V	15 V	4.2	-	3.4	-	2.4	-	2.4	-	mA	
II	input leakage current		15 V	-	±0.1	-	±0.1	-	±1.0	-	±1.0	μА	
I _{DD}	supply current		5 V	-	0.25	-	0.25	-	7.5	-	7.5	μΑ	
		combinations;	10 V	-	0.5	-	0.5	-	15.0	-	15.0	μА	
		$I_O = 0 A$	15 V	-	1.0	-	1.0	-	30.0	-	30.0	μΑ	
C _I	input capacitance	digital inputs		-	-	-	7.5	-	-	-	-	pF	

10. Dynamic characteristics

Table 6. Dynamic characteristics

 T_{amb} = 25 °C; for waveforms see Figure 4; for test circuit see Figure 5.

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula[1]	Min	Тур	Max	Unit
t _{PHL}	HIGH to LOW	nA to nY;	5 V	18 ns + (0.55 ns/pF)C _L	-	45	90	ns
	propagation delay		10 V	9 ns + (0.23 ns/pF)C _L	-	20	40	ns
			10 V 15 V 15	7 ns + (0.16 ns/pF)C _L	-	15	25	ns
t _{PLH}	LOW to HIGH	nA to nY	5 V	13 ns + (0.55 ns/pF)C _L	-	40	80	ns
	propagation delay		10 V	9 ns + (0.23 ns/pF)C _L	-	20	40	ns
			15 V	7 ns + (0.16 ns/pF)C _L	-	15	30	ns
t_{THL}	HIGH to LOW output	output nY	5 V	10 ns + (1.00 ns/pF)C _L	-	60	120	ns
	transition time		10 V	9 ns + (0.42 ns/pF)C _L	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF)C _L	-	20	40	ns
t _{TLH}	LOW to HIGH output	output nY	5 V	10 ns + (1.00 ns/pF)C _L	-	60	120	ns
	transition time		10 V	9 ns + (0.42 ns/pF)C _L	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF)C _L	-	20	40	ns

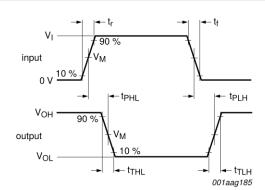
^[1] The typical value of the propagation delay and output transition time can be calculated with the extrapolation formula (C_L in pF).

Table 7. Dynamic power dissipation

 $V_{SS} = 0 \ V; \ t_r = t_f \le 20 \ ns; \ T_{amb} = 25 \ ^{\circ}C.$

Symbol	Parameter	V_{DD}	Typical formula	Where
P_D	dynamic power dissipation	5 V	$P_D = 600 \times f_i + \Sigma (f_o \times C_L) \times V_{DD}^2 (\mu W)$	f _i = input frequency in MHz;
		10 V	$P_D = 4000 \times f_i + \Sigma (f_o \times C_L) \times V_{DD}^2 (\mu W)$	fo = output frequency in MHz;
		15 V	$P_D = 22000 \times f_i + \Sigma (f_o \times C_L) \times V_{DD}^2 (\mu W)$	C_L = output load capacitance in pF;
				$\Sigma(f_0 \times C_L)$ = sum of the outputs;
				V _{DD} = supply voltage in V.

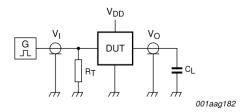
11. Waveforms



Measurement points: $V_M = 0.5V_{DD}$.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 4. Propagation delay and transition times



Definitions for test circuit:

C_L = load capacitance including jig and probe capacitance;

 R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator;

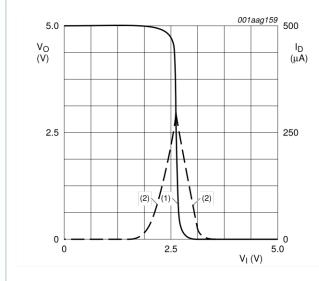
For test data refer to Table 8.

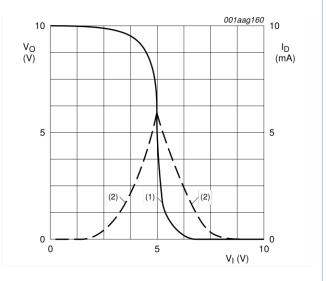
Fig 5. Test circuit for measuring switching times

Table 8. Test data

Supply voltage	Input	Input L					
V_{DD}	VI	t _r , t _f	CL				
5 V to 15 V	V_{SS} or V_{DD}	≤ 20 ns	50 pF				

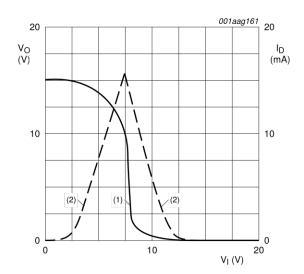
11.1 Transfer characteristics





a.
$$V_{DD} = 5 \text{ V}$$
; $I_{O} = 0 \text{ A}$





- c. $V_{DD} = 15 \text{ V}; I_{O} = 0 \text{ A}$
- (1) V_O = output voltage.
- (2) I_D = drain current.

Fig 6. Typical transfer characteristics

12. Application information

Some examples of applications for the HEF4069UB.

<u>Figure 7</u> shows an astable relaxation oscillator using two HEF4069UB inverters and 2 BAW62 diodes. The oscillation frequency is mainly determined by R1 \times C1, provided R1 << R2 and R2 \times C2 << R1 \times C1.

The function of R2 is to minimize the influence of the forward voltage across the protection diodes on the frequency; C2 is a stray (parasitic) capacitance.

The period T_p is given by $T_p = T_1 + T_2$,

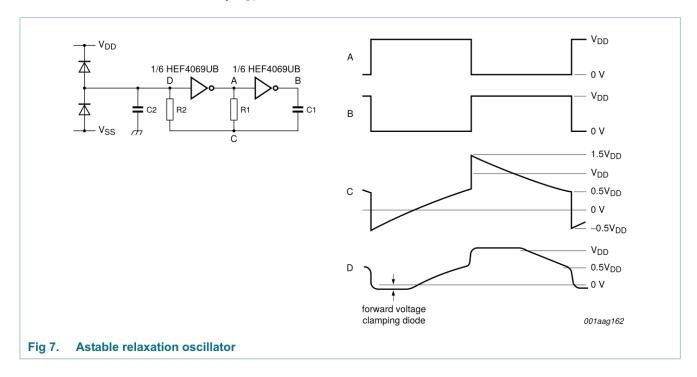
where:

$$T_{I} = R1C1In \frac{V_{DD} + V_{ST}}{V_{ST}}$$

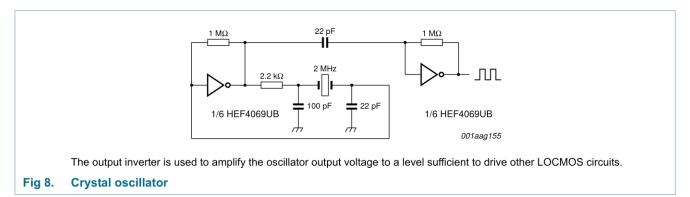
$$T_2 = RICIIn \frac{2V_{DD} - V_{ST}}{V_{DD} - V_{ST}}$$

 V_{ST} = the signal threshold level of the inverter.

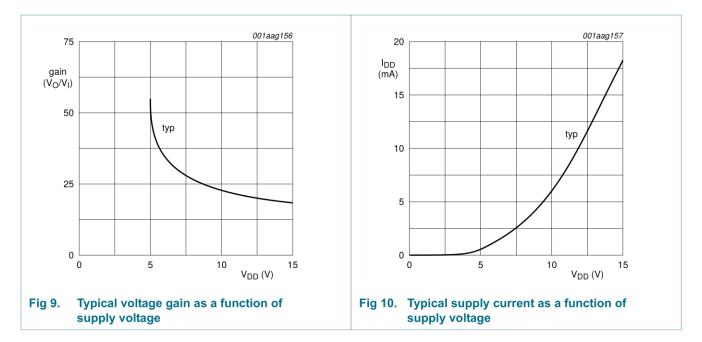
The period is fairly independent of V_{DD} , V_{ST} and temperature. The duty factor, however, is influenced by V_{ST} .

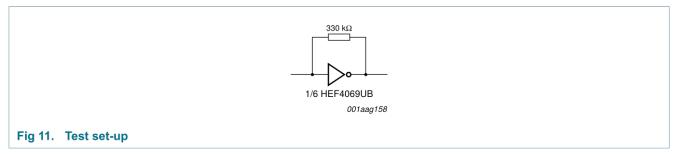


<u>Figure 8</u> shows a crystal oscillator for frequencies up to 10 MHz using two HEF4069UB inverters. The second inverter amplifies the oscillator output voltage to a level sufficient to drive other Local Oxidation CMOS (LOCMOS) circuits.



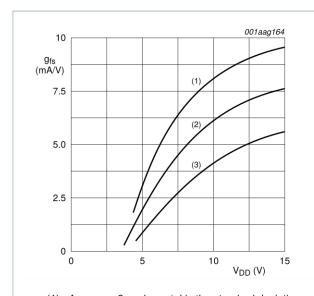
<u>Figure 9</u> and <u>Figure 10</u> show voltage gain and supply current. <u>Figure 11</u> shows the test set-up and an example of an analog amplifier using one HEF4069UB.





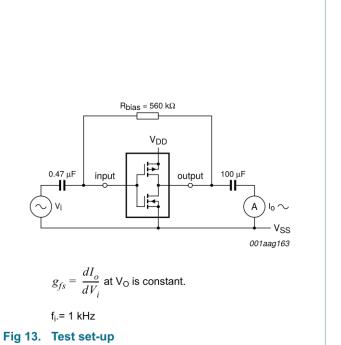
HEF4069UB

Figure 12 shows typical forward transconductance and Figure 13 shows the test set-up.



- (1) Average +2 σ ; where: ' σ ' is the standard deviation.
- (2) Average.
- (3) Average -2σ ; where: ' σ ' is the standard deviation.

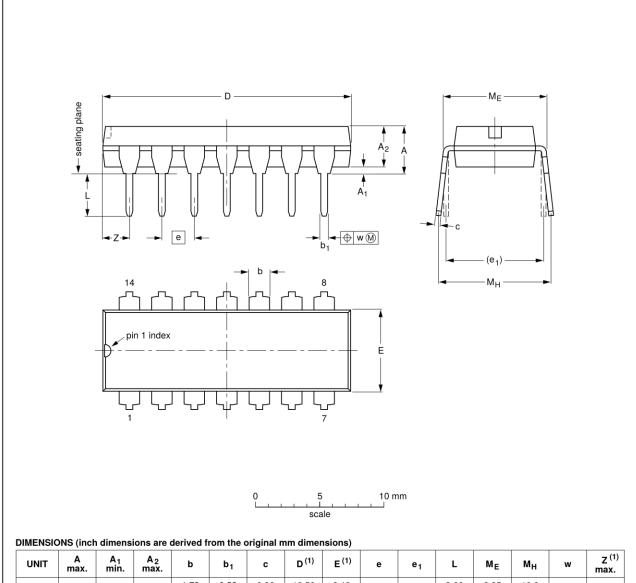
Fig 12. Typical forward transconductance as a function of supply voltage at T_{amb} = 25 °C



13. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	С	D ⁽¹⁾	E ⁽¹⁾	е	e ₁	L	ME	Мн	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.02	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE		REFER	RENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT27-1	050G04	MO-001	SC-501-14		99-12-27 03-02-13

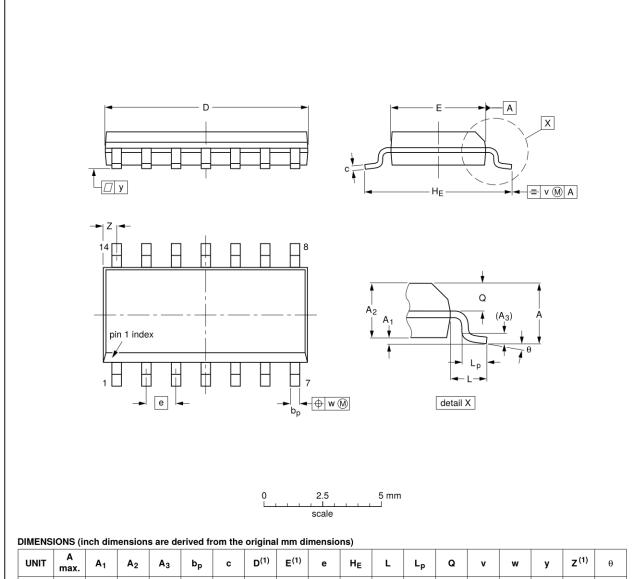
Fig 14. Package outline SOT27-1 (DIP14)

HEF4069UB

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SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



UNIT	A max.	Α1	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01		0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	0°

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE		REFER	RENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	1330E DATE
SOT108-1	076E06	MS-012			99-12-27 03-02-19

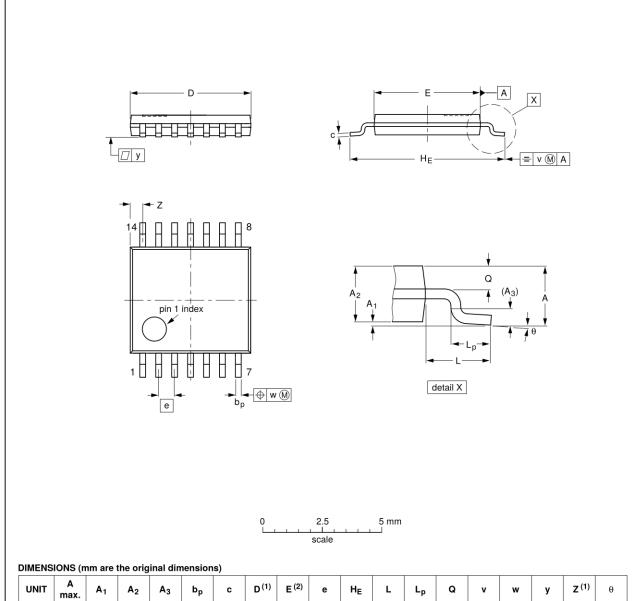
Fig 15. Package outline SOT108-1 (SO14)

HEF4069UB

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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E (2)	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

		EUROPEAN	ISSUE DATE			
IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
	MO-153				99-12-27 03-02-18	
	IEC				IEC JEDEC JEHA	

Fig 16. Package outline SOT402-1 (TSSOP14)

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14. Revision history

Table 9. Revision history

	•			
Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4069UB v.8	20111116	Product data sheet	-	HEF4069UB v.7
Modifications:	 Legal pages 	s updated.		
	 Changes in 	"General description", "Feat	tures and benefits" and	"Applications".
HEF4069UB v.7	20110511	Product data sheet	-	HEF4069UB v.6
HEF4069UB v.6	20091208	Product data sheet	-	HEF4069UB v.5
HEF4069UB v.5	20090723	Product data sheet	-	HEF4069UB v.4
HEF4069UB v.4	20080704	Product data sheet	-	HEF4069UB_CNV v.3
HEF4069UB_CNV v.3	19950101	Product specification	-	HEF4069UB_CNV v.2
HEF4069UB_CNV v.2	19950101	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design
- [2] The term 'short data sheet' is explained in section "Definitions"
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17. Contents

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