



PESD3V3S2UT

Double ESD protection diode

11 April 2023

Product data sheet

1. General description

Uni-directional double ESD protection diode in a SOT23 plastic package. Designed to protect up to two transmission or data lines from ElectroStatic Discharge (ESD) damage.

2. Features and benefits

- Uni-directional ESD protection of up to two lines
- Max. peak pulse power: $P_{pp} = 330 \text{ W}$ at $t_p = 8/20 \text{ us}$
- Low clamping voltage: $V_{(CL)R} = 20 \text{ V}$ at $I_{pp} = 18 \text{ A}$
- Ultra-low reverse leakage current: $I_{RM} < 700 \text{ nA}$
- ESD protection $> 30 \text{ kV}$
- IEC 61000-4-2; level 4 (ESD)
- IEC 61000-4-5 (surge); $I_{pp} = 18 \text{ A}$ at $t_p = 8/20 \text{ us}$.

3. Applications

- Computers and peripherals
- Communication systems
- Audio and video equipment
- High speed data lines
- Parallel ports

4. Quick reference data

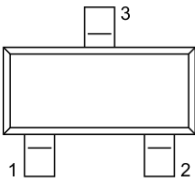
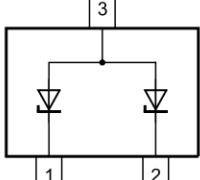
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	$T_{amb} = 25 \text{ }^{\circ}\text{C}$	[1]	-	-	3.3	V
C_d	diode capacitance	$f = 1 \text{ MHz}$; $V_R = 0 \text{ V}$; $T_{amb} = 25 \text{ }^{\circ}\text{C}$	[1]	-	207	300	pF

[1] Measured from pin 1 or 2 to pin 3.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)	 SOT23	 006aaa154
2	K2	cathode (diode 2)		
3	A	common anode		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD3V3S2UT	SOT23	plastic, surface-mounted package; 3 terminals; 1.9 mm pitch; 2.9 mm x 1.3 mm x 1 mm body	SOT23

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PESD3V3S2UT	%U9

[1] % = placeholder for manufacturing site code

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
P _{PPM}	rated peak pulse power	t _p = 8/20 μs	[1] [2]	-	330	W
I _{PPM}	rated peak pulse current		[1] [2]	-	18	A
T _j	junction temperature			-	150	°C
T _{amb}	ambient temperature			-65	150	°C
T _{stg}	storage temperature			-65	150	°C
ESD maximum ratings						
V _{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (contact discharge)	[3] [2]	-	30	kV
		IEC 61000-4-2 (air discharge)	[3] [2]	-	15	kV
		MIL-STD-883 (human body model)		-	10	kV

- [1] Non-repetitive current pulse 8/20 μs exponential decay waveform according to IEC 61000-4-5.
[2] Measured from pin 1 or 2 to pin 3.
[3] Device stressed with ten non-repetitive ESD pulses.

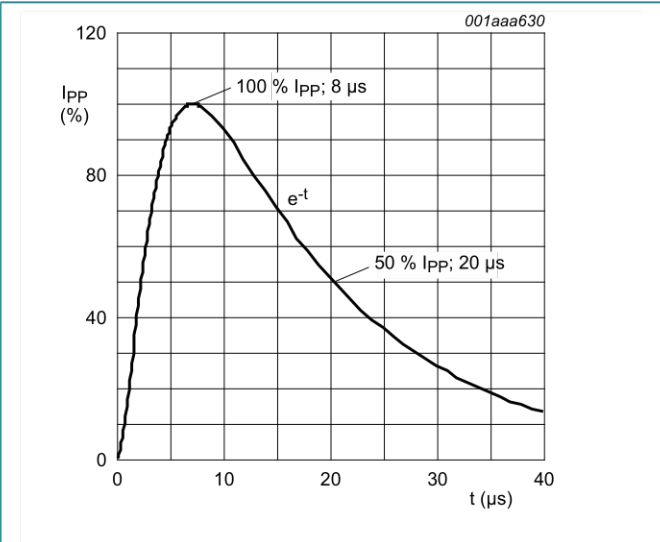


Fig. 1. 8/20 μs pulse waveform according to IEC 61000-4-5

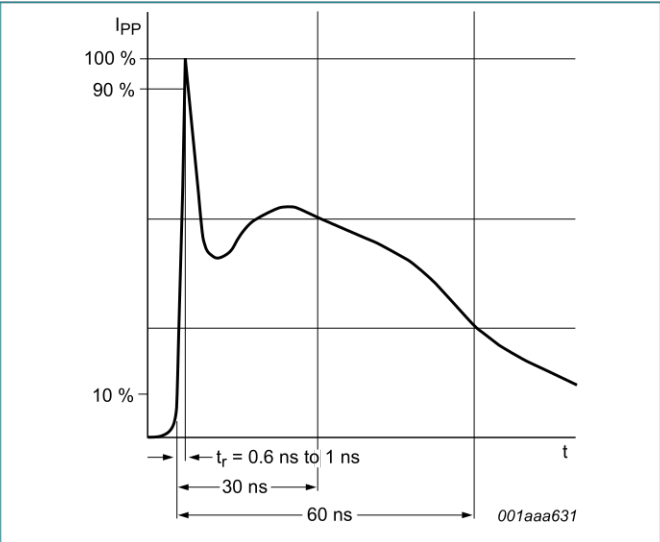


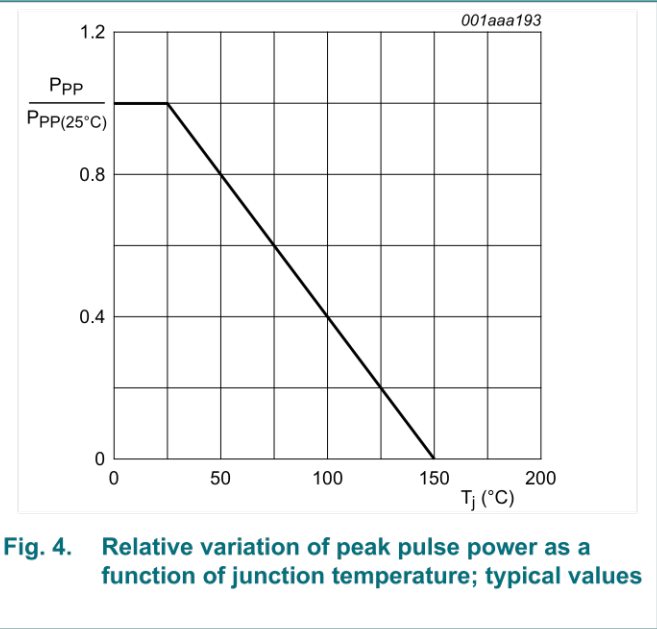
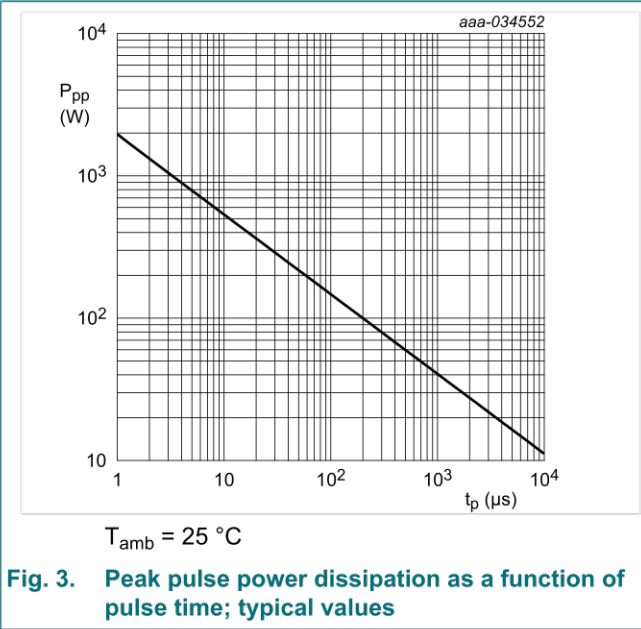
Fig. 2. ESD pulse waveform according to IEC 61000-4-2

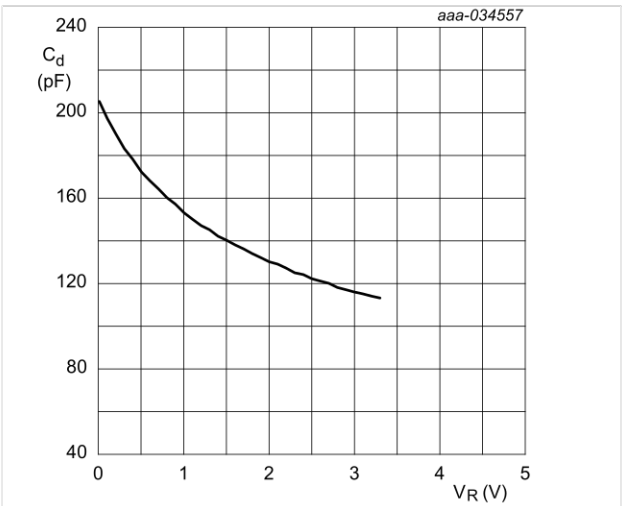
9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{RWM}	reverse standoff voltage	T _{amb} = 25 °C	[1]	-	-	3.3	V
V _{BR}	breakdown voltage	I _R = 5 mA; T _{amb} = 25 °C	[1]	5.2	5.6	6	V
I _{RM}	reverse leakage current	V _{RWM} = 3.3 V; T _{amb} = 25 °C	[1]	-	0.7	2	μA
C _d	diode capacitance	f = 1 MHz; V _R = 0 V; T _{amb} = 25 °C	[1]	-	207	300	pF
V _{CL}	clamping voltage	I _{PP} = 1 A; T _{amb} = 25 °C	[1] [2]	-	-	7	V
		I _{PP} = 18 A; T _{amb} = 25 °C	[1] [2]	-	-	20	V
R _{diff}	differential resistance	I _R = 1 mA; T _{amb} = 25 °C	[1]	-	-	400	Ω

- [1] Measured from pin 1 or 2 to pin 3.
[2] Non-repetitive current pulse 8/20 μs exponential decay waveform according to IEC 61000-4-5.





$f = 1\text{ MHz}; T_{\text{amb}} = 25\text{ °C}$

Fig. 5. Diode capacitance as a function of reverse voltage; typical values

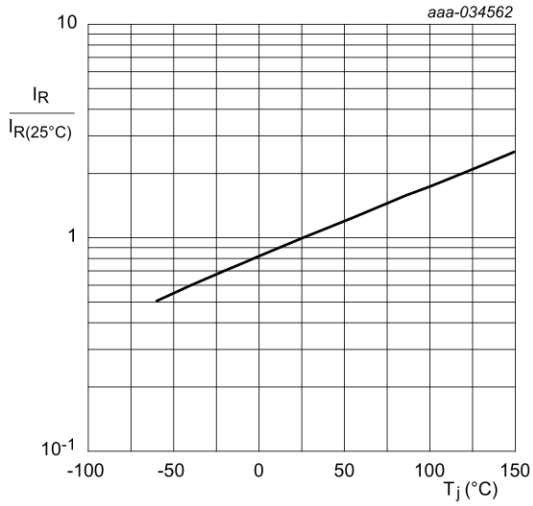
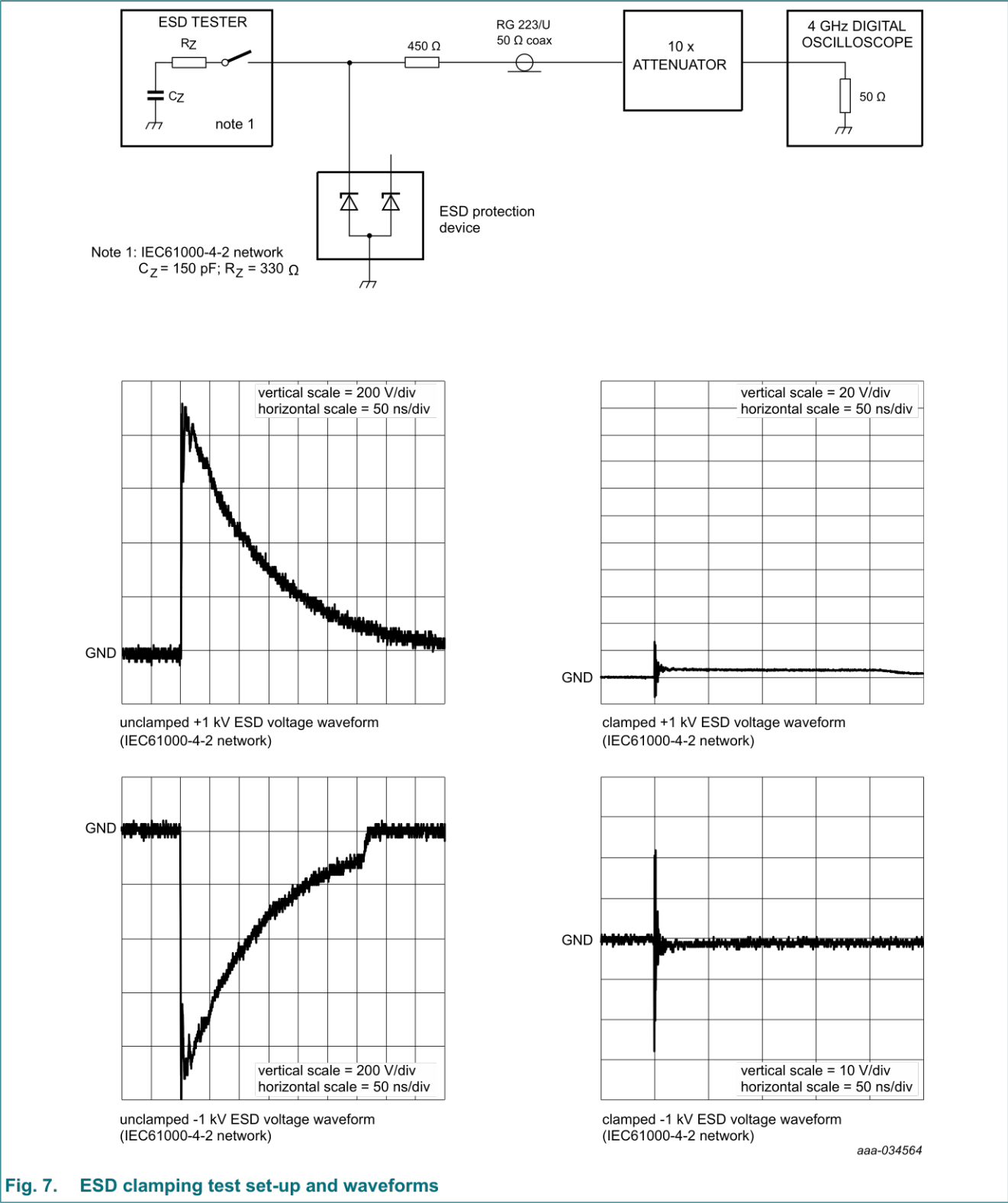


Fig. 6. Relative variation of reverse leakage current as a function of junction temperature; typical values



10. Application information

The device is designed for the protection of up to two unidirectional data or signal lines from the damage caused by ESD and surge pulses. The devices may be used on lines where the signal polarities are either positive or negative with respect to ground.

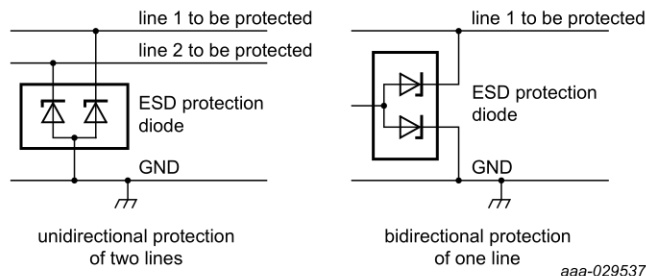


Fig. 8. Application diagram

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Package outline

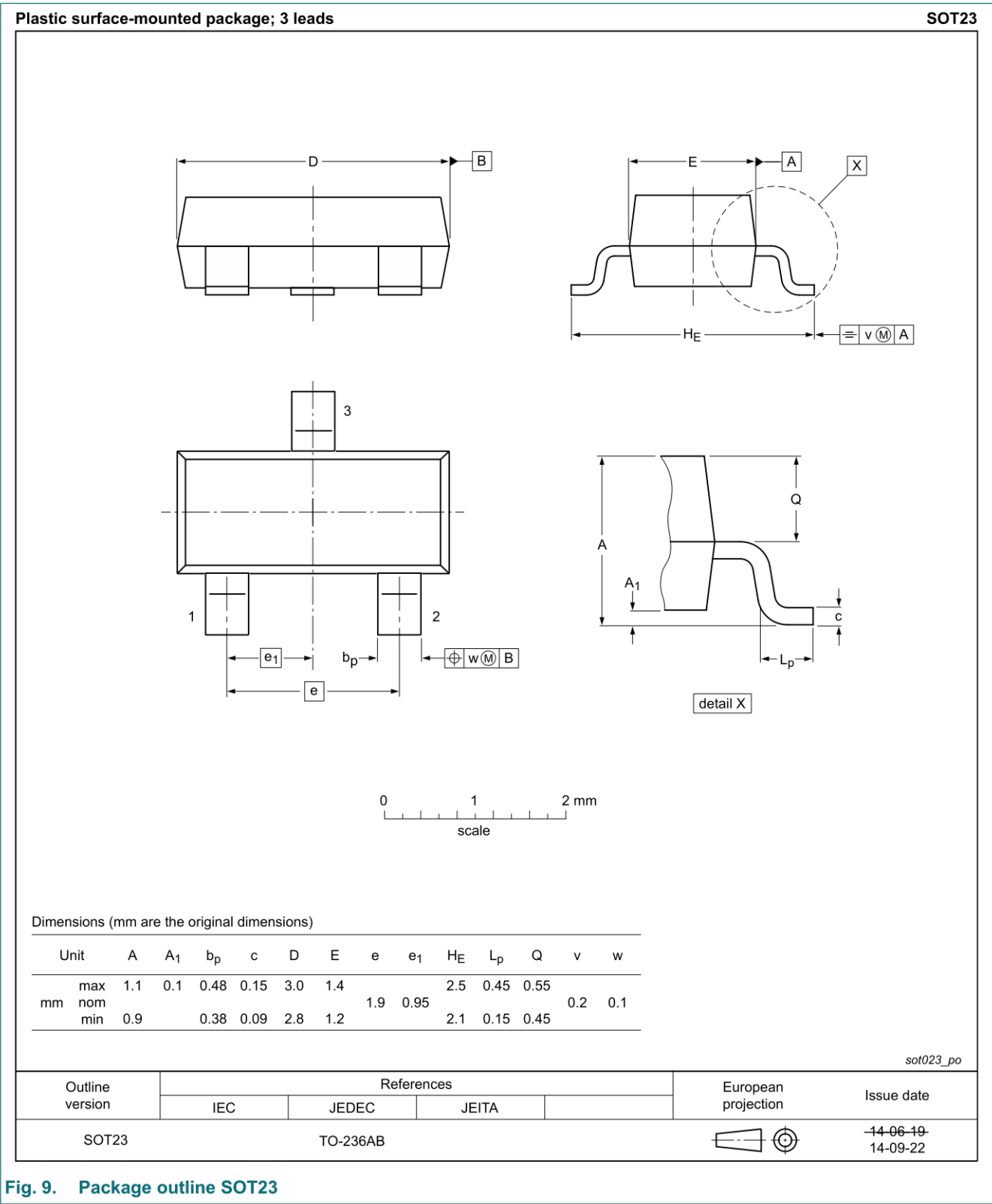


Fig. 9. Package outline SOT23

12. Soldering

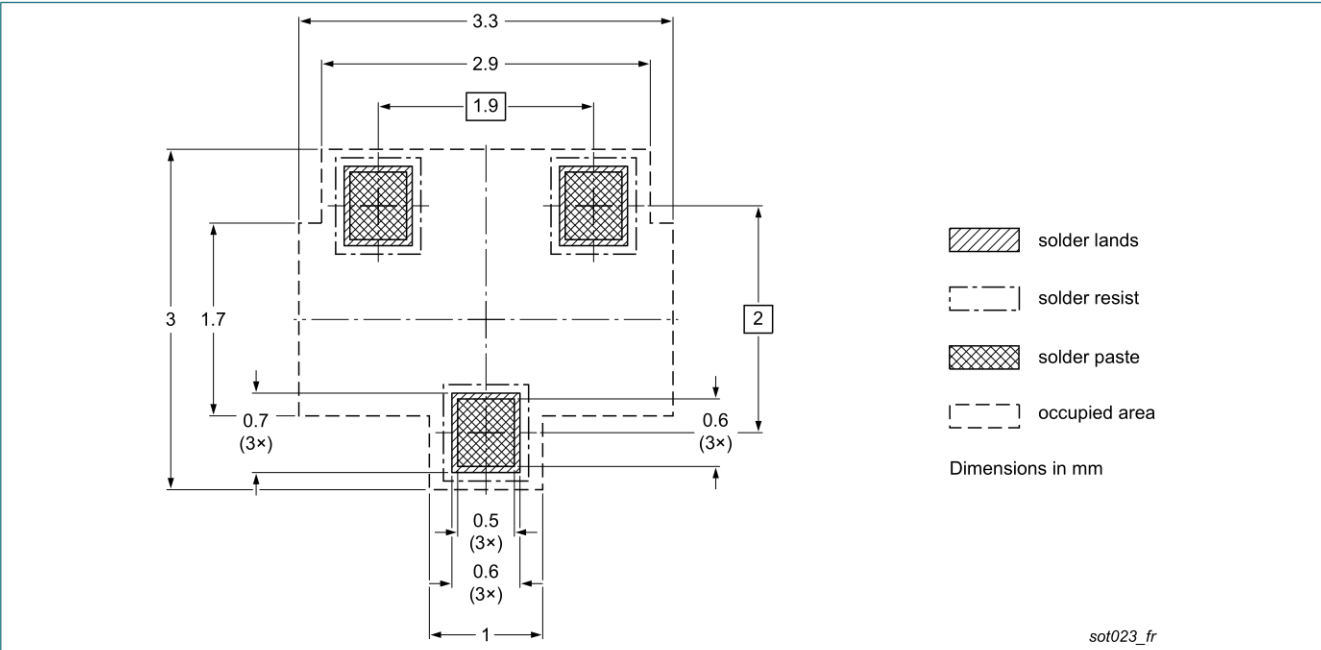


Fig. 10. Reflow soldering footprint for SOT23

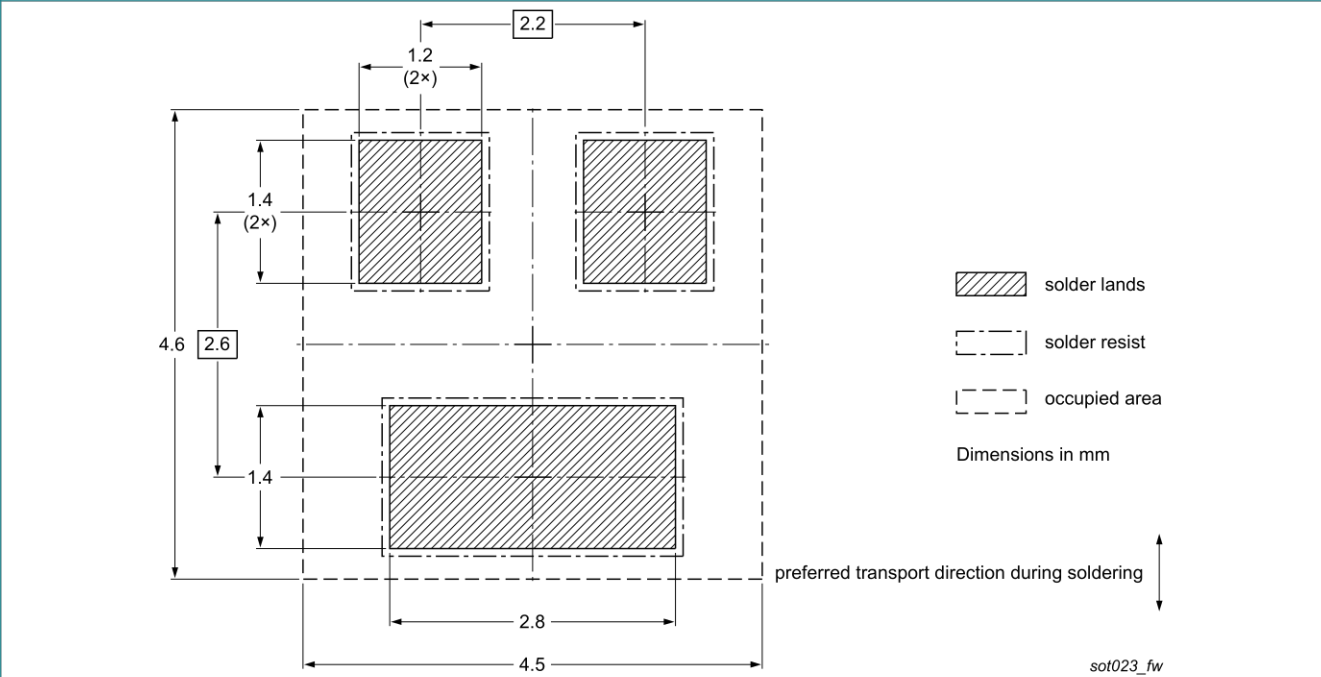


Fig. 11. Wave soldering footprint for SOT23

13. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD3V3S2UT v.3	20230411	Product data sheet	-	PESDXS2UT_SERIES v.2
Modifications:	- Product changed to non-automotive qualification. Please refer to nexperia.com for automotive(-Q) product alternative(s). - Family data sheet reduced to single type data sheet			
PESDXS2UT_SERIES v.2	20040415	Product data sheet	-	PESDXS2UT_SERIES v.1
PESDXS2UT_SERIES v.1	20030820	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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Contents

1. General description..... 1

2. Features and benefits..... 1

3. Applications..... 1

4. Quick reference data..... 1

5. Pinning information.....2

6. Ordering information.....2

7. Marking.....2

8. Limiting values..... 3

9. Characteristics.....4

10. Application information..... 7

11. Package outline..... 8

12. Soldering..... 9

13. Revision history.....10

14. Legal information.....11

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