

Single D Flip Flop

NL17SZ74

The NL17SZ74 is a high performance, full function Edge triggered D Flip Flop, with all the features of a standard logic device such as the 74LCX74.

Features

- Designed for 1.65 V to 5.5 V V_{CC} Operation
- 2.6 ns t_{PD} at $V_{CC} = 5$ V (typ)
- Inputs/Outputs Overvoltage Tolerant up to 5.5 V
- I_{OFF} Supports Partial Power Down Protection
- Source/Sink 24 mA at 3.0 V
- Available in US8, UDFN8 and UQFN8 Packages
- Chip Complexity < 100 FETs
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

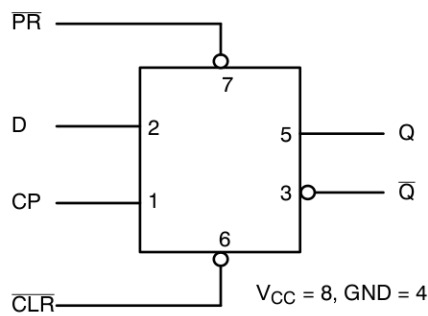

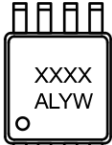

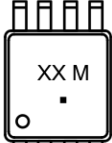

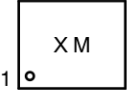



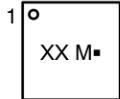


Figure 1. Logic Symbol



www.onsemi.com

MARKING DIAGRAMS		
	US8 US SUFFIX CASE 493	 Commercial
	UDFN8, 1.45x1.0 MU3 SUFFIX CASE 517BZ	 NLV Prefix
	UDFN8, 1.95x1.0 MU1 SUFFIX CASE 517CA	
	UQFN8, 1.4x1.2 MQ2 SUFFIX CASE 523AS	
	UQFN8, 1.6x1.6 MQ1 SUFFIX CASE 523AN	

X, XX, XXXX = Specific Device Code
 A = Assembly Location
 L = Lot Code
 Y = Year Code
 W = Week Code
 M = Date Code
 ■ = Pb-Free Package

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 8 of this data sheet.

NL17SZ74

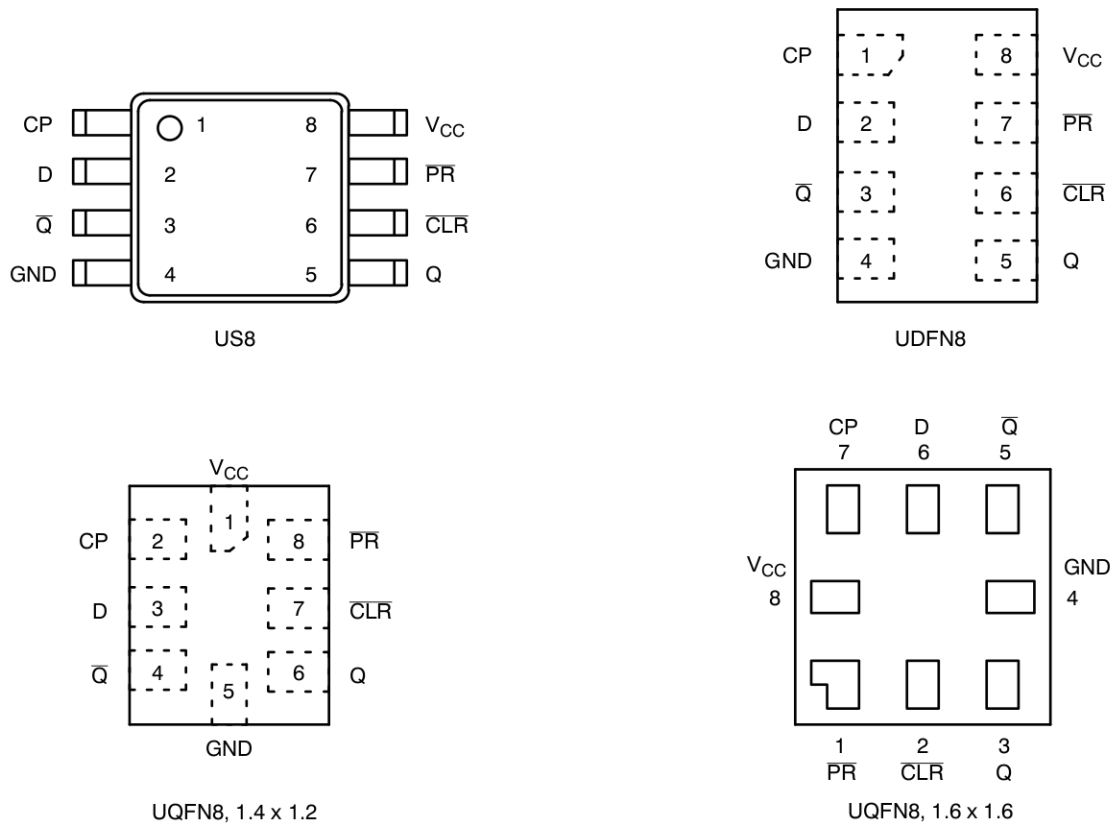


Figure 2. Pinout (Top View)

PIN ASSIGNMENT

Pin	US8	UDFN8	UQFN8, 1.4x1.2	UQFN8, 1.6x1.6
1	CP	CP	V_{CC}	\bar{PR}
2	D	D	CP	\bar{CLR}
3	\bar{Q}	\bar{Q}	D	Q
4	GND	GND	\bar{Q}	GND
5	Q	Q	GND	\bar{Q}
6	\bar{CLR}	\bar{CLR}	Q	D
7	PR	PR	\bar{CLR}	CP
8	V_{CC}	V_{CC}	\bar{PR}	V_{CC}

FUNCTION TABLE

Inputs				Outputs		Operating Mode
PR	CLR	CP	D	Q	\bar{Q}	
L	H	X	X	H	L	Asynchronous Set Asynchronous Clear Underdetermined
H	L	X	X	L	H	
L	L	X	X	H	H	
H	H	\uparrow	h	H	L	Load and Read Register
H	H	\uparrow	l	L	H	
H	H	\uparrow	X	NC	NC	Hold

H = High Voltage Level
 h = High Voltage Level One Setup Time Prior to Low-to-High Clock Transition
 L = Low Voltage Level
 l = Low Voltage Level One Setup Time Prior to Low-to-High Clock Transition
 NC = No Change
 X = High or Low Voltage Level and Transitions are Acceptable
 \uparrow = Low-to-High Transition
 \uparrow = Low-to-High Transition
 For I_{CC} reasons, DO NOT FLOAT Inputs

NL17SZ74

MAXIMUM RATINGS

Symbol	Characteristics	Value	Unit
V _{CC}	DC Supply Voltage	NLV -0.5 to +7.0 -0.5 to +6.5	V
V _{IN}	DC Input Voltage	NLV -0.5 to +7.0 -0.5 to +6.5	V
V _{OUT}	DC Output Voltage (NLV)	Active-Mode (High or Low State) Tri-State Mode (Note 6) Power-Down Mode (V _{CC} = 0 V)	-0.5 to V _{CC} + 0.5 -0.5 to +7.0 -0.5 to +7.0
	DC Output Voltage	Active-Mode (High or Low State) Tri-State Mode (Note 6) Power-Down Mode (V _{CC} = 0 V)	-0.5 to V _{CC} + 0.5 -0.5 to +6.5 -0.5 to +6.5
I _{IK}	DC Input Diode Current	V _{IN} < GND	-50 mA
I _{OK}	DC Output Diode Current	V _{OUT} < GND	-50 mA
I _{OUT}	DC Output Source/Sink Current		±50 mA
I _{CC} or I _{GND}	DC Supply Current per Supply Pin or Ground Pin		±100 mA
T _{STG}	Storage Temperature Range		-65 to +150 °C
T _L	Lead Temperature, 1 mm from Case for 10 secs		260 °C
T _J	Junction Temperature Under Bias		+150 °C
θ _{JA}	Thermal Resistance (Note 7)	US8 UQFN8 UDFN8	250 210 231 °C/W
P _D	Power Dissipation in Still Air	US8 UQFN8 UDFN8	500 595 541 mW
MSL	Moisture Sensitivity		Level 1 -
F _R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in -
V _{ESD}	ESD Withstand Voltage (Note 8)	Human Body Model Charged Device Model	2000 1000 V
I _{Latchup}	Latchup Performance (Note 9)		±100 mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri-stated.
2. Measured with minimum pad spacing on an FR4 board, using 10mm-by-1inch, 2 ounce copper trace no air flow per JESD51-7.
3. HBM tested to ANSI/ESDA/JEDEC JS-001-2017. CDM tested to EIA/JESD22-C101-F. JEDEC recommends that ESD qualification to EIA/JESD22-A115-A (Machine Model) be discontinued per JEDEC/JEP172A.
4. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit	
V _{CC}	Positive DC Supply Voltage	1.65	5.5	V	
V _{IN}	DC Input Voltage	0	5.5	V	
V _{OUT}	DC Output Voltage	Active-Mode (High or Low State)	0	V _{CC}	
		Tri-State Mode (Note 6)	0	5.5	
		Power-Down Mode (V _{CC} = 0 V)	0	5.5	
T _A	Operating Temperature Range	-55	+125	°C	
	Input Rise and Fall Time	V _{CC} = 1.65 V to 1.95 V	0		20
		V _{CC} = 2.3 V to 2.7 V	0		20
		V _{CC} = 3.0 V to 3.6 V	0		10
		V _{CC} = 4.5 V to 5.5 V	0		5

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

NL17SZ74

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			-55°C ≤ T _A ≤ 125°C		Units
				Min	Typ	Max	Min	Max	
V _{IH}	High-Level Input Voltage		1.65 to 1.95	0.65 V _{CC}	-	-	0.65 V _{CC}	-	V
			2.3 to 5.5	0.70 V _{CC}	-	-	0.70 V _{CC}	-	
V _{IL}	Low-Level Input Voltage		1.65 to 1.95	-	-	0.35 V _{CC}	-	0.35 V _{CC}	V
			2.3 to 5.5	-	-	0.30 V _{CC}	-	0.30 V _{CC}	
V _{OH}	High-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OH} = -100 μA I _{OH} = -4 mA I _{OH} = -8 mA I _{OH} = -12 mA I _{OH} = -16 mA I _{OH} = -24 mA I _{OH} = -32 mA	1.65 to 5.5	V _{CC} - 0.1	V _{CC}	-	V _{CC} - 0.1	-	V
			1.65	1.29	1.4	-	1.29	-	
			2.3	1.9	2.1	-	1.9	-	
			2.7	2.2	2.4	-	2.2	-	
			3.0	2.4	2.7	-	2.4	-	
			3.0	2.3	2.5	-	2.3	-	
			4.5	3.8	4.0	-	3.8	-	
V _{OL}	Low-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OL} = 100 μA I _{OL} = 4 mA I _{OL} = 8 mA I _{OL} = 12 mA I _{OL} = 16 mA I _{OL} = 24 mA I _{OL} = 32 mA	1.65 to 5.5	-	-	0.1	-	0.1	V
			1.65	-	0.08	0.24	-	0.24	
			2.3	-	0.2	0.3	-	0.3	
			2.7	-	0.22	0.4	-	0.4	
			3.0	-	0.28	0.4	-	0.4	
			3.0	-	0.38	0.55	-	0.55	
			4.5	-	0.42	0.55	-	0.55	
I _{IN}	Input Leakage Current	V _{IN} = 5.5 V or GND	1.65 to 5.5	-	-	±0.1	-	±1.0	μA
I _{OFF}	Power Off Leakage Current	V _{IN} = 5.5 V or V _{OUT} = 5.5 V	0	-	-	1.0	-	10	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5	-	-	1.0	-	10	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NL17SZ74

AC ELECTRICAL CHARACTERISTICS

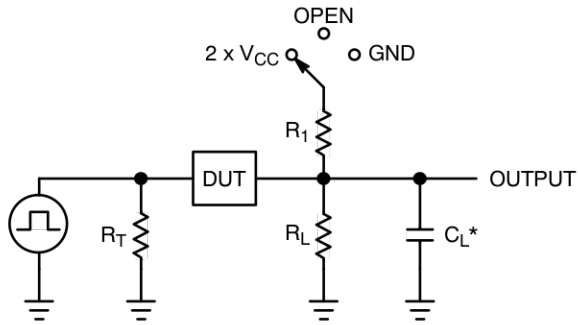
Symbol	Parameter	V _{CC} (V)	Test Conditions	T _A = 25°C			T _A = -55 to 125°C		Units
				Min	Typ	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency (50% Duty Cycle) (Waveform 1)	1.65 to 1.95	C _L = 15 pF R _L = 1 MΩ S ₁ = Open	75	-	-	75	-	MHz
		2.3 to 2.7		150	-	-	150	-	
		3.0 to 3.6		200	-	-	200	-	
		4.5 to 5.5		250	-	-	250	-	
		3.0 to 3.6	C _L = 50 pF, R _L = 500 Ω, S ₁ = Open	175	-	-	175	-	
		4.5 to 5.5		200	-	-	200	-	
t _{PLH} , t _{PHL}	Propagation Delay, CP to Q or Q (Waveform 1)	1.65 to 1.95	C _L = 15 pF R _L = 1 MΩ S ₁ = Open	-	6.5	12.5	-	13	ns
		2.3 to 2.7		-	3.8	7.5	-	8.0	
		3.0 to 3.6		-	2.8	6.5	-	7.0	
		4.5 to 5.5		-	2.2	4.5	-	5.0	
		3.0 to 3.6	C _L = 50 pF, R _D = 500 Ω, S ₁ = Open	-	3.4	7.0	-	7.5	
		4.5 to 5.5		-	2.6	5.0	-	5.5	
t _{PLH} , t _{PHL}	Propagation Delay, PR or CLR to Q or Q (Waveform 2)	1.65 to 1.95	C _L = 15 pF R _L = 1 MΩ S ₁ = Open	-	6.5	14	-	14.5	ns
		2.3 to 2.7		-	3.8	9.0	-	9.5	
		3.0 to 3.6		-	2.8	6.5	-	7.0	
		4.5 to 5.5		-	2.2	5.0	-	5.5	
		3.0 to 3.6	C _L = 50 pF, R _L = 500 Ω, S ₁ = Open	-	3.4	7.0	-	7.5	
		4.5 to 5.5		-	2.6	5.0	-	5.5	
t _S	Setup Time, D to CP (Waveform 1)	1.65 to 1.95	C _L = 15 pF R _L = 1 MΩ S ₁ = Open	6.5	-	-	6.5	-	ns
		2.3 to 2.7		3.5	-	-	3.5	-	
		3.0 to 3.6		2.0	-	-	2.0	-	
		4.5 to 5.5		1.5	-	-	1.5	-	
		3.0 to 3.6	C _L = 50 pF, R _L = 500 Ω, S ₁ = Open	2.0	-	-	2.0	-	
		4.5 to 5.5		1.5	-	-	1.5	-	
t _H	Hold Time, D to CP (Waveform 1)	1.65 to 1.95	C _L = 15 pF R _L = 1 MΩ S ₁ = Open	0.5	-	-	0.5	-	ns
		2.3 to 2.7		0.5	-	-	0.5	-	
		3.0 to 3.6		0.5	-	-	0.5	-	
		4.5 to 5.5		0.5	-	-	0.5	-	
		3.0 to 3.6	C _L = 50 pF, R _L = 500 Ω, S ₁ = Open	0.5	-	-	0.5	-	
		4.5 to 5.5		0.5	-	-	0.5	-	
t _W	Pulse Width, CP, CLR, PR (Waveform 3)	1.65 to 1.95	C _L = 15 pF R _L = 1 MΩ S ₁ = Open	6.0	-	-	6.0	-	ns
		2.3 to 2.7		4.0	-	-	4.0	-	
		3.0 to 3.6		3.0	-	-	3.0	-	
		4.5 to 5.5		2.0	-	-	2.0	-	
		3.0 to 3.6	C _L = 50 pF, R _L = 500 Ω, S ₁ = Open	3.0	-	-	3.0	-	
		4.5 to 5.5		2.0	-	-	2.0	-	
t _{REC}	Recover Time PR; CLR to CP (Waveform 3)	1.65 to 1.95	C _L = 15 pF R _D = 1 MΩ S ₁ = Open	8.0	-	-	8.0	-	ns
		2.3 to 2.7		4.5	-	-	4.5	-	
		3.0 to 3.6		3.0	-	-	3.0	-	
		4.5 to 5.5		3.0	-	-	3.0	-	
		3.0 to 3.6	C _L = 50 pF, R _L = 500 Ω, S ₁ = Open	3.0	-	-	3.0	-	
		4.5 to 5.5		3.0	-	-	3.0	-	

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}/2 (per flip-flop). C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Units
C _{IN}	Input Capacitance	V _{CC} = 5.5 V, V _{IN} = 0 V or V _{CC}	2.5	pF
C _{OUT}	Output Capacitance	V _{CC} = 5.5 V, V _{IN} = 0 V or V _{CC}	2.5	pF
C _{PD}	Power Dissipation Capacitance (Note 6)	10 MHz, V _{CC} = 3.3 V, V _{IN} = 0 V or V _{CC} 10 MHz, V _{CC} = 5.5 V, V _{IN} = 0 V or V _{CC}	9 11	pF

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.



C_L includes probe and jig capacitance
R_T is Z_{OUT} of pulse generator (typically 50 Ω)
f = 1 MHz

Figure 3. Test Circuit

Test	Switch Position	C _L , pF	R _L , Ω	R ₁ , Ω
t _{PLH} / t _{PHL}	Open	See AC Characteristics Table		
t _{PZL} / t _{PZL}	2 x V _{CC}	50	500	500
t _{PHZ} / t _{PZH}	GND	50	500	500

X = Don't Care

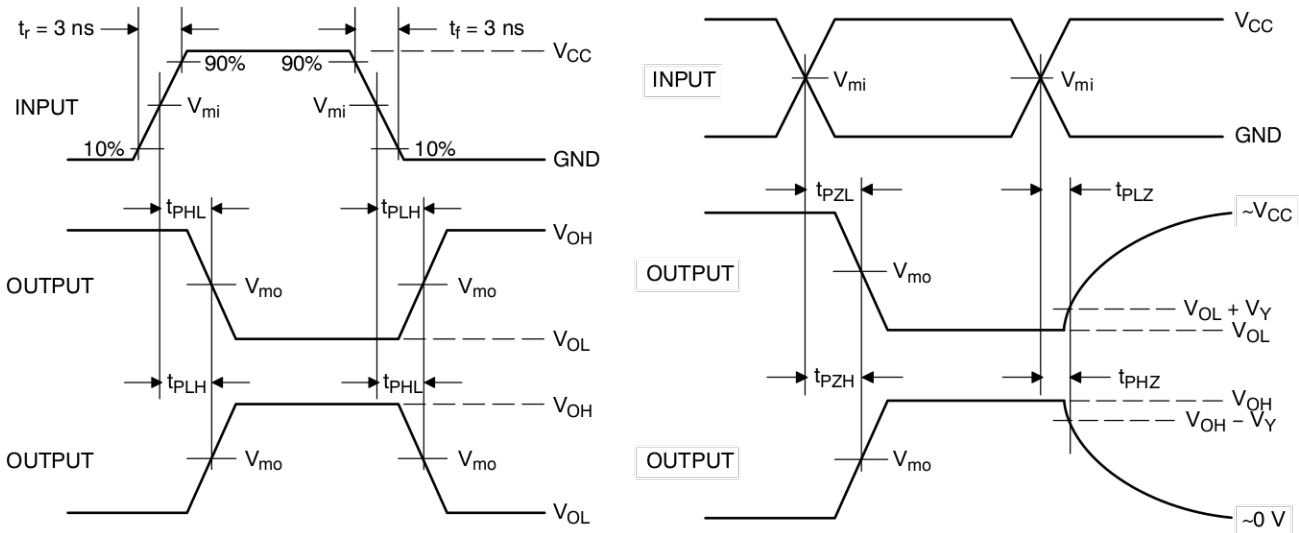


Figure 4. Switching Waveforms

NL17SZ74

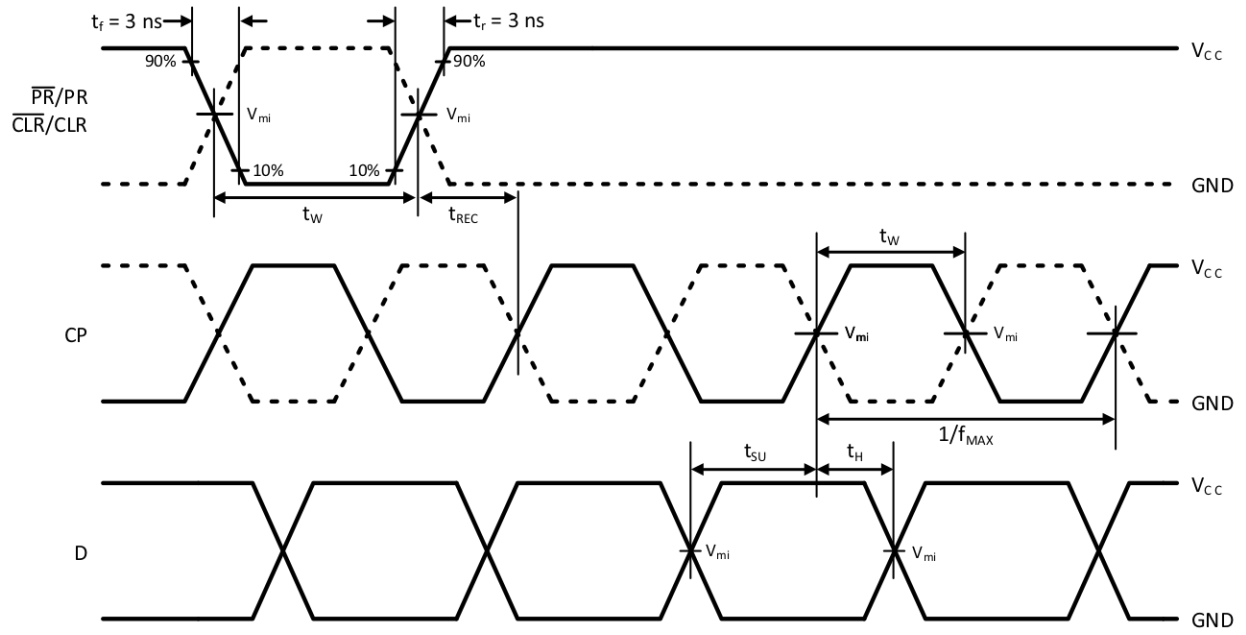


Figure 5. Setup, Hold and Recovery Time Waveforms

V_{CC}, V	V_{mi}, V	V_{mo}, V		V_Y, V
		t_{PLH}, t_{PHL}	$t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}$	
1.65 to 1.95	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	0.15
2.3 to 2.7	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	0.15
3.0 to 3.6	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	0.3
4.5 to 5.5	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	0.3

NL17SZ74

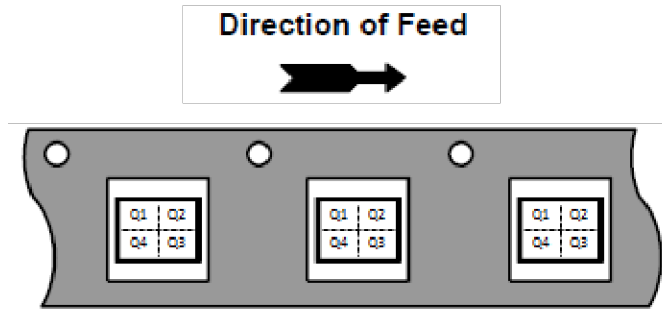
DEVICE ORDERING INFORMATION

Device	Packages	Marking	Pin 1 Orientation (See below)	Shipping [†]
NL17SZ74USG	US8	MH	Q4	3000 / Tape & Reel
NLV17SZ74USG*	US8	MH	Q4	3000 / Tape & Reel
NL17SZ74MQ1TCG	UQFN8, 1.6 x 1.6, 0.5P	AA	Q1	3000 / Tape & Reel
NLV17SZ74MQ1TCG* (In Development)	UQFN8, 1.6 x 1.6, 0.5P	AA	Q1	3000 / Tape & Reel
NL17SZ74MU1TCG (In Development)	UDFN8, 1.95 x 1.0, 0.5P	TBD	Q4	3000 / Tape & Reel
NL17SZ74MU3TCG (In Development)	UDFN8, 1.45 x 1.0, 0.35P	TBD	Q4	3000 / Tape & Reel
NL17SZ74MQ2TCG (In Development)	UQFN8, 1.4 x 1.2, 0.4P	TBD	TBD	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

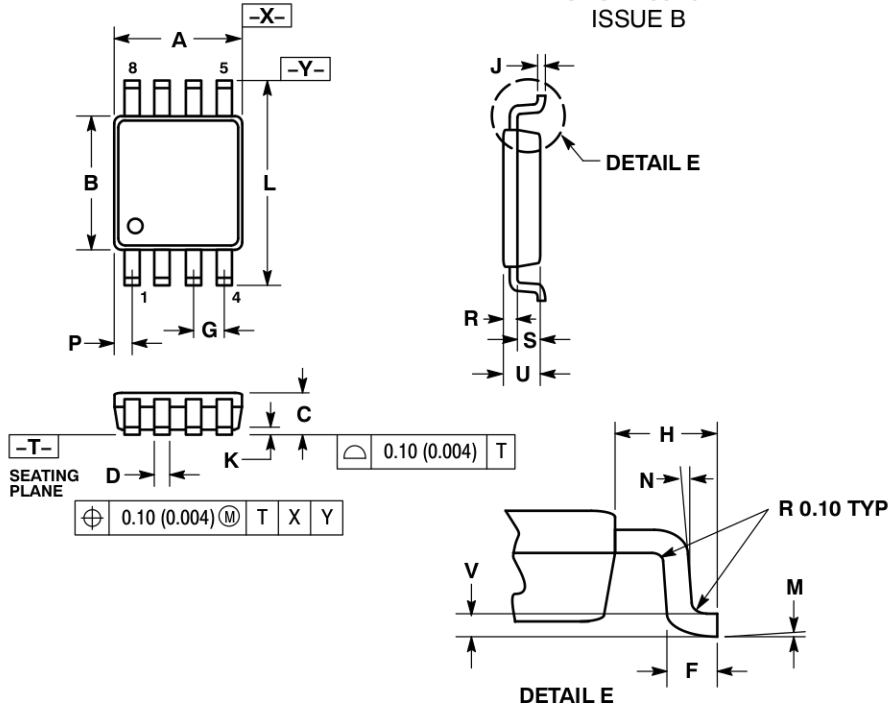
Pin 1 Orientation in Tape and Reel



NL17SZ74

PACKAGE DIMENSIONS

US8
US SUFFIX
CASE 493-02
ISSUE B

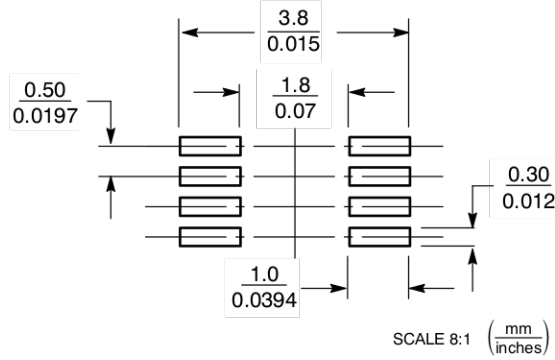


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION "A" DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR. MOLD FLASH, PROTRUSION AND GATE BURR SHALL NOT EXCEED 0.140 MM (0.0055") PER SIDE.
4. DIMENSION "B" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSION. INTER-LEAD FLASH AND PROTRUSION SHALL NOT EXCEED 0.140 (0.0055") PER SIDE.
5. LEAD FINISH IS SOLDER PLATING WITH THICKNESS OF 0.0076-0.0203 MM. (300-800 °).
6. ALL TOLERANCE UNLESS OTHERWISE SPECIFIED ±0.0508 (0.0002 °).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.90	2.10	0.075	0.083
B	2.20	2.40	0.087	0.094
C	0.60	0.90	0.024	0.035
D	0.17	0.25	0.007	0.010
F	0.20	0.35	0.008	0.014
G	0.50 BSC		0.020 BSC	
H	0.40 REF		0.016 REF	
J	0.10	0.18	0.004	0.007
K	0.00	0.10	0.000	0.004
L	3.00	3.20	0.118	0.126
M	0 °	6 °	0 °	6 °
N	5 °	10 °	5 °	10 °
P	0.23	0.34	0.010	0.013
R	0.23	0.33	0.009	0.013
S	0.37	0.47	0.015	0.019
U	0.60	0.80	0.024	0.031
V	0.12 BSC		0.005 BSC	

SOLDERING FOOTPRINT*

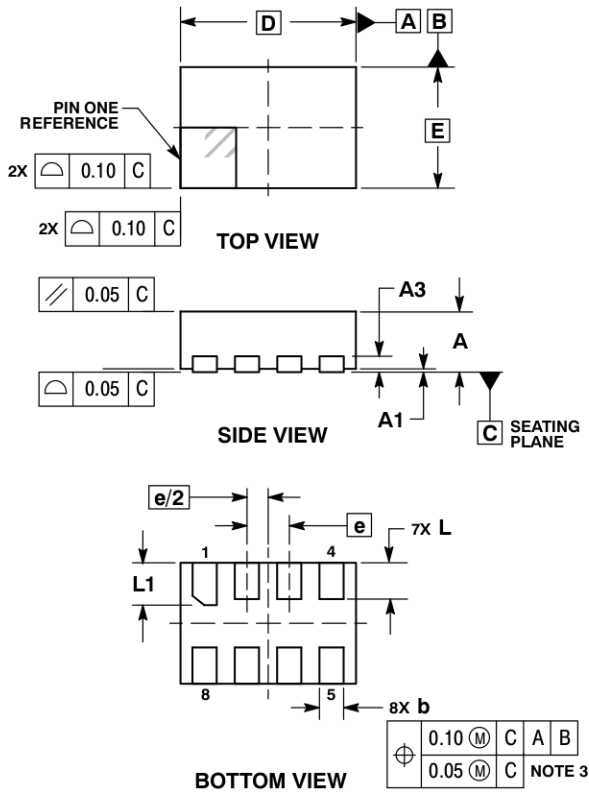


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NL17SZ74

PACKAGE DIMENSIONS

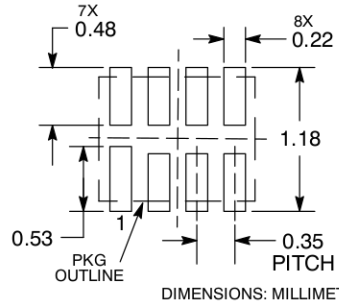
UDFN8, 1.45x1, 0.35P
CASE 517BZ
ISSUE O



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
 4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
D	1.45 BSC	
E	1.00 BSC	
e	0.35 BSC	
L	0.25	0.35
L1	0.30	0.40

RECOMMENDED SOLDERING FOOTPRINT*

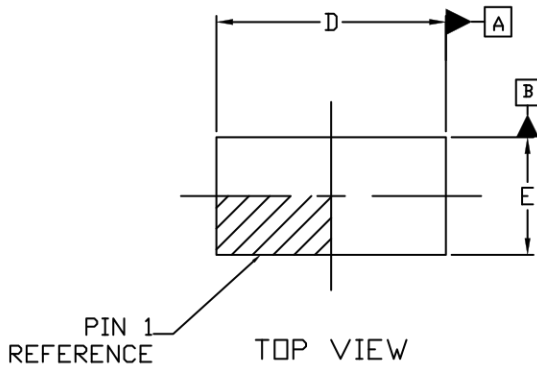


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NL17SZ74

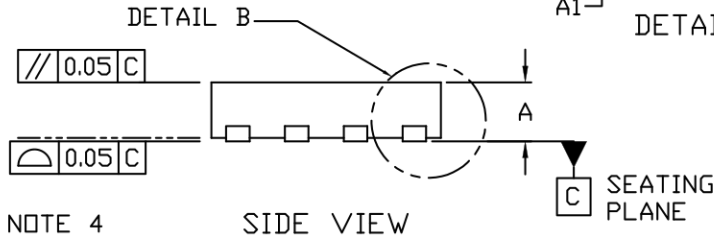
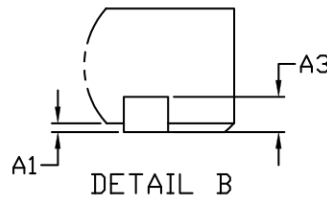
PACKAGE DIMENSIONS

UDFN8, 1.95x1.0, 0.5P
CASE 517CA
ISSUE A

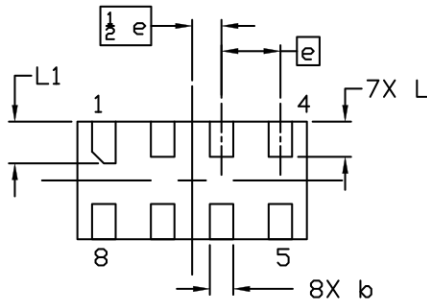


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO TO ALL THE TERMINALS.
5. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

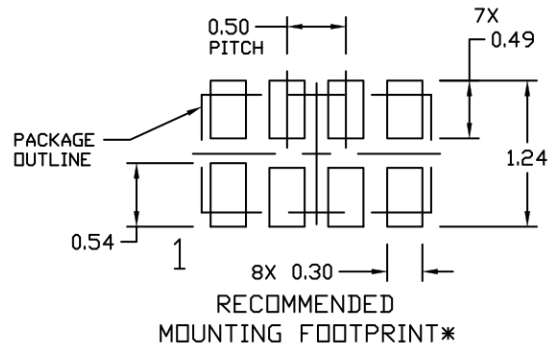


DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.45	0.50	0.55
A1	0.00	---	0.05
A3	0.13 REF		
b	0.15	0.20	0.25
D	1.85	1.95	2.05
E	0.90	1.00	1.10
e	0.50 BSC		
L	0.25	0.30	0.35
L1	0.30	0.35	0.40



⌀	0.10	C	A	B
	0.05	C		

NOTE 3

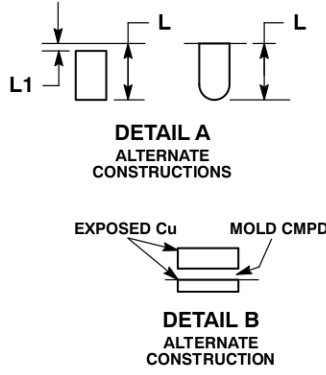
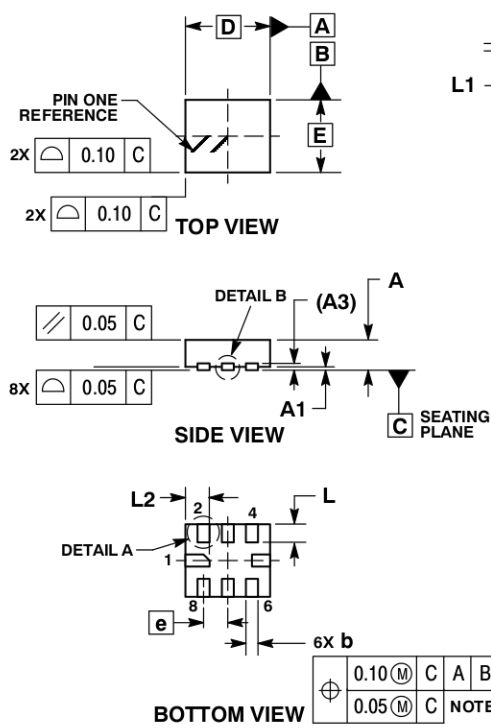


* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NL17SZ74

PACKAGE DIMENSIONS

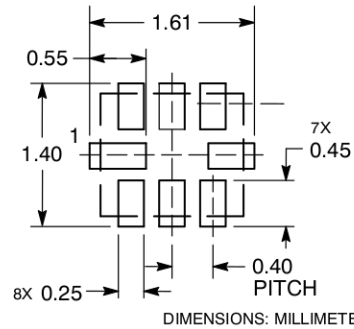
UQFN8, 1.4x1.2, 0.4P
CASE 523AS
ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 mm FROM THE TERMINAL TIP.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13	REF
b	0.15	0.25
D	1.40	BSC
E	1.20	BSC
e	0.40	BSC
L	0.20	0.40
L1	---	0.15
L2	0.30	0.50

SOLDERING FOOTPRINT*

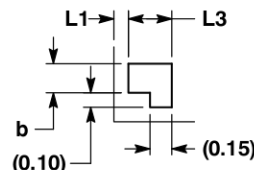
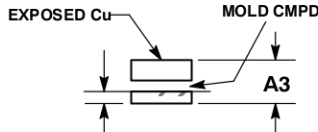
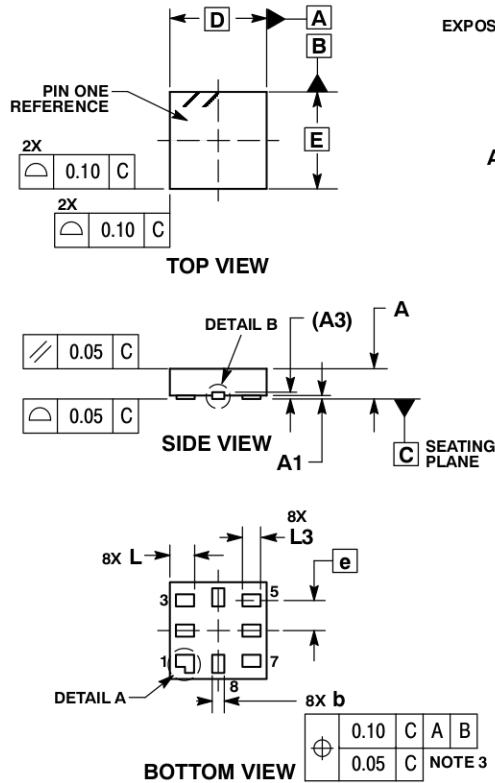


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NL17SZ74

PACKAGE DIMENSIONS

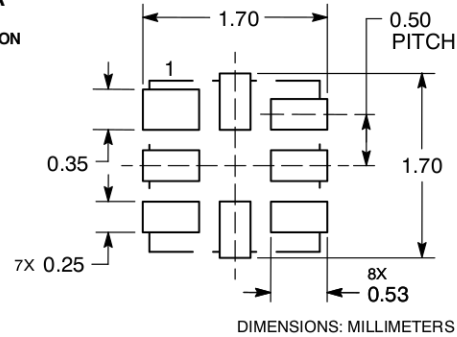
UQFN8, 1.6x1.6, 0.5P CASE 523AN ISSUE O



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.60
A1	0.00	0.05
A3	0.13	REF
b	0.15	0.25
D	1.60	BSC
E	1.60	BSC
e	0.50	BSC
L	0.35	0.45
L1	---	0.15
L3	0.25	0.35

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative