

MJE18004, MJF18004

Switch-mode NPN Bipolar Power Transistor For Switching Power Supply Applications

The MJE/MJF18004 have an applications specific state-of-the-art die designed for use in 220 V line-operated switch-mode Power supplies and electronic light ballasts.

Features

- Improved Efficiency Due to Low Base Drive Requirements:
 - ♦ High and Flat DC Current Gain h_{FE}
 - ♦ Fast Switching
 - ♦ No Coil Required in Base Circuit for Turn-Off (No Current Tail)
- Full Characterization at 125°C
- ON Semiconductor Six Sigma Philosophy Provides Tight and Reproducible Parametric Distributions
- Two Package Choices: Standard TO-220 or Isolated TO-220
- MJF18004, Case 221D, is UL Recognized at 3500 V_{RMS}: File #E69369
- These Devices are Pb-Free and are RoHS Compliant*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Sustaining Voltage	V_{CEO}	450	Vdc
Collector-Base Breakdown Voltage	V_{CES}	1000	Vdc
Emitter-Base Voltage	V_{EBO}	9.0	Vdc
Collector Current – Continuous	I_C	5.0	Adc
Collector Current – Peak (Note 1)	I_{CM}	10	Adc
Base Current – Continuous	I_B	2.0	Adc
Base Current – Peak (Note 1)	I_{BM}	4.0	Adc
RMS Isolation Voltage (Note 2) Test No. 1 Per Figure 22a Test No. 2 Per Figure 22b Test No. 3 Per Figure 22c (for 1 sec, R.H. < 30%, $T_A = 25^\circ\text{C}$)	V_{ISOL}	MJF18004 4500 3500 1500	V
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ MJE18004 MJF18004 Derate above 25°C MJE18004 MJF18004	P_D	75 35 0.6 0.28	W W/°C
Operating and Storage Temperature	T_J, T_{stg}	-65 to 150	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case MJE18004 MJF18004	$R_{\theta JC}$	1.65 3.55	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8" from Case for 5 Seconds	T_L	260	°C

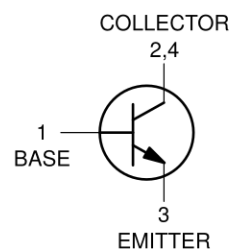
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Pulse Test: Pulse Width = 5 ms, Duty Cycle $\leq 10\%$.
2. Proper strike and creepage distance must be provided.

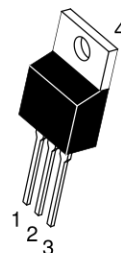


www.onsemi.com

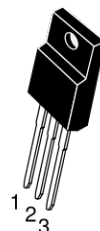
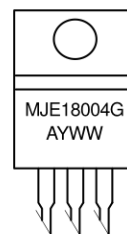
POWER TRANSISTOR 5.0 AMPERES 1000 VOLTS 35 and 75 WATTS



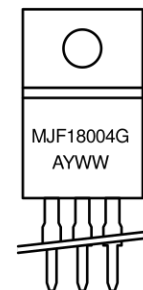
MARKING DIAGRAMS



TO-220AB
CASE 221A-09
STYLE 1



TO-220 FULLPACK
CASE 221D
STYLE 2
UL RECOGNIZED



G = Pb-Free Package
A = Assembly Location
Y = Year
WW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

MJE18004, MJF18004

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (I _C = 100 mA, L = 25 mH)	V _{CEO(sus)}	450	–	–	Vdc
Collector Cutoff Current (V _{CE} = Rated V _{CEO} , I _B = 0)	I _{CEO}	–	–	100	μAdc
Collector Cutoff Current (V _{CE} = Rated V _{CES} , V _{EB} = 0)	I _{CES}	–	–	100	μAdc
(T _C = 25°C)		–	–	500	
(T _C = 125°C)		–	–	100	
Collector Cutoff Current (V _{CE} = 800 V, V _{EB} = 0)		–	–	100	
Emitter Cutoff Current (V _{EB} = 9.0 Vdc, I _C = 0)	I _{EBO}	–	–	100	μAdc

ON CHARACTERISTICS

Base-Emitter Saturation Voltage (I _C = 1.0 Adc, I _B = 0.1 Adc) (I _C = 2.0 Adc, I _B = 0.4 Adc)	V _{BE(sat)}	– –	0.82 0.92	1.1 1.25	Vdc
Collector-Emitter Saturation Voltage (I _C = 1.0 Adc, I _B = 0.1 Adc)	V _{CE(sat)}	–	0.25	0.5	Vdc
(T _C = 125°C)		–	0.29	0.6	
(I _C = 2.0 Adc, I _B = 0.4 Adc)		–	0.3	0.45	
(T _C = 125°C)		–	0.36	0.8	
(I _C = 2.5 Adc, I _B = 0.5 Adc)		–	0.5	0.75	
DC Current Gain (I _C = 1.0 Adc, V _{CE} = 2.5 Vdc)	h _{FE}	12	21	–	–
(T _C = 125°C)		–	20	–	
(I _C = 0.3 Adc, V _{CE} = 5.0 Vdc)		14	–	34	
(T _C = 125°C)		–	32	–	
(I _C = 2.0 Adc, V _{CE} = 1.0 Vdc)		6.0	11	–	
(T _C = 125°C)		–	7.5	–	
(I _C = 10 mAdc, V _{CE} = 5.0 Vdc)		10	22	–	

DYNAMIC CHARACTERISTICS

Current Gain Bandwidth ($I_C = 0.5 \text{ Adc}$, $V_{CE} = 10 \text{ Vdc}$, $f = 1.0 \text{ MHz}$)				f_T	–	13	–	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 1.0 \text{ MHz}$)				C_{ob}	–	50	65	pF
Input Capacitance ($V_{EB} = 8.0 \text{ V}$)				C_{ib}	–	800	1000	pF
Dynamic Saturation Voltage: Determined 1.0 μs and 3.0 μs respectively after rising I_{B1} reaches 90% of final I_{B1} (see Figure 18)	$(I_C = 1.0 \text{ Adc}$ $I_{B1} = 100 \text{ mAdc}$ $V_{CC} = 300 \text{ V})$	1.0 μs	$(T_C = 125^\circ\text{C})$	$V_{CE(dsat)}$	–	6.8	–	Vdc
					–	14	–	
	$(I_C = 2.0 \text{ Adc}$ $I_{B1} = 400 \text{ mAdc}$ $V_{CC} = 300 \text{ V})$	3.0 μs	$(T_C = 125^\circ\text{C})$		–	2.4	–	
					–	5.6	–	
		1.0 μs	$(T_C = 125^\circ\text{C})$		–	11.3	–	
					–	15.5	–	
$(I_C = 2.0 \text{ Adc}$ $I_{B1} = 400 \text{ mAdc}$ $V_{CC} = 300 \text{ V})$	3.0 μs	$(T_C = 125^\circ\text{C})$	–	1.3	–			
			–	6.1	–			

MJE18004, MJF18004

ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Characteristic			Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 μs)							
Turn-On Time	(I _C = 1.0 Adc, I _{B1} = 0.1 Adc, I _{B2} = 0.5 Adc, V _{CC} = 300 V)	(T _C = 125°C)	t _{on}	– –	210 180	300 –	ns
Turn-Off Time		(T _C = 125°C)	t _{off}	– –	1.0 1.3	1.7 –	μs
Turn-On Time	(I _C = 2.0 Adc, I _{B1} = 0.4 Adc, I _{B1} = 1.0 Adc, V _{CC} = 300 V)	(T _C = 125°C)	t _{on}	– –	75 90	110 –	ns
Turn-Off Time		(T _C = 125°C)	t _{off}	– –	1.5 1.8	2.5 –	μs
Turn-On Time	(I _C = 2.5 Adc, I _{B1} = 0.5 Adc, I _{B2} = 0.5 Adc, V _{CC} = 250 V)	(T _C = 125°C)	t _{on}	– –	450 900	800 1400	ns
Storage Time		(T _C = 125°C)	t _s	– –	2.0 2.2	3.0 3.5	μs
Fall Time		(T _C = 125°C)	t _f	– –	275 500	400 800	ns
SWITCHING CHARACTERISTICS: Inductive Load (V _{clamp} = 300 V, V _{CC} = 15 V, L = 200 μH)							
Fall Time	(I _C = 1.0 Adc, I _{B1} = 0.1 Adc, I _{B2} = 0.5 Adc)	(T _C = 125°C)	t _{fi}	– –	100 100	150 –	ns
Storage Time		(T _C = 125°C)	t _{si}	– –	1.1 1.4	1.7 –	μs
Crossover Time		(T _C = 125°C)	t _c	– –	180 160	250 –	ns
Fall Time	(I _C = 2.0 Adc, I _{B1} = 0.4 Adc, I _{B2} = 1.0 Adc)	(T _C = 125°C)	t _{fi}	– –	90 150	175 –	ns
Storage Time		(T _C = 125°C)	t _{si}	– –	1.7 2.2	2.5 –	μs
Crossover Time		(T _C = 125°C)	t _c	– –	180 250	300 –	ns
Fall Time	(I _C = 2.5 Adc, I _{B1} = 0.5 Adc, I _{B2} = 0.5 Adc, V _{BE(off)} = –5.0 Vdc)	(T _C = 125°C)	t _{fi}	– –	70 100	130 175	ns
Storage Time		(T _C = 125°C)	t _{si}	– –	0.75 1.0	1.0 1.3	μs
Crossover Time		(T _C = 125°C)	t _c	– –	250 250	350 500	ns

TYPICAL STATIC CHARACTERISTICS

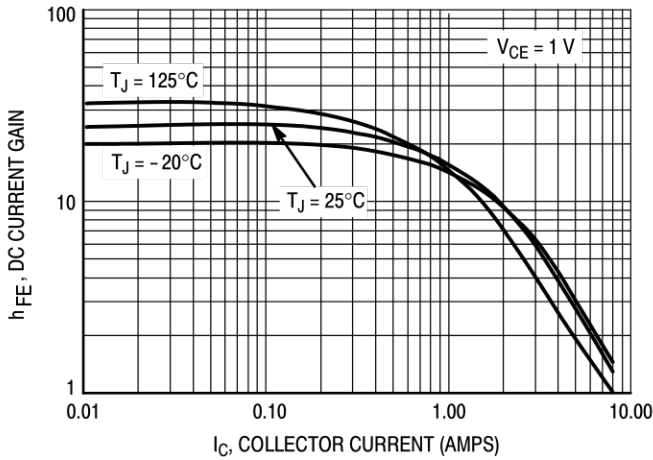


Figure 1. DC Current Gain @ 1 Volt

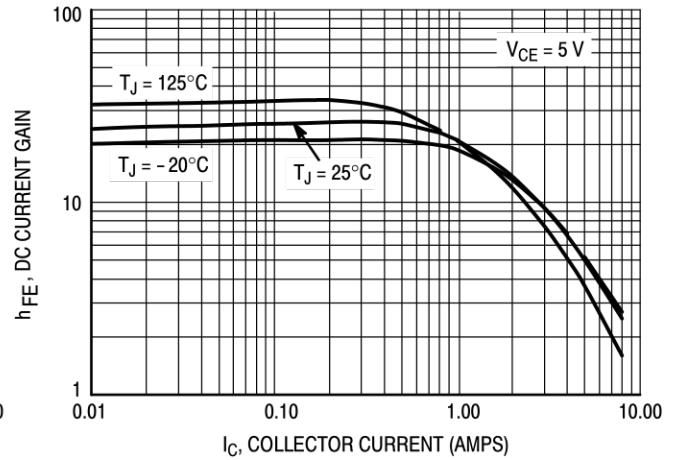


Figure 2. DC Current Gain @ 5 Volts

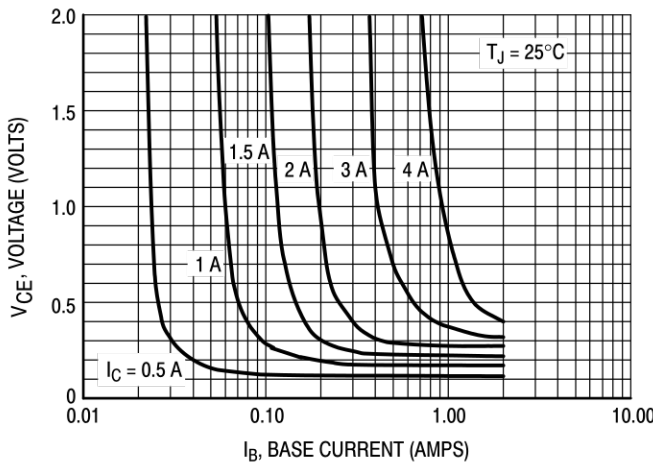


Figure 3. Collector Saturation Region

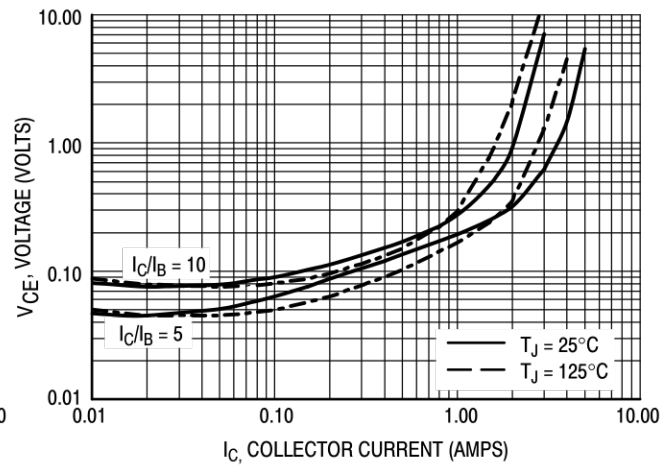


Figure 4. Collector-Emitter Saturation Voltage

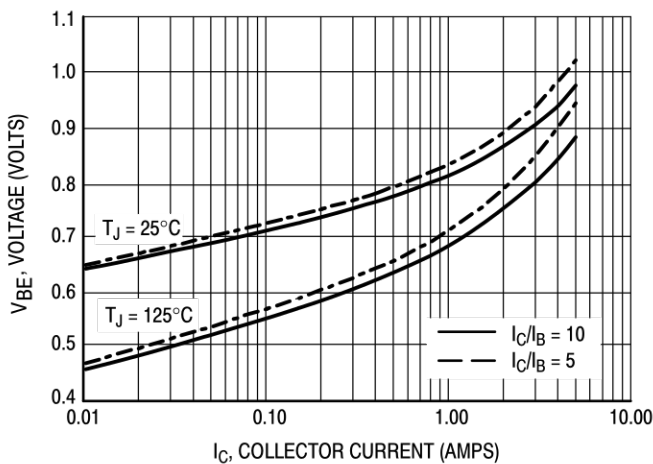


Figure 5. Base-Emitter Saturation Region

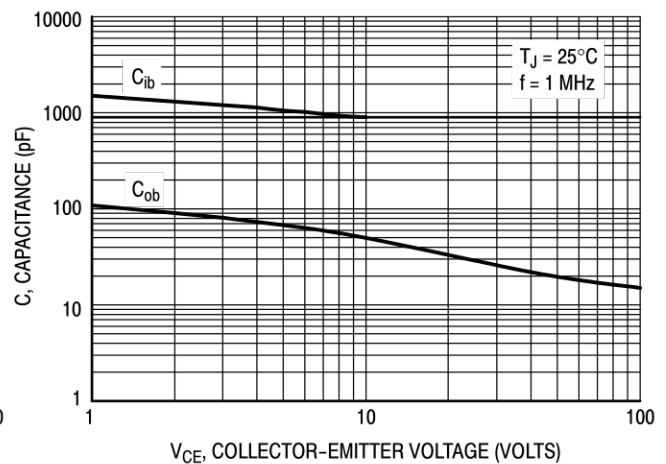


Figure 6. Capacitance

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

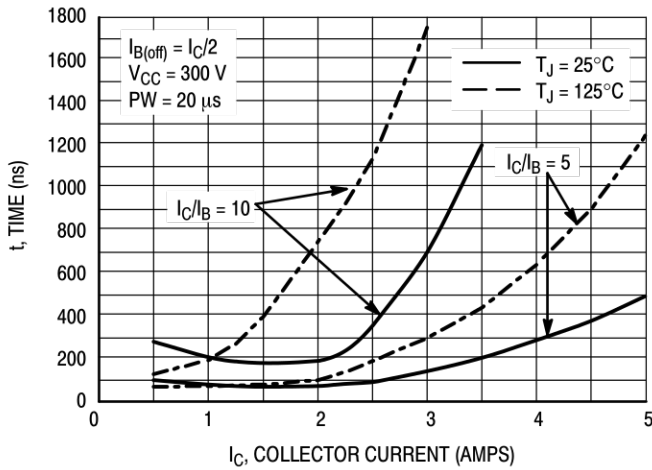


Figure 7. Resistive Switching, t_{on}

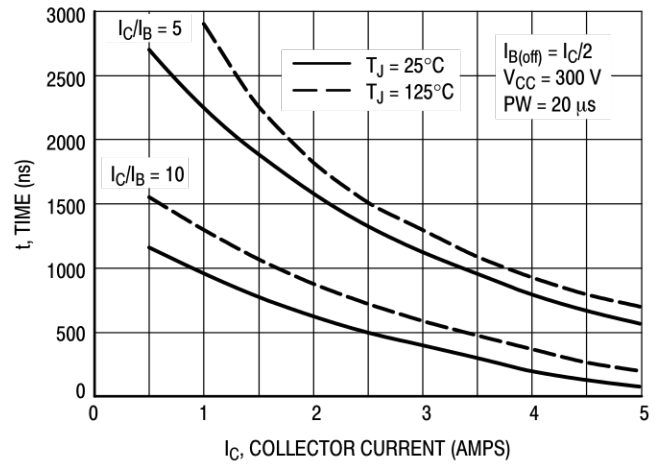


Figure 8. Resistive Switching, t_{off}

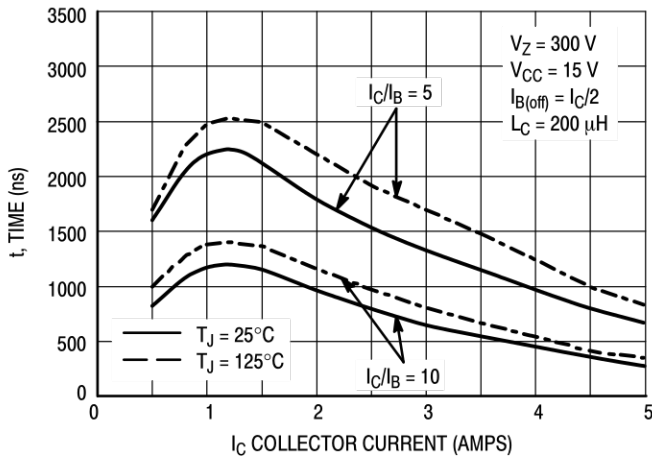


Figure 9. Inductive Storage Time, t_{si}

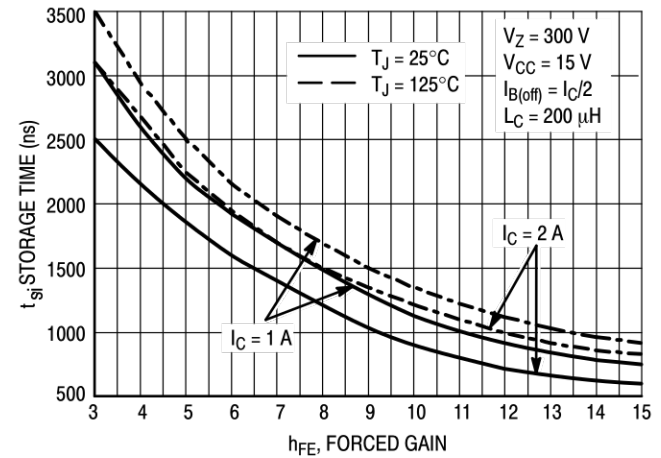


Figure 10. Inductive Storage Time, $t_{si}(h_{FE})$

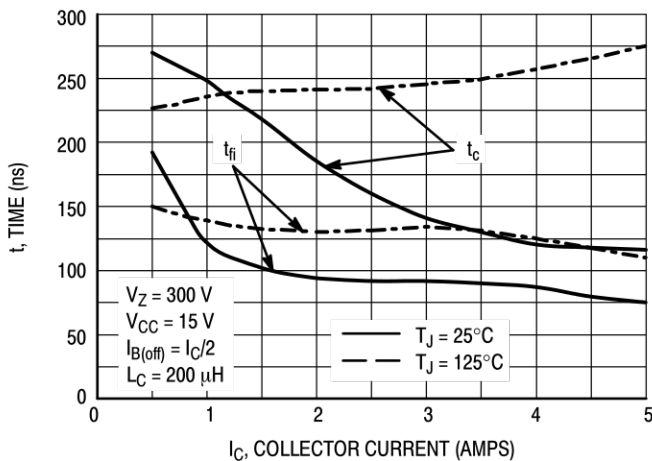


Figure 11. Inductive Switching, t_c and t_{fi} , $I_C/I_B = 5$

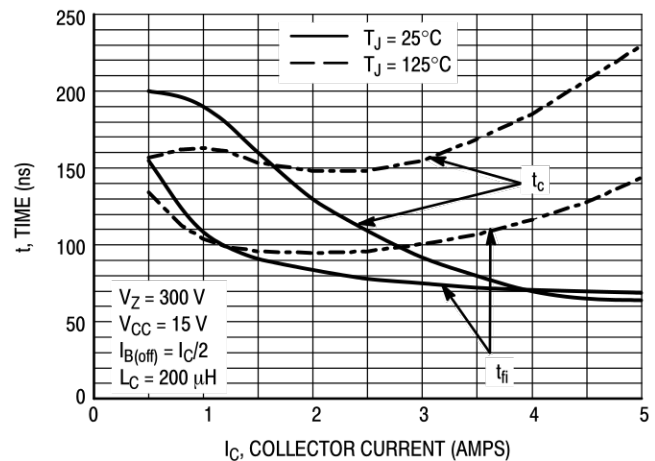


Figure 12. Inductive Switching, t_c and t_{fi} , $I_C/I_B = 10$

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

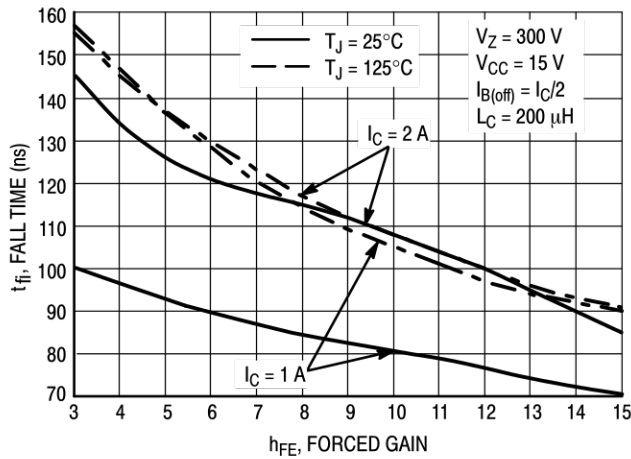


Figure 13. Inductive Fall Time

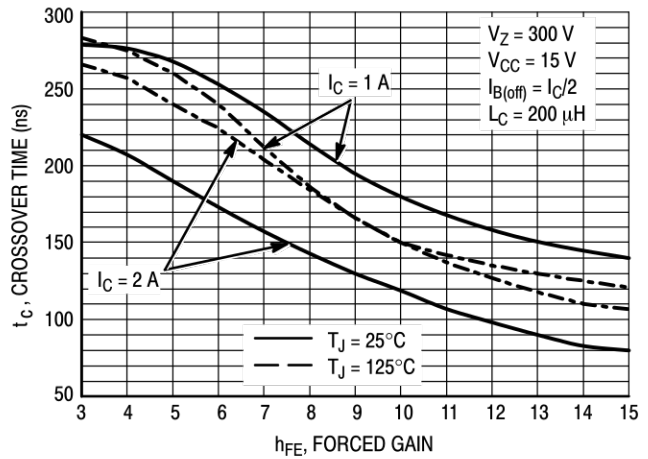


Figure 14. Inductive Crossover Time

GUARANTEED SAFE OPERATING AREA INFORMATION

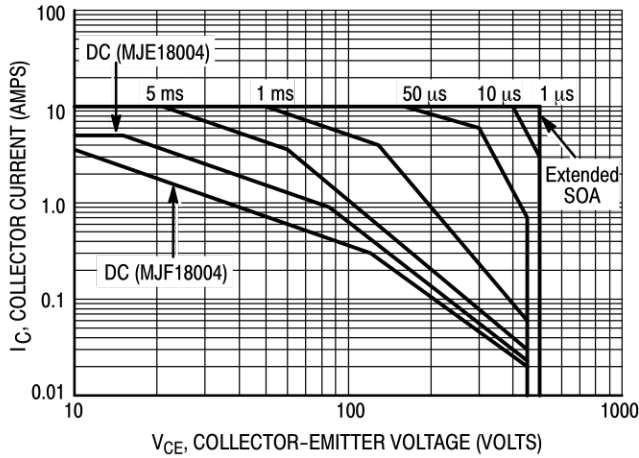


Figure 15. Forward Bias Safe Operating Area

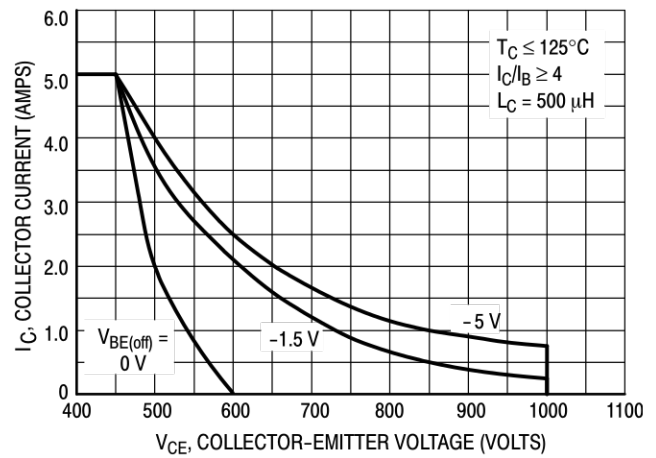


Figure 16. Reverse Bias Safe Operating Area

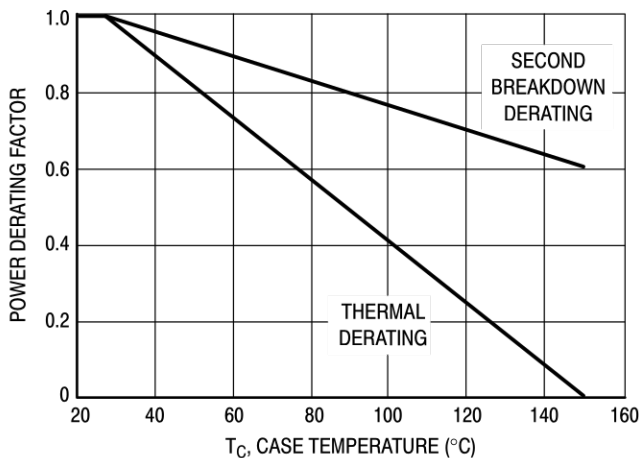


Figure 17. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 15 is based on $T_C = 25^\circ\text{C}$; $T_J(\text{pk})$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 may be found at any case temperature by using the appropriate curve on Figure 17. $T_J(\text{pk})$ may be calculated from the data in Figures 20 and 21. At any case temperatures, thermal limitations will reduce the power that can be handled to values less the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn-off with the base-to-emitter junction reverse biased. The safe level is specified as a reverse-biased safe operating area (Figure 16). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

MJE18004, MJF18004

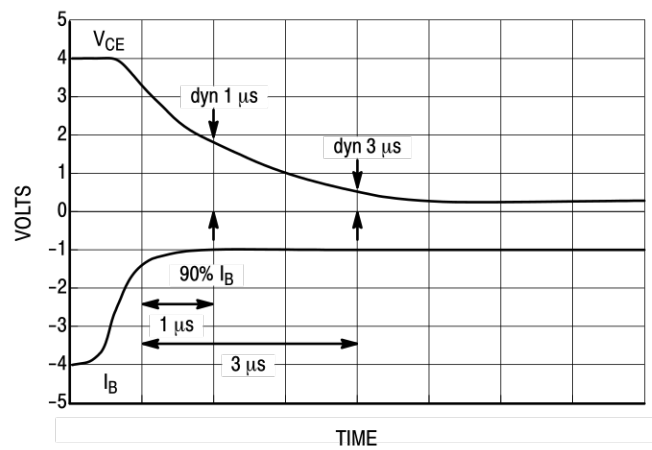


Figure 18. Dynamic Saturation Voltage Measurements

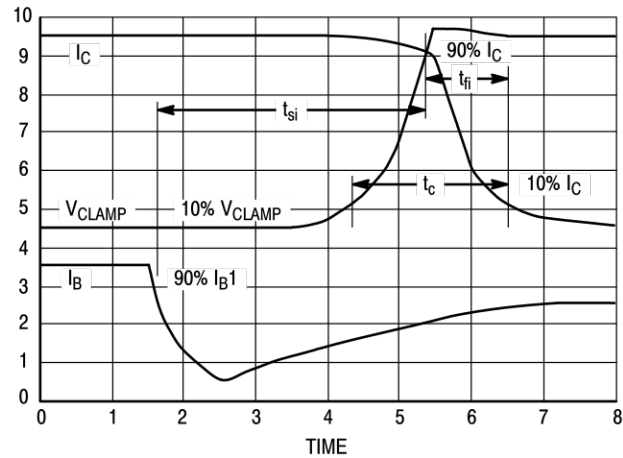


Figure 19. Inductive Switching Measurements

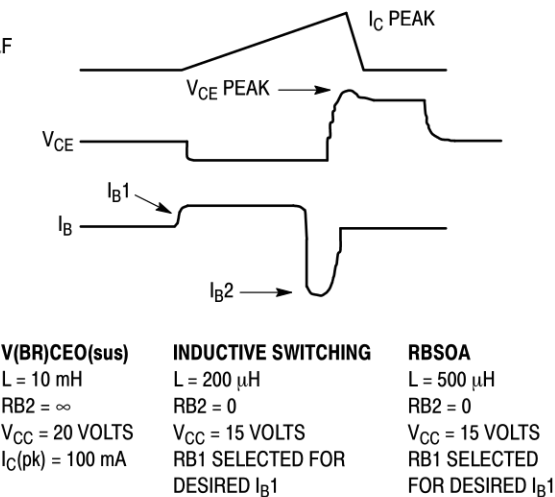
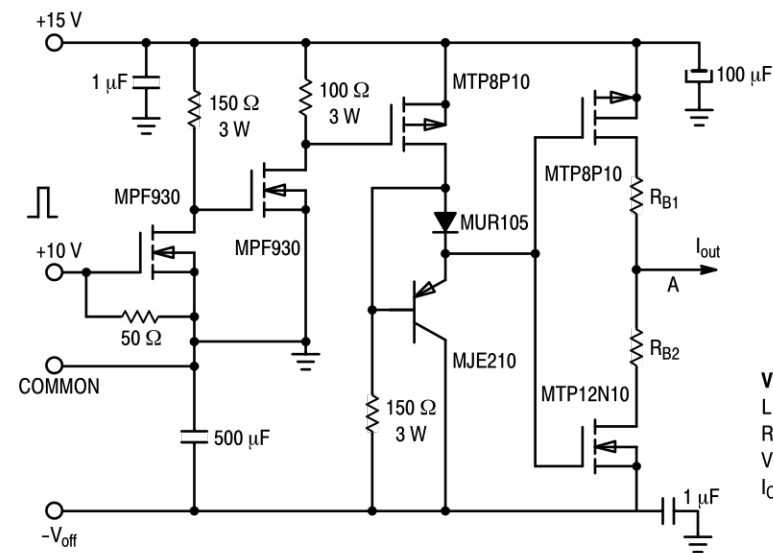


Table 1. Inductive Load Switching Drive Circuit

MJE18004, MJF18004

TYPICAL THERMAL RESPONSE

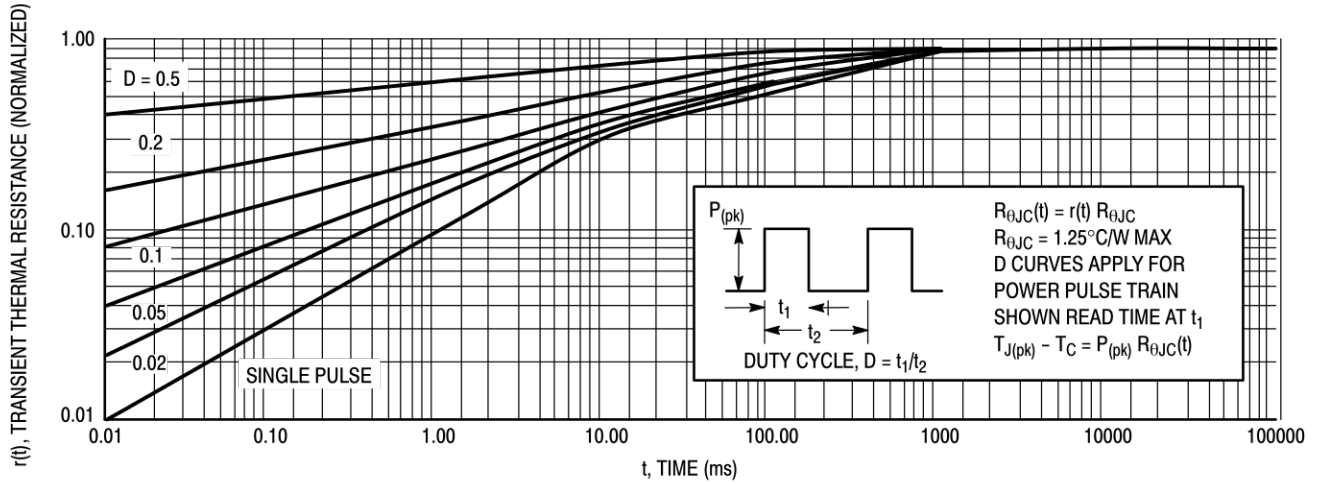


Figure 20. Typical Thermal Response ($Z_{\theta JC}(t)$) for MJE18004

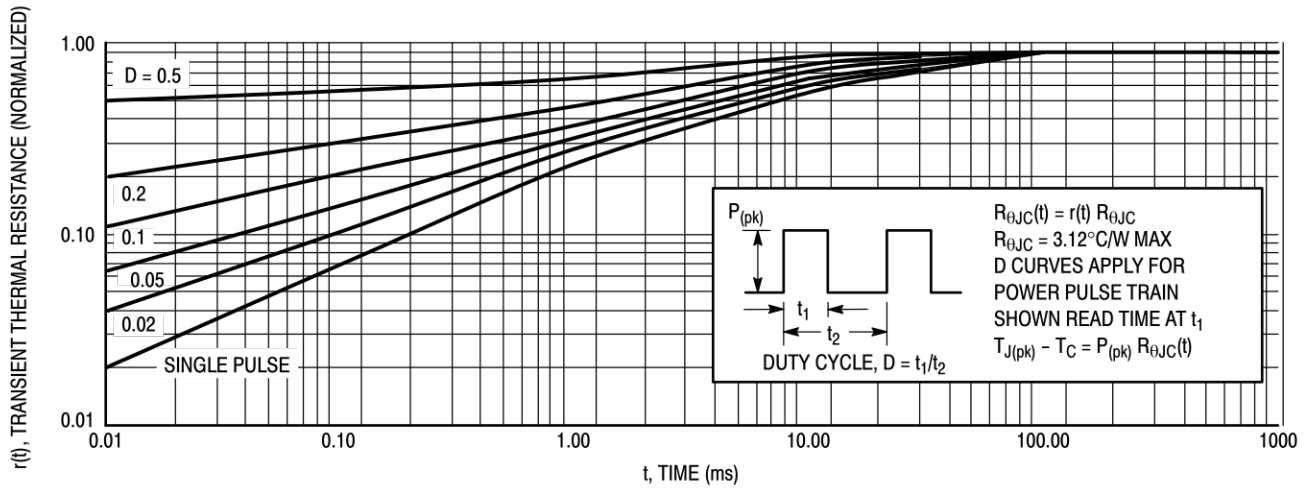


Figure 21. Typical Thermal Response for MJF18004

ORDERING INFORMATION

Device	Package	Shipping
MJE18004G	TO-220AB (Pb-Free)	50 Units / Rail
MJF18004G	TO-220 (Fullpack) (Pb-Free)	50 Units / Rail

TEST CONDITIONS FOR ISOLATION TESTS*

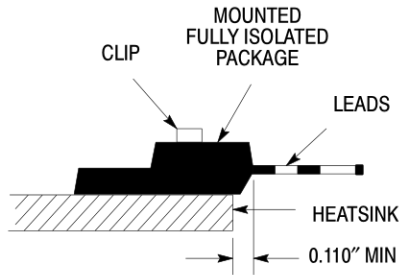


Figure 22a. Screw or Clip Mounting Position for Isolation Test Number 1

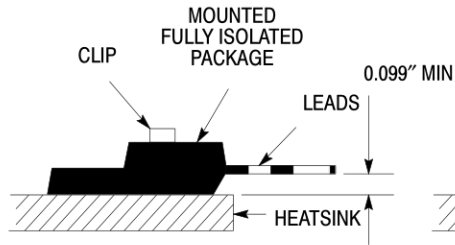


Figure 22b. Clip Mounting Position for Isolation Test Number 2

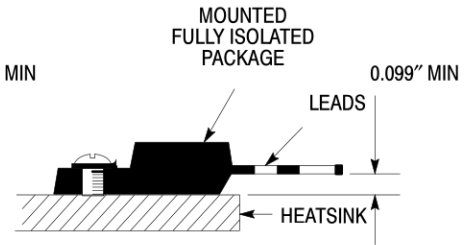


Figure 22c. Screw Mounting Position for Isolation Test Number 3

*Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION**

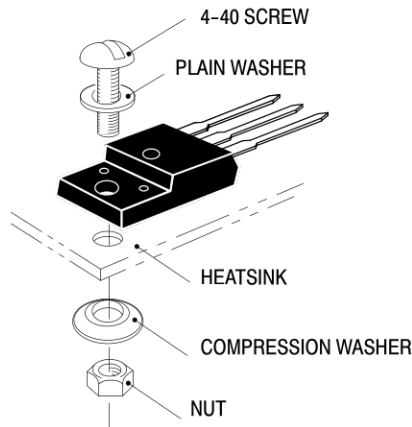


Figure 23a. Screw-Mounted

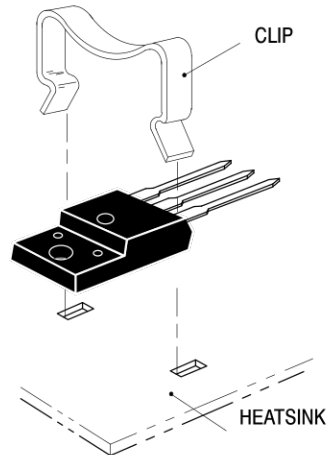


Figure 23b. Clip-Mounted

Figure 23. Typical Mounting Techniques for Isolated Package

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

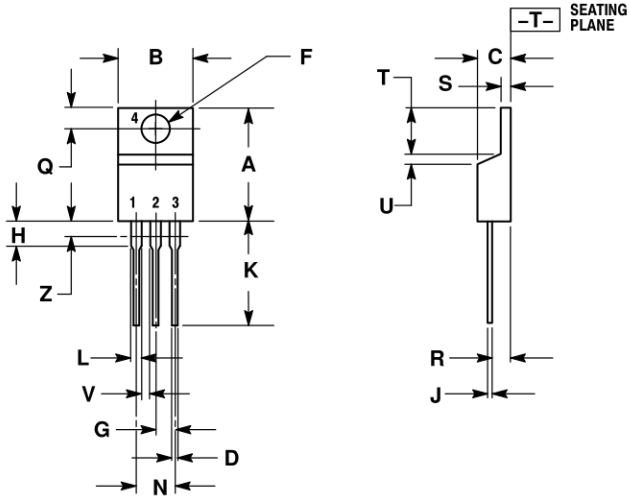
Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, ON Semiconductor does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

MJE18004, MJF18004

PACKAGE DIMENSIONS

TO-220
CASE 221A-09
ISSUE AH



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

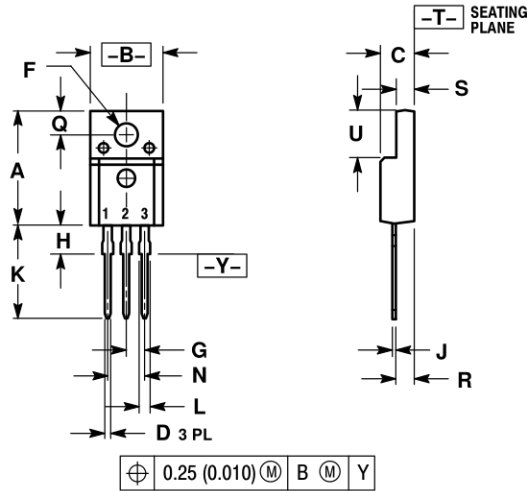
STYLE 1:

- PIN 1: BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

MJE18004, MJF18004

PACKAGE DIMENSIONS

TO-220 FULLPAK CASE 221D-03 ISSUE K



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 221D-01 THRU 221D-02 OBSOLETE, NEW STANDARD 221D-03.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.617	0.635	15.67	16.12
B	0.392	0.419	9.96	10.63
C	0.177	0.193	4.50	4.90
D	0.024	0.039	0.60	1.00
F	0.116	0.129	2.95	3.28
G	0.100 BSC		2.54 BSC	
H	0.118	0.135	3.00	3.43
J	0.018	0.025	0.45	0.63
K	0.503	0.541	12.78	13.73
L	0.048	0.058	1.23	1.47
N	0.200 BSC		5.08 BSC	
Q	0.122	0.138	3.10	3.50
R	0.099	0.117	2.51	2.96
S	0.092	0.113	2.34	2.87
U	0.239	0.271	6.06	6.88

STYLE 2:

- PIN 1. BASE
- COLLECTOR
- EMITTER

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative

MJE18004/D