

NDS352AP

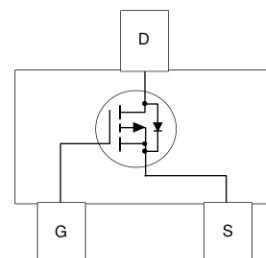
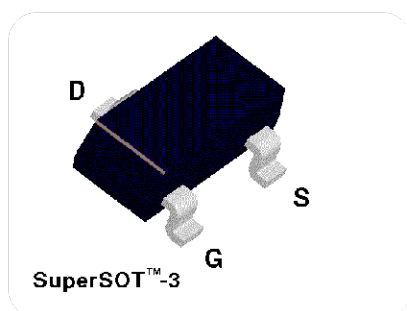
P-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

These P -Channel logic level enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications such as notebook computer power management, portable electronics, and other battery powered circuits where fast high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

Features

- -0.9 A, -30 V. $R_{DS(ON)} = 0.5 \Omega @ V_{GS} = -4.5 \text{ V}$
 $R_{DS(ON)} = 0.3 \Omega @ V_{GS} = -10 \text{ V}.$
- Industry standard outline SOT-23 surface mount package using proprietary SuperSOT™-3 design for superior thermal and electrical capabilities.
- High density cell design for extremely low $R_{DS(ON)}$.
- Exceptional on-resistance and maximum DC current capability.



Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	NDS352AP	Units
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage - Continuous	± 20	V
I_D	Maximum Drain Current - Continuous (Note 1a) - Pulsed	± 0.9	A
		± 10	
P_D	Maximum Power Dissipation (Note 1a) (Note 1b)	0.5	W
		0.46	
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
THERMAL CHARACTERISTICS			
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	250	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	75	$^\circ\text{C/W}$

Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
V_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -24\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
		$T_J = 125^{\circ}\text{C}$			-10	μA
I_{GSSF}	Gate - Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-0.8	-1.7	-2.5	V
		$T_J = 125^{\circ}\text{C}$	-0.5	-1.4	-2.2	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = -4.5\text{ V}, I_D = -0.9\text{ A}$		0.45	0.5	Ω
		$T_J = 125^{\circ}\text{C}$		0.65	0.7	
		$V_{GS} = -10\text{ V}, I_D = -1\text{ A}$		0.25	0.3	
$I_{D(ON)}$	On-State Drain Current	$V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$	-2			A
g_{FS}	Forward Transconductance	$V_{DS} = -5\text{ V}, I_D = -0.9\text{ A}$		1.9		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	$V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		135		pF
C_{oss}	Output Capacitance			88		pF
C_{rss}	Reverse Transfer Capacitance			40		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{d(on)}$	Turn - On Delay Time	$V_{DD} = -6\text{ V}, I_D = -1\text{ A},$ $V_{GS} = -4.5\text{ V}, R_{GEN} = 6\text{ }\Omega$		5	10	ns
t_r	Turn - On Rise Time			17	30	ns
$t_{d(off)}$	Turn - Off Delay Time			35	70	ns
t_f	Turn - Off Fall Time			30	60	ns
$t_{d(on)}$	Turn - On Delay Time	$V_{DD} = -10\text{ V}, I_D = -1\text{ A},$ $V_{GS} = -10\text{ V}, R_{GEN} = 50\text{ }\Omega$		8	15	ns
t_r	Turn - On Rise Time			16	30	ns
$t_{d(off)}$	Turn - Off Delay Time			35	90	ns
t_f	Turn - Off Fall Time			30	90	ns
Q_g	Total Gate Charge	$V_{DS} = -10\text{ V}, I_D = -0.9\text{ A},$ $V_{GS} = -4.5\text{ V}$		2	3	nC
Q_{gs}	Gate-Source Charge			0.5		nC
Q_{gd}	Gate-Drain Charge			1		nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

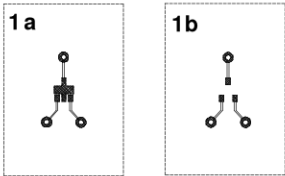
Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I _S	Maximum Continuous Source Current				-0.42	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current				-10	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = -0.42 (Note 2)		-0.8	-1.2	V

Notes:
1. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical R_{θJA} using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

- a. 250°C/W when mounted on a 0.02 in² pad of 2oz copper.
- b. 270°C/W when mounted on a 0.001 in² pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

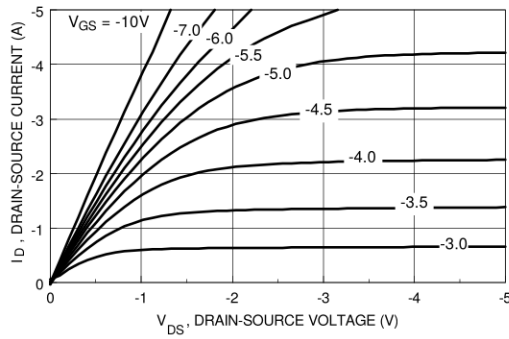


Figure 1. On-Region Characteristics.

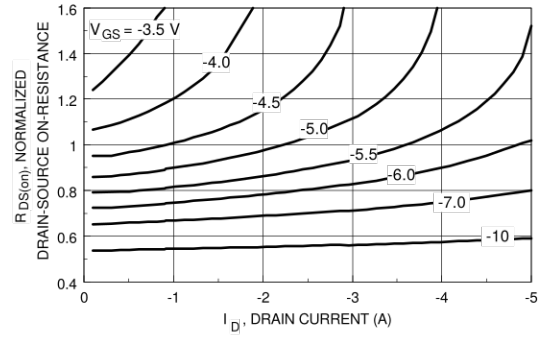


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

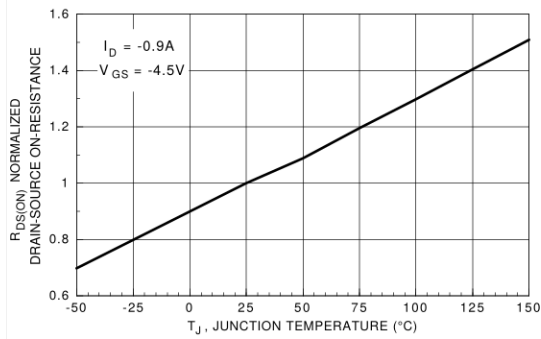


Figure 3. On-Resistance Variation with Temperature.

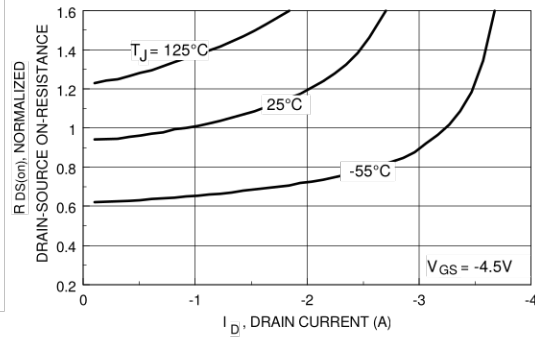


Figure 4. On-Resistance Variation with Drain Current and Temperature.

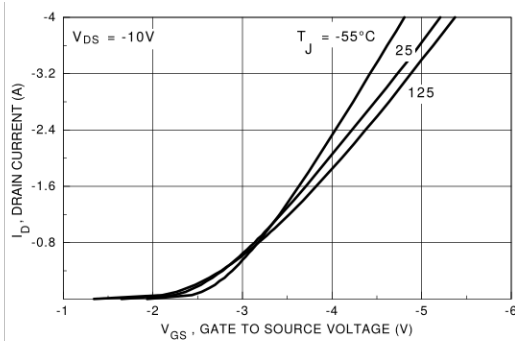


Figure 5. Transfer Characteristics.

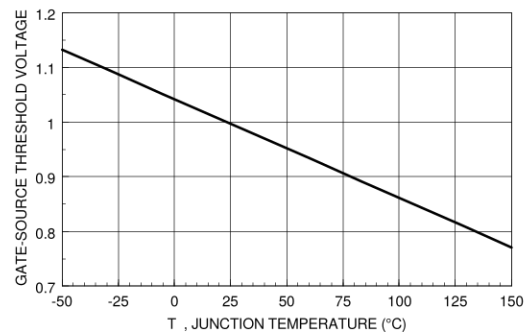


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

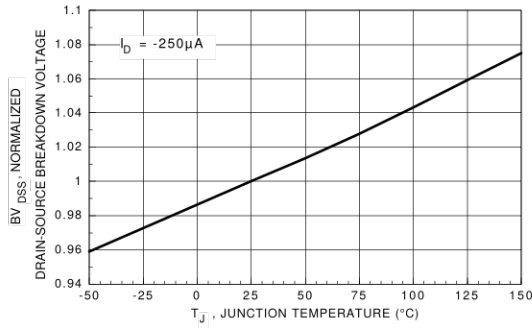


Figure 7. Breakdown Voltage Variation with Temperature.

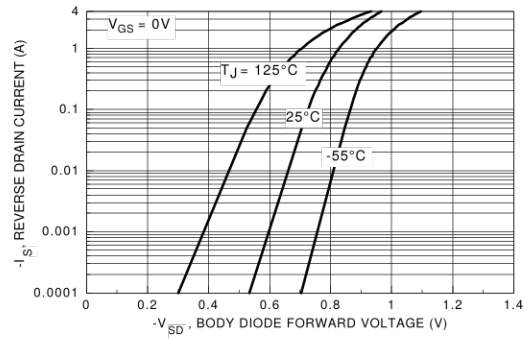


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature.

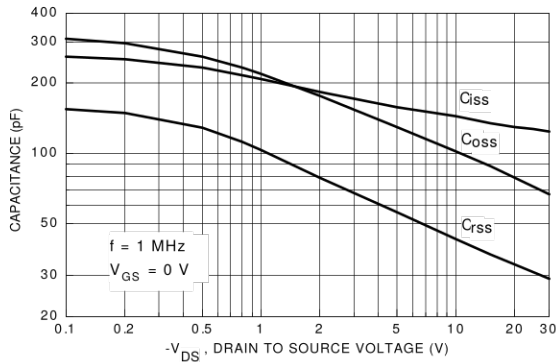


Figure 9. Capacitance Characteristics.

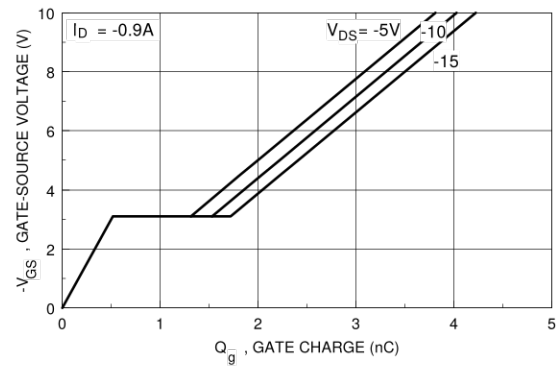


Figure 10. Gate Charge Characteristics.

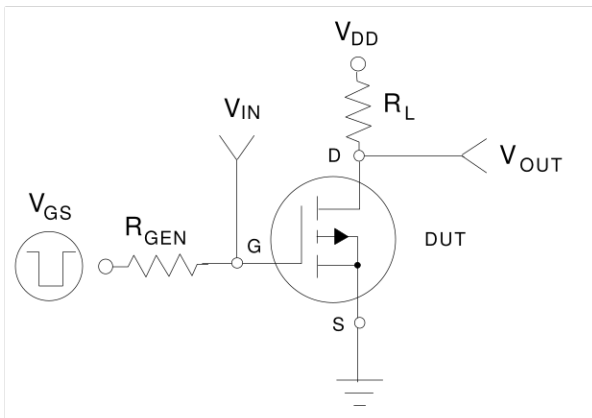


Figure 11. Switching Test Circuit.

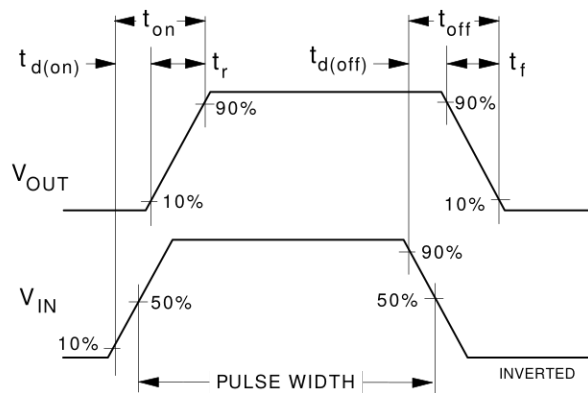
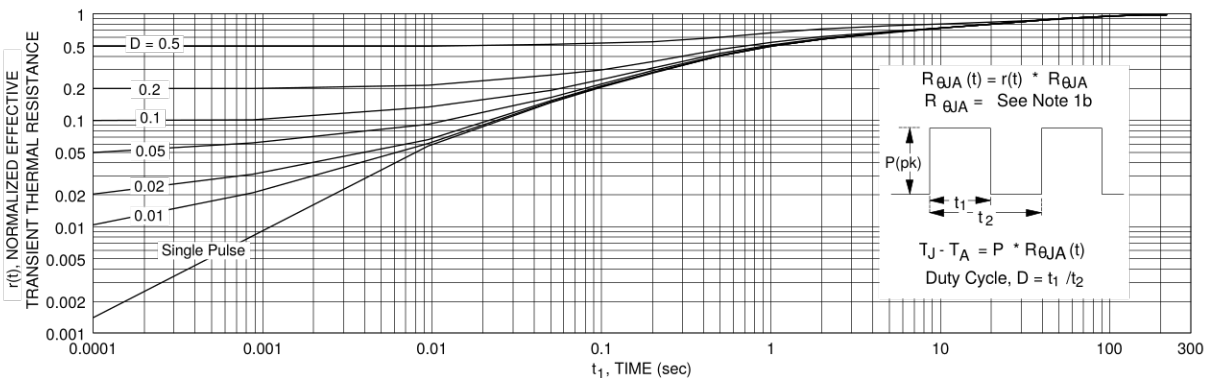
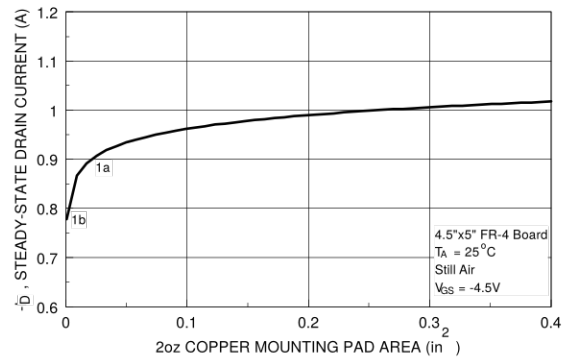
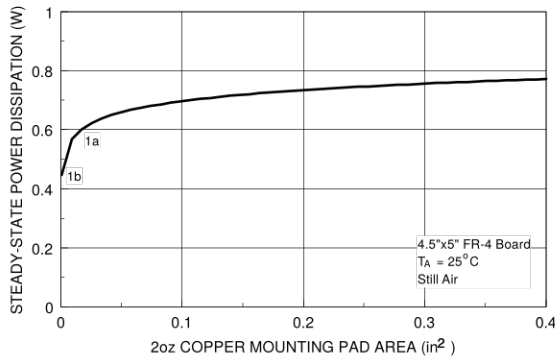
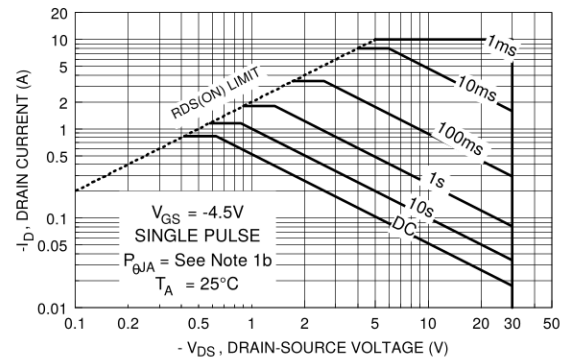
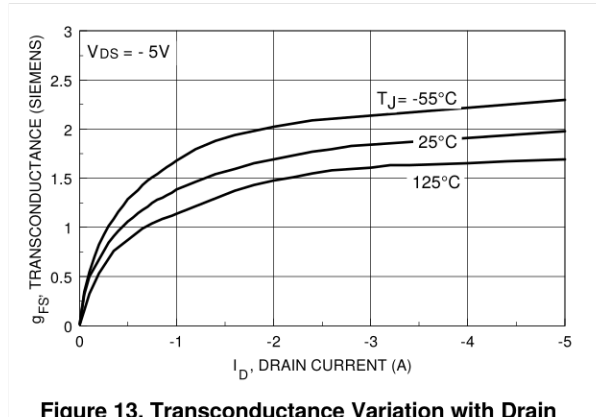


Figure 12. Switching Waveforms.

Typical Electrical Characteristics (continued)



TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACE ^{Ex} TM	FAST □	OPTOLOGIC TM	SMART START TM	VCX TM
Bottomless TM	FAST ^r TM	OPTOPLANAR TM	STAR*POWER TM	
CoolFET TM	FRFET TM	PACMAN TM	Stealth TM	
CROSSVOLT TM	GlobalOptoisolator TM	POP TM	SuperSOT TM -3	
DenseTrench TM	GTO TM	Power247 TM	SuperSOT TM -6	
DOME TM	HiSeC TM	PowerTrench □	SuperSOT TM -8	
EcoSPARK TM	ISOPLANAR TM	QFET TM	SyncFET TM	
E ² CMOS TM	LittleFET TM	QS TM	TinyLogic TM	
EnSigna TM	MicroFET TM	QT Optoelectronics TM	TruTranslation TM	
FACT TM	MicroPak TM	Quiet Series TM	UHC TM	
FACT Quiet Series TM	MICROWIRE TM	SILENT SWITCHER □	UltraFET □	

STAR*POWER is used under license

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.