MN15283

■ Features

• ROM capacity: 8,192 × 8 bits

• RAM capacity: 512 × 4 bits

• Machine cycle:1.91 μ s(4.0 to 5.5 V) $^{\circ}$ 6.15 μ s(3.0 to 5.5 V)

Interrupt:External interrupt

Timer interrupt 1
Serial interrupt 1

Watch/digit interrupt

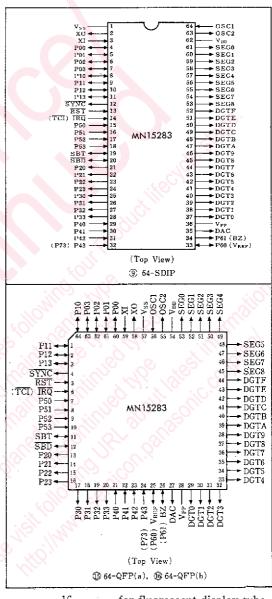
Time base interrupt 1

- Timer/counter: Timer and event count functions provided by 8-bit programmable timer with 7-bit prescaler
- Serial interface: 8-bit synchronous type
- Fluorescent display tube direct drive pins: 16 for digit output, 9 for segment output
- Channel selecting function: 14-bit PWM system
 D/A clonverter
- Buzzer driver circuit incorporated: 2 kHz
- Pulse width measuring circuit incorporated:
 Pulse width measurable
- High impedance control: Port high impedance controllable
- System clock selector circuit incorporated:

 Programmable selection of system
 clock sources enabled. Clock
 sources are OSC1, OSC2 or XI, XO.
- Backup mode: STOP/HALT mode
- Operating voltage range: 3.0 to 5.5 V

• operating	Tortage	range, o.v to o.b v
● I/O pins:	· 8	for general purpose I/O
	10	for general purpose output
	8	for general purpose input
	1 -	for serial data I/O
	1	for serial clock I/O
	1	for buzzer output
	1	for analog input
	1	for V _{REF} input
	1	for PWM output
	9	for fluorescent display, tube
		segment output

■ Pin Configuration



16 for fluorescent display tube
digit output
for LED driver output

- Process: Silicon gate CMOS
- Package: 64-QFP/SDIP

Piggyback: EP15283

■ Pin Descriptions

Pin		Symbol	Pin Name	I/O	Description
64 SDIP	64-QFP			, .	
62 1	54 57	$V_{ t DD} \ V_{ t SS}$	Power supply	I	Connect +3.0-5.5 V to V _{nn} , and O V to V _{ss} .
64 63	56 55	OSC1 OSC2	Clock input Clock output	O	Oscillation terminals to connect fose ceramic oscillator or crystal oscillator. A feedback resistor incorporated between OSCI and OSC2.
3 2	59 58	XO	Clock input Clock output	O	Event counter clock source terminals to connect crystal oscillator. A feedback resistor between XI an XO can be selected with a mask option. They serve a an operating clock source when XI/XO is specified b clock selection.
13	5	RST	Reset input	I	Reset is applied if the "L" level is inputted over 0.3μ A pull-up resistor can be specified with a mas option.
12	4	SYNC	SYNC. signal output	0	An internal timing signal is outputted every machine cycle at reset time.
14	6	IRQ (TCI)	External inter- rupt/pulse input	I	When used as an external interrupt, it receives a interrupt at a negative edge. A time base interrupt results in case of internal interrupt. TCI/IRQ can be selected through an internal port.
19	11	SBT	Serial interface clock I/O	I/O	Serial interface send/receive clock I/O terminal. I serves as an output terminal in the internal cloc mode, and as an input terminal in the external cloc mode. A pull up resistor can be specified with a mas option.
20	12	SBD	Serial interface data I/O	I/O	Serial interface send/receive data I/O terminal. I inputs 8-bit serial data in the receive mode. an outputs 8-bit serial data in the send mode. An output type is either push-pull or N-channel open drai which can be selected with a mask option.
35	27	DAC	D/A converter output	.00	14 bit D/A converter output terminal(PWM system An output type is either push-pull or N-channe which can be selected with a mask option.
4~11	60~64 1~3	P00~P13	Parallel data I/O	I/O	4-bit parallel data I/O ports. Output, I/O or input ca be selected with a mask option. A pull-up resistor ca be specified with a mask option.
21~28	13~20	P20~P33	Parallel data output	0	4-bit parallel data output ports.
29~32 15~18	21~24 7~10	P40~P53	Parallel data input	I	4-bit parallel data input ports. A pull-up resistor ca be specified with a mask option. P50-53 can be als specified for TTL level input with a mask option. P4 and P73 are commonly used.
32	24	P73	Analog input	%I	Input terminal to compare with V _{REP} . P43 and P73 at commonly used.
33 34	25 26	P60(V _{REF}) ~P61 (BZ)	Parallel data output terminal/input	O /I	2-bit parallel data output ports. P60 is the N-channe open drain output(LED directly drivable) and commonly used for V _{REF} . P61 can be specified for buzze output with a mask option.
37~52	29~44	DGT0 ~DGTF	Fluorescent dis- play tube digit output	0	High-voltage output terminal to be connected to fluorescent display tube digit input terminal. Dut can be selected with a mask option. DGT0-4 can be specified for LED drivers with a mask option.

■ Pin Descriptions(Continued)

Pin 64-SDIP	No. 64 QFP	Symbol	Pin Name	I/O	Description
53~61	45~53	SEG0~ SEG8	Fluorescent dis- play tube seg- ment output	0	High-voltage output terminal to be connected to a fluorescent display tube segment input terminal.
36	28	VPP	High voltage power	I	High-voltage output transistor laoding power supply. Normally, Vpp = -30 V.

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