DOUBLE BALANCED MODULATOR/DEMODULATOR

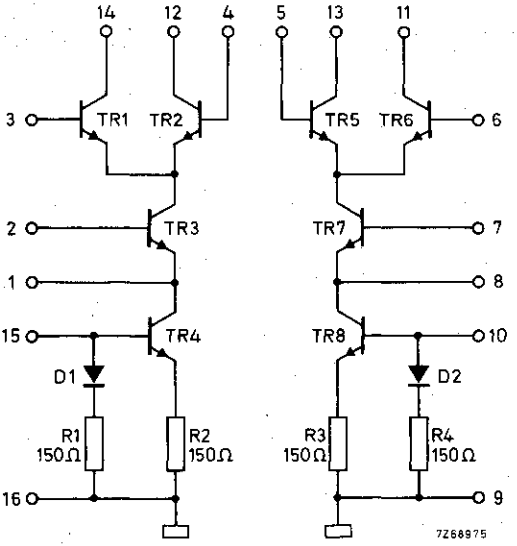
The TCA240 is a monolithic integrated circuit used for general purpose applications, such as:

- modulator
- mixer
- switch/chopper
- a.m. synchronous demodulator
- f.m. quadrature demodulator
- phase comparator
- differential amplifier

The circuit is arranged to offer very flexible circuit design possibilities.
The excellent matching and temperature tracking of the transistors in the circuit allows the use of circuit techniques which are not available when using discrete devices.

PACKAGE OUTLINE plastic 16-lead dual in-line (see general section).

CIRCUIT DIAGRAM



Note

Pins 16 and 9 are connected to the substrate.
When both long tailed pairs are used connect pin 9 with pin 16 externally.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages (each transistor)

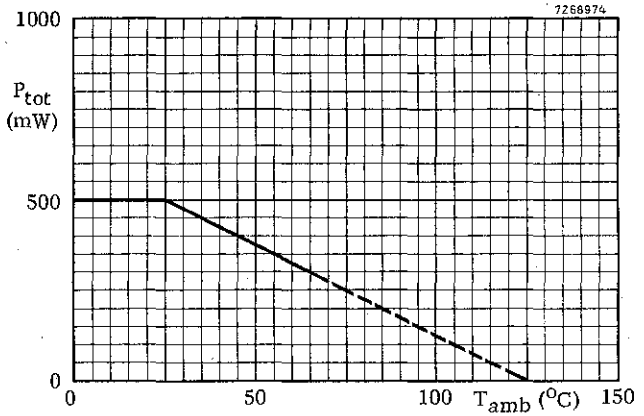
Collector-substrate voltage (open base and emitter)	V_{CSO}	max.	16	V
Collector-base voltage (open emitter)	V_{CBO}	max.	16	V
Collector-emitter voltage (open base)	V_{CEO}	max.	12	V
Emitter-base voltage (open collector)	V_{EBO}	max.	5	V

Currents (each transistor)

Emitter current	I_E	max.	10	mA
Base current	I_B	max.	10	mA

RATINGS (continued)

Total power dissipation (mounted on a printed-wiring board)



Temperatures

Storage temperature	T_{stg}	−55 to +125		°C
Operating ambient temperature	T_{amb}	−20 to +70		°C
Crystal temperature	T_c	max.	125	°C

THERMAL RESISTANCE

From crystal to ambient	$R_{th\ j\text{-}a}$	=	200	°C/W

CHARACTERISTICS at $V_{11-9} = V_{13-9} = V_{12-16} = V_{14-16} = 12$ V;
$V_{3-16} = V_{4-16} = V_{5-9} = V_{6-9} = 6$ V; $V_{2-16} = V_{7-9} = 4$ V;
$T_{amb} = 25$ °C; unless otherwise specified

Collector current difference				
between transistors TR4 and TR8 $I_{10} = I_{15} = 1,5$ mA	$\lvert I_{C4} - I_{C8} \rvert$	<	0,07	mA
Base-emitter voltage				
of transistors TR3 and TR7 $I_1 = I_8 = -1$ mA	$V_{BE3}; V_{BE7}$		690 to 770	mV
Base-emitter voltage difference				
between transistors TR1 and TR2 $V_{12-16} = V_{14-16} = 10$ V; $I_{15} = 1,5$ mA	$\lvert V_{BE1} - V_{BE2} \rvert$	<	2,5	mV
between transistors TR5 and TR6 $V_{11-9} = V_{13-9} = 10$ V; $I_{10} = 1,5$ mA	$\lvert V_{BE5} - V_{BE6} \rvert$	<	2,5	mV
between the parallel connection of TR1, TR5 and TR2, TR6 $V_{11-9} = V_{13-9} = V_{12-16} = V_{14-16} = 8$ V $I_1 + I_8 = -3$ mA	$\lvert V_{BE1;5} - V_{BE2;6} \rvert$	<	2,1	mV
D.C. current gain				
of transistors TR3 and TR7 $I_1 + I_8 = -3$ mA	h_{FE3}, h_{FE7}		23 to 190	
D.C. current gain ratio				
of transistors TR3 and TR7 $I_1 + I_8 = -3$ mA	$\left\lvert \frac{h_{FE3} - h_{FE7}}{h_{FE3} + h_{FE7}} \right\rvert \times 200$		0 to 60	%
D.C. current gain				
of transistors TR1, TR2, TR5 and TR6 $I_E = 750$ µA	$h_{FE1}, h_{FE2}, h_{FE5}, h_{FE6}$		23 to 190	
D.C. current gain ratio				
of transistors TR1 and TR2 $I_1 = -1,5$ mA	$\left\lvert \frac{h_{FE1} - h_{FE2}}{h_{FE1} + h_{FE2}} \right\rvert \times 200$		0 to 60	%
of transistors TR5 and TR6 $I_8 = -1,5$ mA	$\left\lvert \frac{h_{FE5} - h_{FE6}}{h_{FE5} + h_{FE6}} \right\rvert \times 200$		0 to 60	%

CHARACTERISTICS (continued)

D.C. current gain

of the parallel connection of TR1 and TR6 at $I_1 + I_8 = -3$ mA	h_{FE1}, h_{FE6}	23 to 190	
of the parallel connection of TR2 and TR5 at $I_1 + I_8 = -3$ mA	h_{FE2}, h_{FE5}	23 to 190	

D.C. current gain ratio

of the parallel connection of TR1, TR6 and TR2, TR5 $I_1 + I_8 = -3$ mA	$\left\lvert \frac{h_{FE1;6} - h_{FE2;5}}{h_{FE1;6} + h_{FE2;5}} \right\rvert \times 200$	0 to 60	%

DYNAMIC DESIGN DATA

Noise figure at f = 100 MHz

$I_C = 1$ mA; $V_{CB} = 5$ V; $G_s = 3,7$ mA/V; $B_s = -2,5$ mA/V	F	<	3,7	dB
$I_E = 2,5$ mA; $V_{CB} = 5$ V; $G_s = 6,5$ mA/V; $B_s = -2,5$ mA/V	F	<	4,2	dB

y parameters

$V_{CE} = 5$ V; f = 100 MHz			$I_E = 1$ mA	$I_E = 5$ mA	
Input conductance	g_{ie}	typ.	4,4	13,6	mA/V
Input susceptance	b_{ie}	typ.	7,6	9	mA/V
Feedback admittance	$\lvert y_{re} \rvert$	typ.	0,4	0,4	mA/V
Phase angle of feedback admittance	$-\varphi_{re}$	typ.	100°	100°	
Transfer admittance	$\lvert y_{fe} \rvert$	typ.	22	55	mA/V
Phase angle of feedback admittance	$-\varphi_{fe}$	typ.	45°	96°	
Output conductance	g_{oe}	typ.	0,4	0,5	mA/V
Output susceptance	b_{oe}	typ.	1,8	1,8	mA/V

Frequency response (see circuit on page 6)

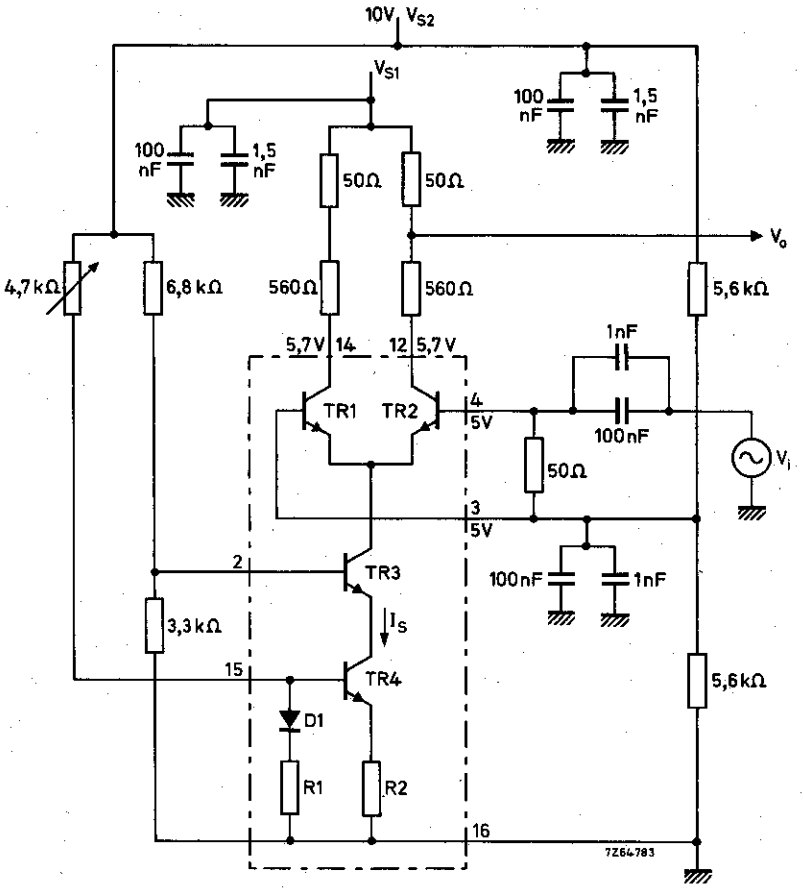
$I_S = 5$ mA; $R_C = 600\ \Omega$; f = −3 dB	f	typ.	34	MHz

Switching times (see circuit on page 7)

	I_S =		0,5	1	2	4	mA
Rise time	t_r	typ.	2,9	2,7	2,7	3,1	ns
Fall time	t_f	typ.	1,4	1,3	1,6	2,3	ns
Rise propagation delay time [1]	t_{pdr}	typ.	1,1	1,2	1,4	1,7	ns
Fall propagation delay time [1]	t_{pdf}	typ.	1,1	1,2	1,4	1,7	ns

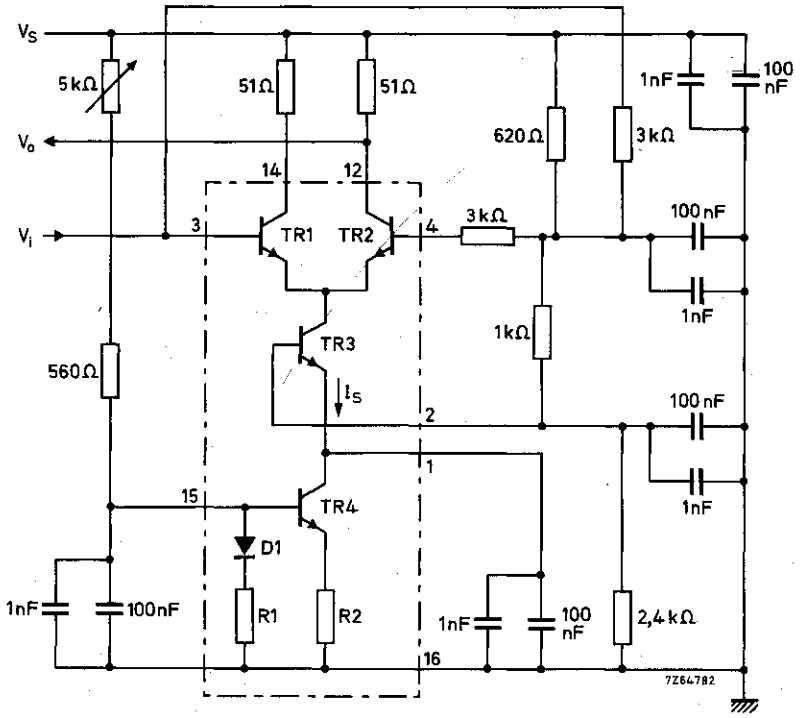
[1] Reference level 50 %.

DYNAMIC DESIGN DATA (continued)



Circuit for measuring the frequency response

DYNAMIC DESIGN DATA (continued)



Circuit for measuring t_r, t_f, t_{pdr} and t_{pdf}