

82S185 8K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S185 is field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The standard 82S185 is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 1 chip enable input for memory expansion. It features Three-state outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S185 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

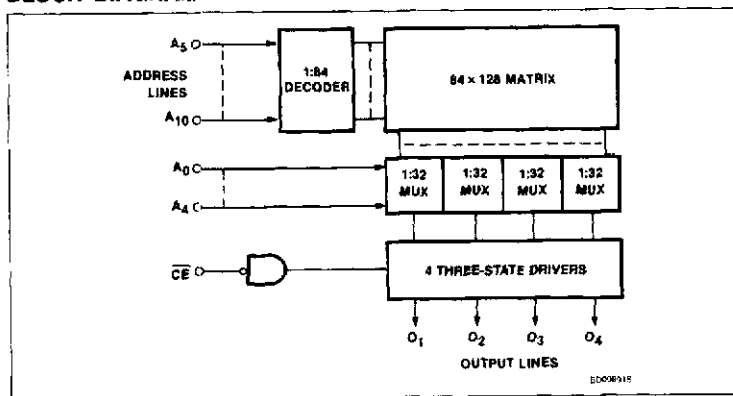
FEATURES

- Low power dissipation: 50 μ W/bit typ
- Address access time: 100ns max
- Input loading: $\sim 100\mu$ A max
- On-chip address decoding
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible
- One chip enable input
- Outputs: Three-state

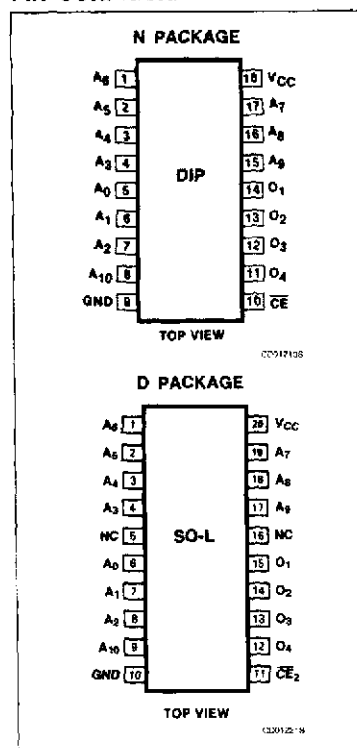
APPLICATIONS

- Sequential controllers
- Control store
- Random logic
- Code conversion

BLOCK DIAGRAM



PIN CONFIGURATION



8K-Bit TTL Bipolar PROM (2048 x 4)

82S185

ORDERING CODE

DESCRIPTION	ORDER CODE
Plastic Dual Inline 300mil wide 18-pin	N82S185 N
Plastic Small Outline 300mil wide 20-pin	N82S185 D

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	V _{dc}
V _{IN} Input voltage	+5.5	V _{dc}
V _O Output voltage Off-state	+5.5	V _{dc}
T _A Temperature range Operating	0 to +75	°C
T _{STG} Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS ^{1,2}	LIMITS			UNIT
		Min	Typ ⁵	Max	
Input voltage¹ V _{IL} Low V _{IH} High V _{IC} Clamp	I _{IN} = -12mA	2.0	-0.8	0.8 -1.2	V
Output voltage¹ V _{OL} Low V _{OH} High	CE = Low I _{OUT} = 16mA I _{OUT} = -2mA	2.4		0.45	V
Input current² I _{IL} Low I _{IH} High	V _{IN} = 0.45V V _{IN} = 5.5V			-100 40	μA
Output current I _{OZ} Hi-Z State I _{OS} Short circuit ³	CE = High, V _{OUT} = 0.5V, CE = High, V _{OUT} = 5.5V CE = Low, V _{OUT} = 0V High stored	-15		-40 40 -70	μA mA
Supply current I _{CC}	V _{CC} = 5.25V		90	120	mA
Capacitance C _{IN} Input C _{OUT} Output	CE = High, V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8		pF

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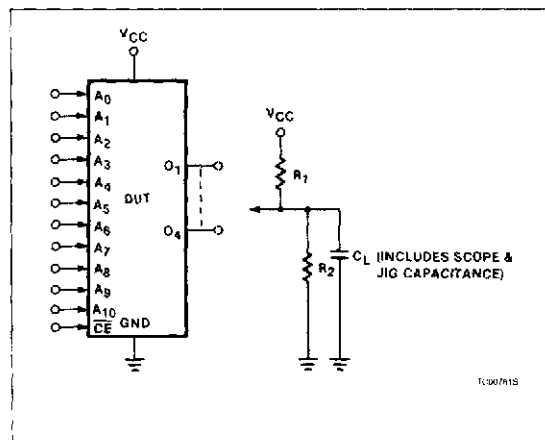
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AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30\text{pF}$, $0^\circ\text{C} \leq T_A \leq +75^\circ\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$

PARAMETER	TO	FROM	LIMITS			UNIT
			Min	Typ ⁵	Max	
Access time⁴ T_{AA} T_{CE}	Output Output	Address Chip Enable		70 30	100 40	ns
Disable time⁶ T_{CD}	Output	Chip disable		30	40	ns

NOTES:

1. All voltage values are with respect to network ground terminal.
2. Positive current is defined as into the terminal referenced.
3. Duration of the short circuit should not exceed 1 second.
4. Tested at an address cycle time of $1\mu\text{sec}$.
5. All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5\text{pF}$.

TEST LOAD CIRCUIT**VOLTAGE WAVEFORM**