

FEBRUARY 1975

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 82S25 is a 64-bit, Schottky clamped TTL, Read-Write Random Access Memory ideal for use in scratch pad and high-speed buffer memory applications.

The 82S25 is a fully decoded memory array organized as 16 words of 4 bits each, with separate input and output lines. It features PNP inputs, one chip enable line, and open collector outputs for ease of memory expansion.

The outputs of the 82S25 assume a logic "1" state during write. This allows both memory inputs and outputs to share a common bus for minimizing interconnections, and more effective utilization of common I/O circuitry.

The 82S25 is available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S25, B or F. For the military temperature range (-55°C to +125°C) specify S82S25, F only.

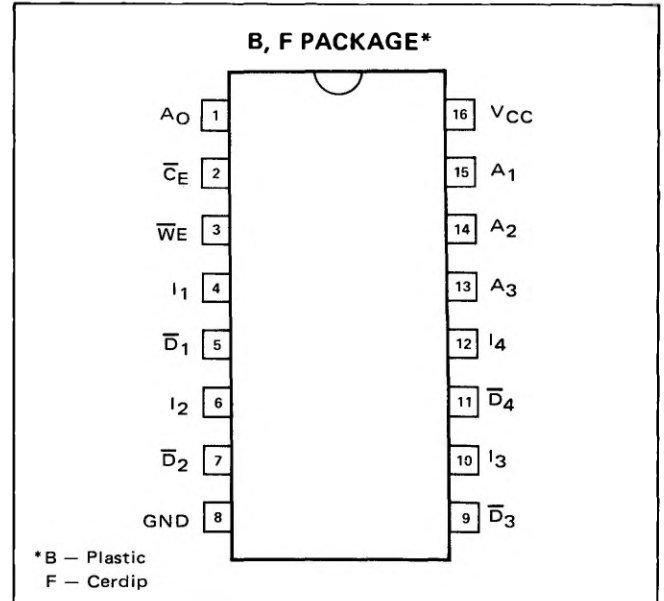
FEATURES

- ORGANIZATION – 16 X 4
- ADDRESS ACCESS TIME:
S82S25 – 60ns, MAXIMUM
N82S25 – 50ns, MAXIMUM
- WRITE CYCLE TIME:
S82S25 – 50ns, MAXIMUM
N82S25 – 35ns, MAXIMUM
- POWER DISSIPATION – 6.25mW/BIT, TYPICAL
- INPUT LOADING:
S82S25 – (-150µA) MAXIMUM
N82S25 – (-100µA) MAXIMUM
- OUTPUT BLANKING DURING WRITE
- ON-CHIP ADDRESS DECODING
- OPEN COLLECTOR OUTPUTS
- 16 PIN CERAMIC DIP

APPLICATIONS

- SCRATCH PAD MEMORY
- BUFFER MEMORY
- PUSH DOWN STACKS
- CONTROL STORE

PIN CONFIGURATION

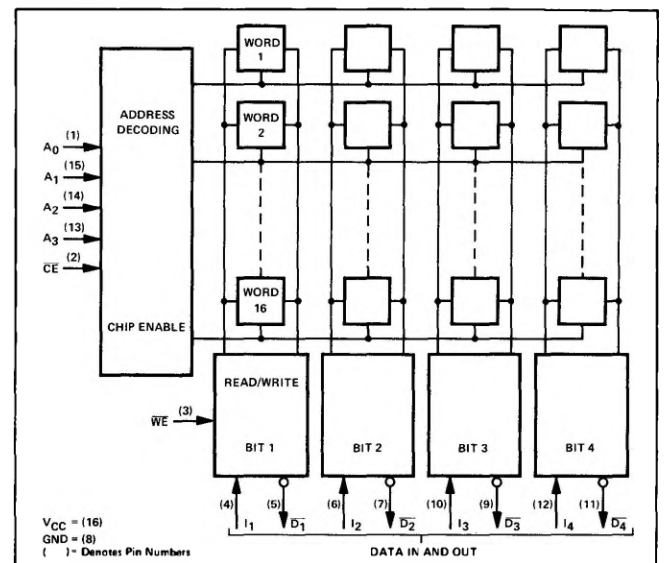


TRUTH TABLE

MODE	\overline{CE}	\overline{WE}	I_n	\overline{D}_n
Read	0	1	X	Complement of data stored
Write "0"	0	0	0	1
Write "1"	0	0	1	1
Disabled	1	X	X	1

X = Don't care.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER ¹	RATING	UNIT
V _{CC} Power Supply Voltage	+7	Vdc
V _{in} Input Voltage	+5.5	Vdc
V _{OH} High Level Output Voltage	+5.5	Vdc
T _A Operating Temperature Range (N82S25)	0° to +75°	°C
(S82S25)	-55° to +125°	°C
T _{stg} Storage Temperature Range	-65° to +150°	°C

ELECTRICAL CHARACTERISTICS S82S25 -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V
 N82S25 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS	S82S25 ^{1,2,3}			N82S25 ^{1,2,3}			UNIT
		MIN	TYP ⁸	MAX	MIN	TYP ⁸	MAX	
I _{IL} "0" Input Current	V _{IN} = 0.45V		-10	-150		-10	-100	μA
I _{IH} "1" Input Current	V _{IN} = 5.5V			25			10	μA
V _{IL} "0" Level Input Voltage	V _{CC} = MIN			.80			.85	V
V _{IH} "1" Level Input Voltage	V _{CC} = MAX	2.0			2.0			V
V _{IC} Input Clamp Voltage	I _{IN} = -12mA, V _{CC} = MIN (Note 6)		-1.0	-1.5		-1.0	-1.5	V
V _{OL} "0" Output Voltage	I _{OUT} = 16mA, V _{CC} = MIN (Notes 4, 5)		0.35	0.5		0.35	0.45	V
C _{IN} Input Capacitance	V _{IH} = 2.0V, V _{CC} = 5.0V		5			5		pF
C _{OUT} Output Capacitance	V _{OUT} = 2.0V, V _{CC} = 5.0V, CE = "1"		8			8		pF
I _{CC} Power Supply Current	(Note 5)		80	120		80	105	mA
I _{OLK} Output Leakage Current	CE = "1", V _{OUT} = 5.5V, V _{CC} = MIN		<1	100		<1.0	100	μA

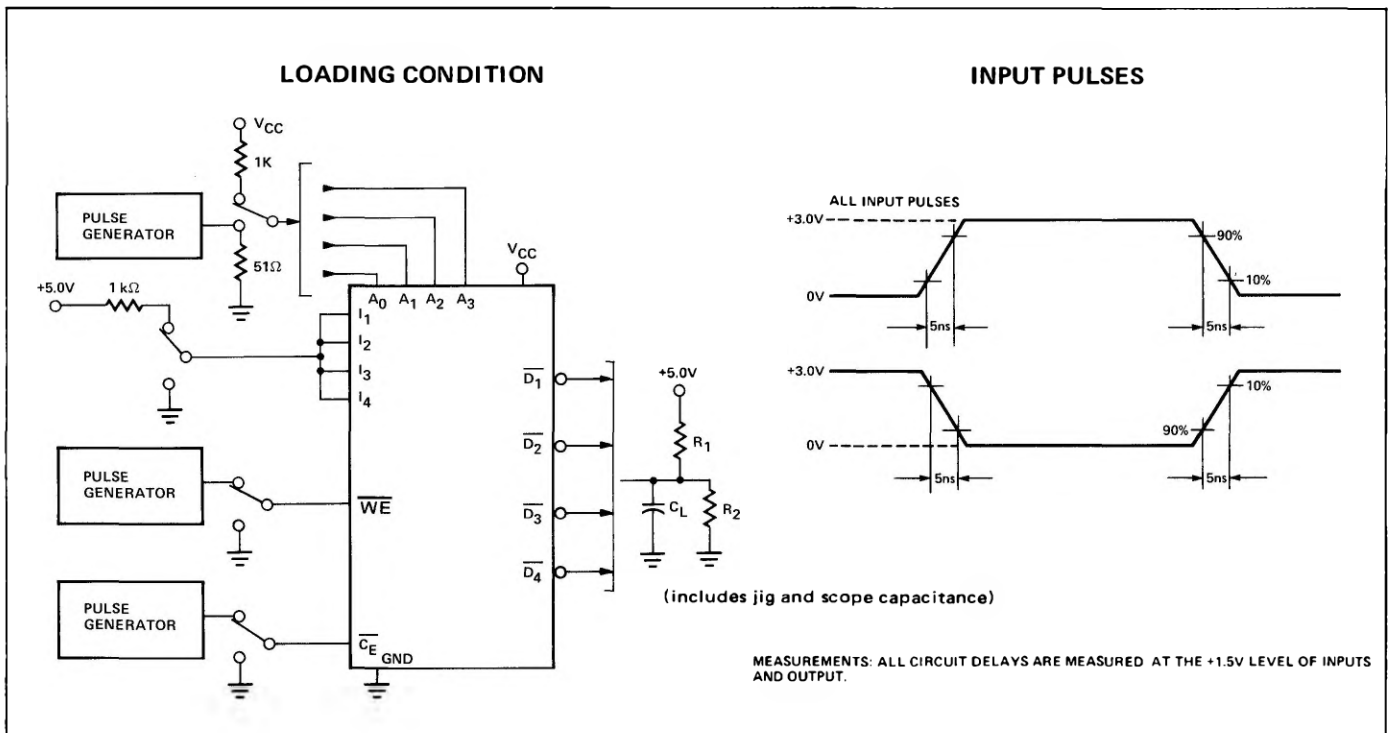
NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Positive current is defined as into the terminal referenced.
3. Positive logic definition: "1" = HIGH ≈ +5.0V; "0" = LOW ≈ GRD.
4. Output sink current is supplied through a resistor to V_{CC}.
5. All sense outputs in "0" state.
6. Test each input one at a time.
7. To guarantee a WRITE into the slowest bit.
8. Typical values are at V_{CC} = +5.0V and T_A = +25°C.

SWITCHING CHARACTERISTICS S82S25 $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$
 N82S25 $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$

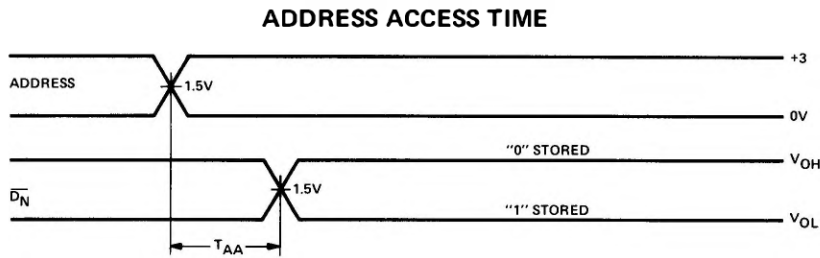
PARAMETER	TEST CONDITIONS	S82S25			N82S25			UNIT
		MIN	TYP ⁸	MAX	MIN	TYP ⁸	MAX	
Propagation Delays								
T _{AA}	Address Access Time		35	60		35	50	ns
T _{CE}	Chip Enable Access Time		20	35		20	35	ns
T _{CD}	Chip Enable Output Disable Time		20	35		20	35	ns
T _{WD}	Write Enable to Output Disable Time		20	30		20	25	ns
T _{WR}	Write Recovery Time		35	60		35	50	ns
Write Set-up Times								
		R ₁ = 270Ω R ₂ = 600Ω C _L = 30pF						
T _{WSA}	Address to Write Enable	10	-8		0	-8		ns
T _{WSD}	Data In to Write Enable	25	5		20	5		ns
T _{WSC}	$\overline{\text{CE}}$ to Write Enable	0	-5		0	-5		ns
Write Hold Times								
T _{WHA}	Address to Write Enable	10	0		5	0		ns
T _{WHD}	Data In to Write Enable	10	-3		5	-3		ns
T _{WHC}	$\overline{\text{CE}}$ to Write Enable	5	0		5	0		ns
T _{WP}	Write Enable Pulse Width (Note 7)	30	18		30	18		ns

AC TEST LOAD AND WAVEFORMS

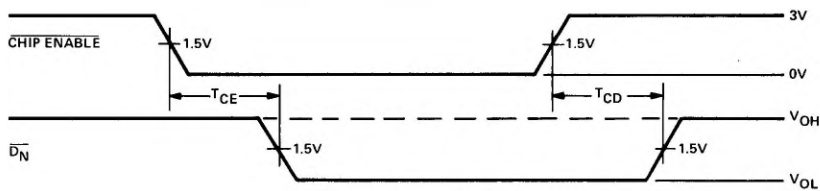


SWITCHING PARAMETERS MEASUREMENT INFORMATION

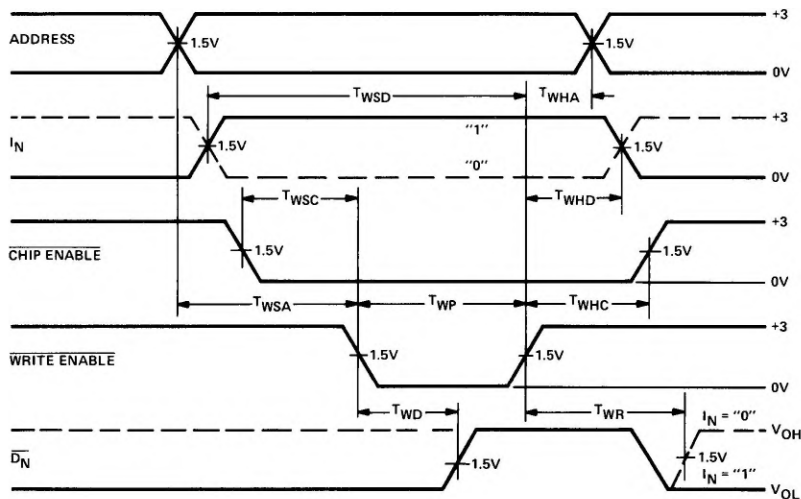
READ CYCLE



CHIP ENABLE/DISABLE TIMES



WRITE CYCLE



MEMORY TIMING DEFINITIONS

- T_{WR} Delay between end of WRITE ENABLE pulse and when DATA OUTPUT becomes valid. (Assuming ADDRESS still valid — not as shown.)
- T_{CE} Delay between beginning of CHIP ENABLE low (with ADDRESS valid) and when DATA OUTPUT becomes valid.
- T_{CD} Delay between when CHIP ENABLE becomes high and DATA OUTPUT is in off state.
- T_{AA} Delay between beginning of valid ADDRESS (with CHIP ENABLE low) and when DATA OUTPUT becomes valid.
- T_{WSC} Required delay between beginning of valid CHIP ENABLE and beginning of WRITE ENABLE pulse.

- T_{WHD} Required delay between end of WRITE ENABLE pulse and end of valid INPUT DATA.
- T_{WHP} Width of WRITE ENABLE pulse.
- T_{WSA} Required delay between beginning of valid ADDRESS and beginning of WRITE ENABLE pulse.
- T_{WSD} Required delay between beginning of valid DATA INPUT and end of WRITE ENABLE pulse.
- T_{WD} Delay between beginning of WRITE ENABLE pulse and when DATA OUTPUT is in off state.
- T_{WHC} Required delay between end of WRITE ENABLE pulse and end of CHIP ENABLE.
- T_{WHA} Required delay between end of WRITE ENABLE pulse and end of valid ADDRESS.