# STB38N65M5, STP38N65M5, STW38N65M5

## N-channel 650 V, 0.073 Ω typ., 30 A MDmesh™ V Power MOSFETs in D²PAK, TO-220 and TO-247 packages

**Datasheet - production data**

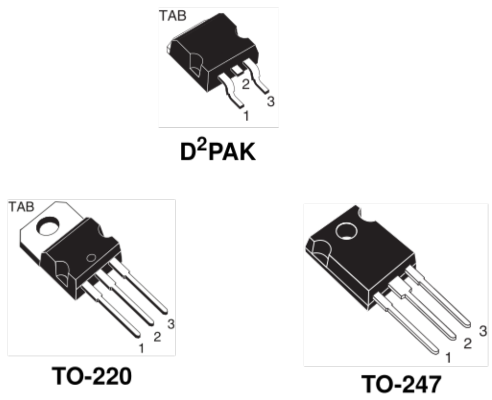
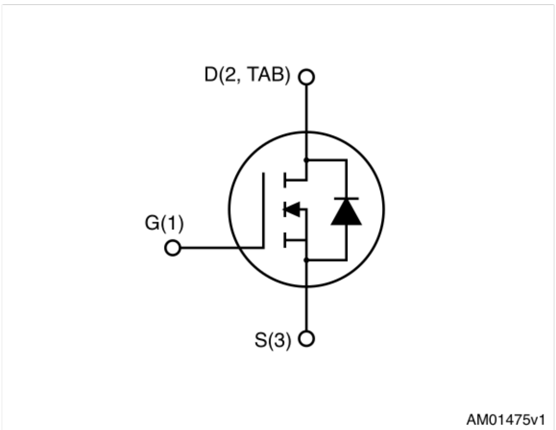



**Figure 1. Internal schematic diagram**




## Features

| Order codes | $V_{DS}$ @ $T_{Jmax}$ | $R_{DS(on)}$ max | $I_D$ |
|---|---|---|---|
| STB38N65M5 | 710 V | 0.095 Ω | 30 A |
| STP38N65M5 | | | |
| STW38N65M5 | | | |

- Higher $V_{DSS}$ rating and high dv/dt capability
- Excellent switching performance
- 100% avalanche tested

## Applications

- Switching applications

## Description

These devices are N-channel MDmesh™ V Power MOSFETs based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

**Table 1. Device summary**

| Order codes | Marking | Package | Packaging |
|---|---|---|---|
| STB38N65M5 | 38N65M5 | D²PAK | Tape and reel |
| STP38N65M5 | | TO-220 | Tube |
| STW38N65M5 | | TO-247 | |



This is information on a product in full production.

# Contents

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{GS}$ | Gate-source voltage | ± 25 | V |
| $I_D$ | Drain current (continuous) at $T_C$ = 25 °C | 30 | A |
| $I_D$ | Drain current (continuous) at $T_C$ = 100 °C | 19 | A |
| $I_{DM}$ (1) | Drain current (pulsed) | 120 | A |
| $P_{TOT}$ | Total dissipation at $T_C$ = 25 °C | 190 | W |
| dv/dt (2) | Peak diode recovery voltage slope | 15 | V/ns |
| dv/dt (3) | MOSFET dv/dt ruggedness | 50 | V/ns |
| $T_{stg}$ | Storage temperature | - 55 to 150 | °C |
| $T_j$ | Max. operating junction temperature | 150 | °C |

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq$ 30 A, di/dt $\leq$ 400 A/µs; $V_{Peak} < V_{(BR)DSS}$, $V_{DD}$ = 400 V
3. $V_{DS} \leq$ 520 V

**Table 3. Thermal data**

| Symbol | Parameter | Value | | | Unit |
|---|---|---|---|---|---|
| | | $D^2PAK$ | TO-220 | TO-247 | |
| $R_{thj-case}$ | Thermal resistance junction-case max | 0.66 | | | °C/W |
| $R_{thj-pcb}$ | Thermal resistance junction-pcb max(1) | 30 | | | °C/W |
| $R_{thj-amb}$ | Thermal resistance junction-ambient max | | 62.5 | 50 | °C/W |

1. 1.When mounted on 1inch² FR-4 board, 2 oz Cu.

**Table 4. Avalanche characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $I_{AR}$ | Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$) | 8 | A |
| $E_{AS}$ | Single pulse avalanche energy (starting $t_j$ = 25°C, $I_d$= $I_{AR}$; $V_{dd}$= 50V) | 660 | mJ |

# 2 Electrical characteristics

($T_C$ = 25 °C unless otherwise specified)

**Table 5. On /off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $I_D$ = 1 mA, $V_{GS}$ = 0 | 650 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current ($V_{GS}$ = 0) | $V_{DS}$ = 650 V | | | 1 | µA |
| | | $V_{DS}$ = 650 V, $T_C$=125 °C | | | 100 | µA |
| $I_{GSS}$ | Gate-body leakage current ($V_{DS}$ = 0) | $V_{GS}$ = ± 25 V | | | ± 100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 3 | 4 | 5 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS}$ = 10 V, $I_D$ = 15 A | | 0.073 | 0.095 | Ω |

**Table 6. Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input capacitance | $V_{DS}$ = 100 V, f = 1 MHz, $V_{GS}$ = 0 | - | 3000 | - | pF |
| $C_{oss}$ | Output capacitance | | - | 74 | - | pF |
| $C_{rss}$ | Reverse transfer capacitance | | - | 5.8 | - | pF |
| $C_{o(tr)}$(1) | Equivalent capacitance time related | $V_{DS}$ = 0 to 520 V, $V_{GS}$ = 0 | - | 244 | - | pF |
| $C_{o(er)}$(2) | Equivalent capacitance energy related | | - | 70 | - | pF |
| $R_G$ | Intrinsic gate resistance | f = 1 MHz open drain | - | 2.4 | - | Ω |
| $Q_g$ | Total gate charge | $V_{DD}$ = 520 V, $I_D$ = 15 A, $V_{GS}$ = 10 V (see *Figure 18*) | - | 71 | - | nC |
| $Q_{gs}$ | Gate-source charge | | - | 18 | - | nC |
| $Q_{gd}$ | Gate-drain charge | | - | 30 | - | nC |

1. Time related is defined as a constant equivalent capacitance giving the same charging time as $C_{oss}$ when $V_{DS}$ increases from 0 to 80% $V_{DSS}$
2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as $C_{oss}$ when $V_{DS}$ increases from 0 to 80% $V_{DSS}$

**Table 7. Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d\ (v)}$ | Voltage delay time | $V_{DD}$ = 400 V, $I_D$ = 20 A, $R_G$ = 4.7 Ω, $V_{GS}$ = 10 V (see *Figure 19* and *Figure 22*) | - | 66 | - | ns |
| $t_{r\ (v)}$ | Voltage rise time | | - | 9 | - | ns |
| $t_{f\ (i)}$ | Current fall time | | - | 9 | - | ns |
| $t_{c(off)}$ | Crossing time | | - | 13 | - | ns |

**Table 8. Source drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain current | | - | | 30 | A |
| $I_{SDM}$ (1) | Source-drain current (pulsed) | | - | | 120 | A |
| $V_{SD}$ (2) | Forward on voltage | $I_{SD}$ = 30 A, $V_{GS}$ = 0 | - | | 1.5 | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 30 A, di/dt = 100 A/μs $V_{DD}$ = 100 V (see *Figure 22*) | - | 382 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 6.6 | | μC |
| $I_{RRM}$ | Reverse recovery current | | - | 35 | | A |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 30 A, di/dt = 100 A/μs $V_{DD}$ = 100 V, $T_j$ = 150 °C (see *Figure 22*) | - | 522 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 10.3 | | μC |
| $I_{RRM}$ | Reverse recovery current | | - | 40 | | A |

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs, duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

**Figure 2. Safe operating area for D²PAK and TO-220**

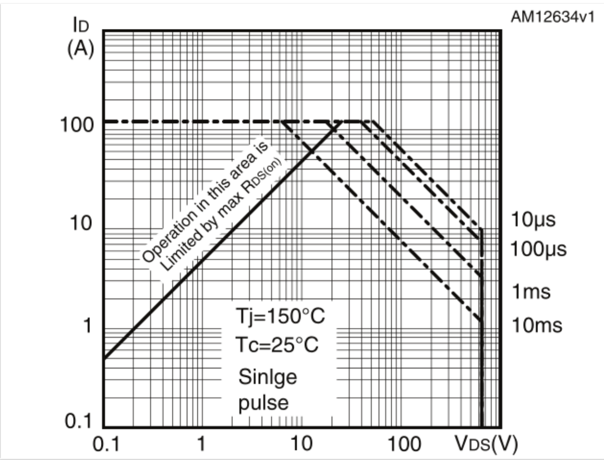



**Figure 3. Thermal impedance for D²PAK and TO-220**

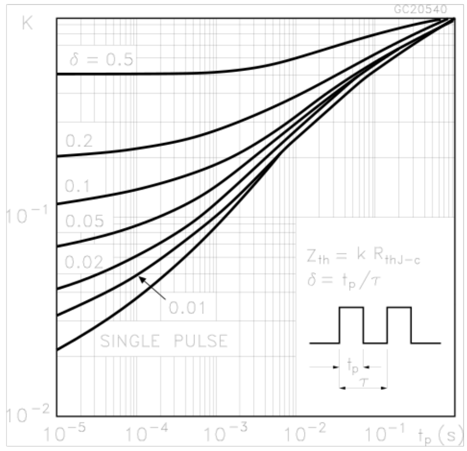



**Figure 4. Safe operating area for TO-247**

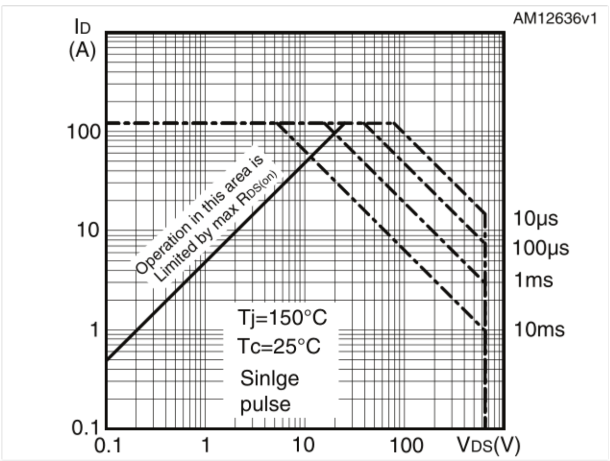



**Figure 5. Thermal impedance for TO-247**

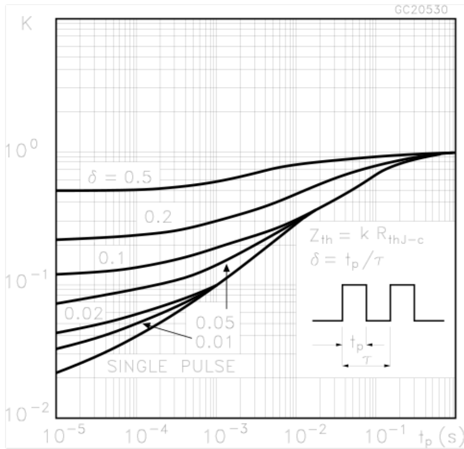



**Figure 6. Output characteristics**

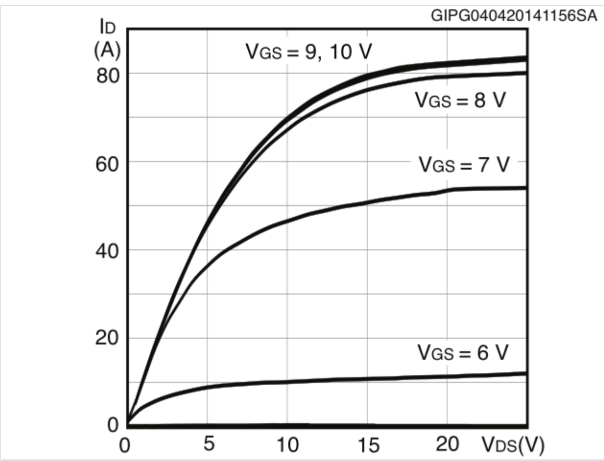



**Figure 7. Transfer characteristics**

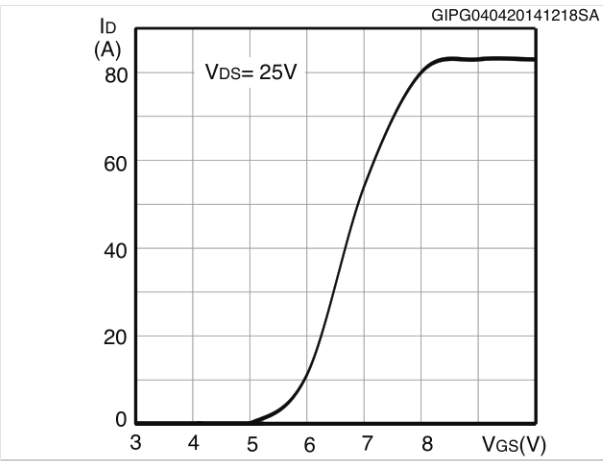


**Figure 8. Gate charge vs gate-source voltage**

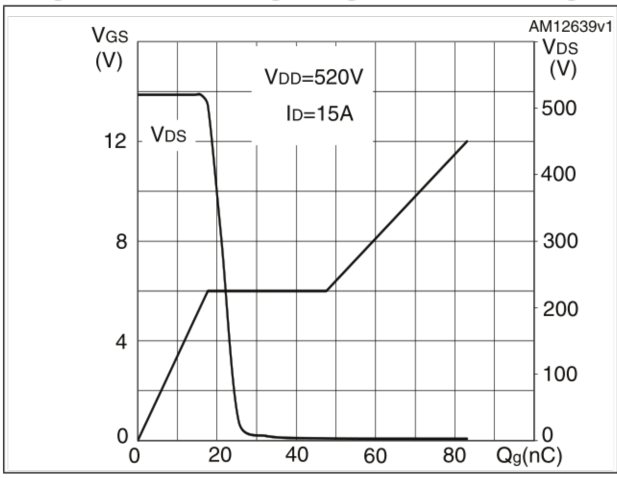



**Figure 9. Static drain-source on-resistance**

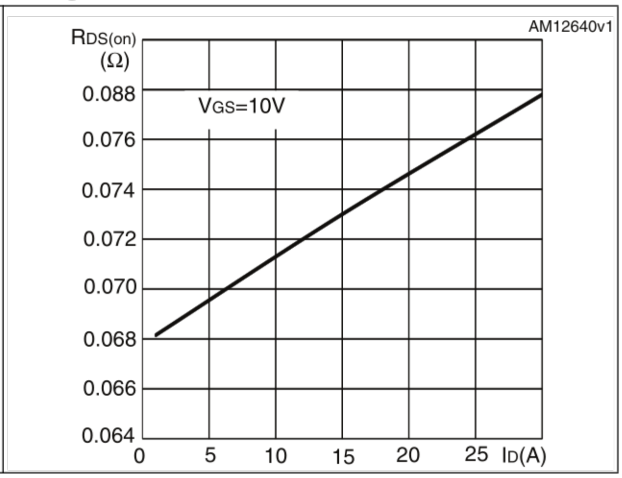



**Figure 10. Capacitance variations**

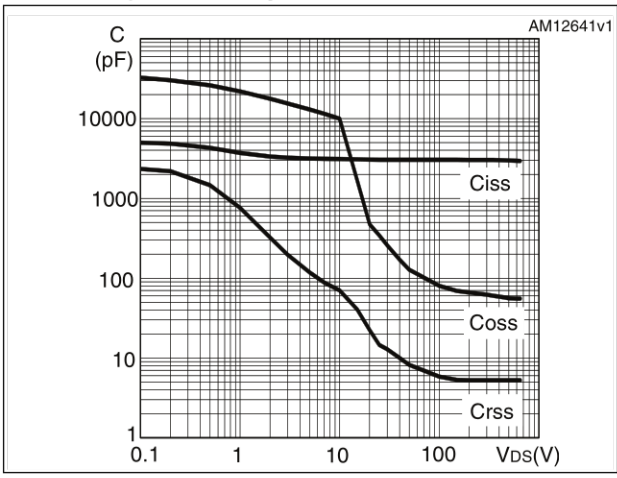



**Figure 11. Output capacitance stored energy**

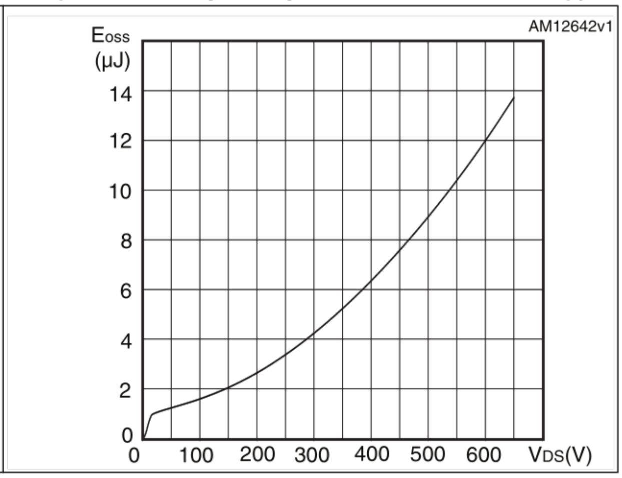



**Figure 12. Normalized gate threshold voltage vs temperature**

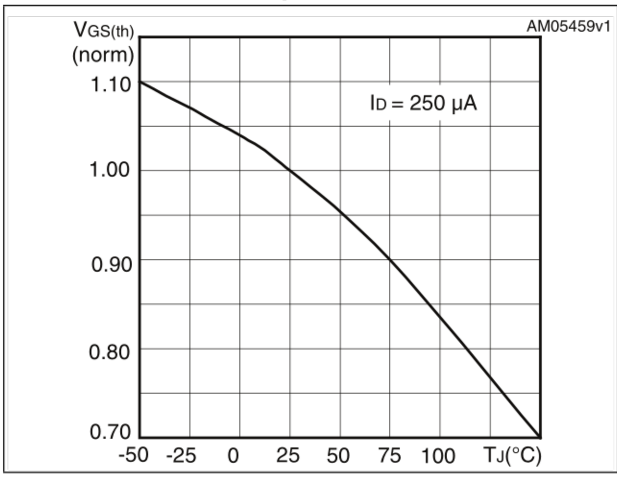



**Figure 13. Normalized on-resistance vs temperature**

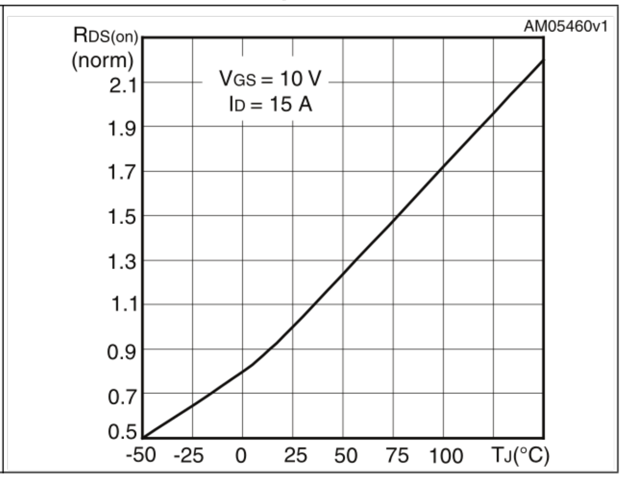


**Figure 14. Source-drain diode forward characteristics**

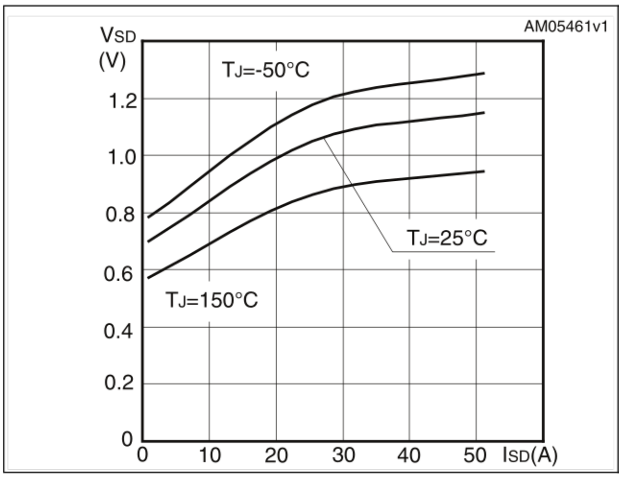



**Figure 15. Normalized $V_{(BR)DSS}$ vs temperature**

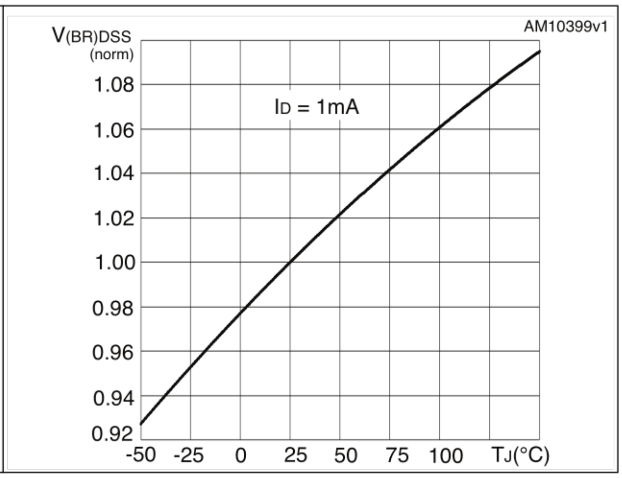
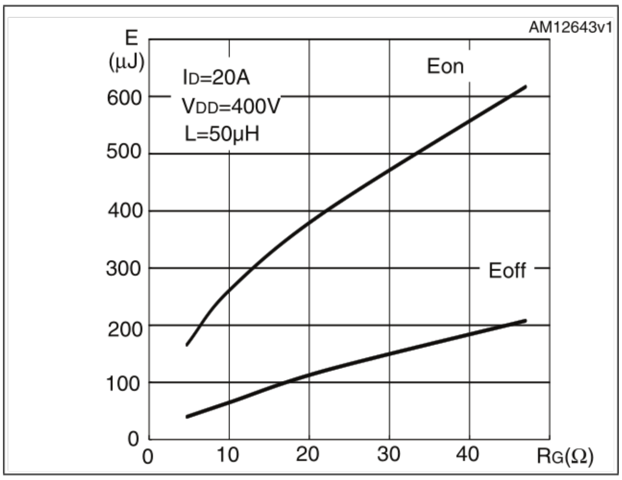



**Figure 16. Switching losses vs gate resistance (1)**




1. Eon including reverse recovery of a SiC diode.

# 3 Test circuits

**Figure 17. Switching times test circuit for resistive load**

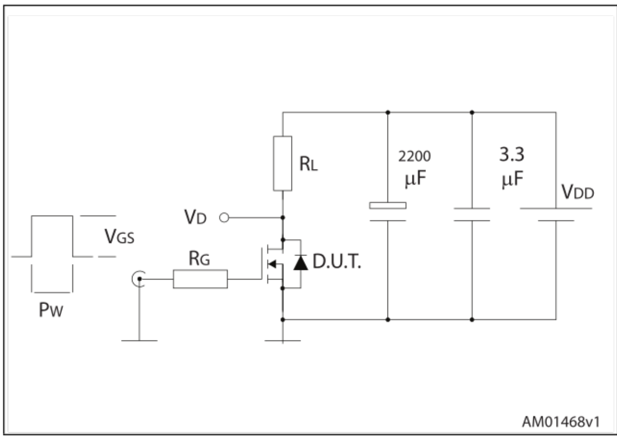



**Figure 18. Gate charge test circuit**

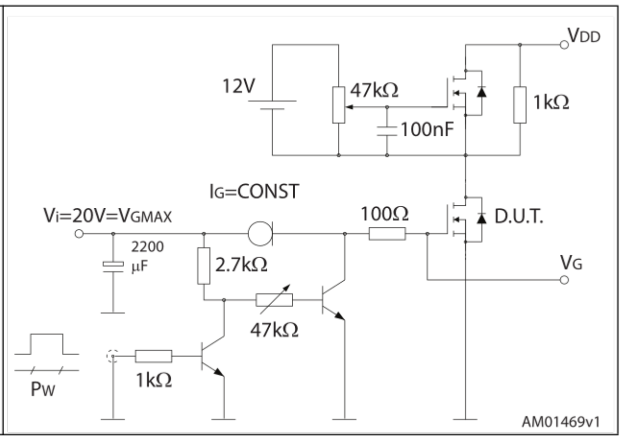



**Figure 19. Test circuit for inductive load switching and diode recovery times**

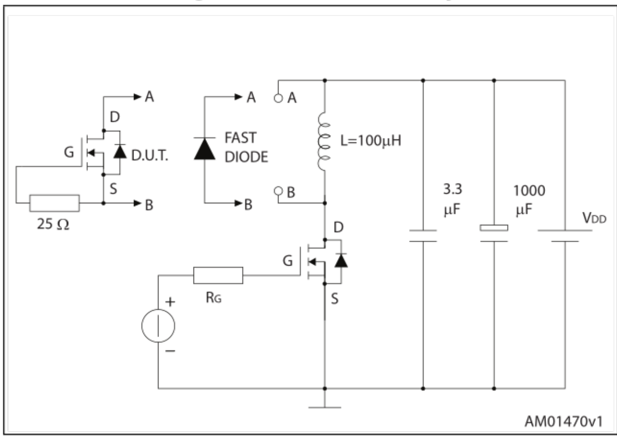



**Figure 20. Unclamped inductive load test circuit**

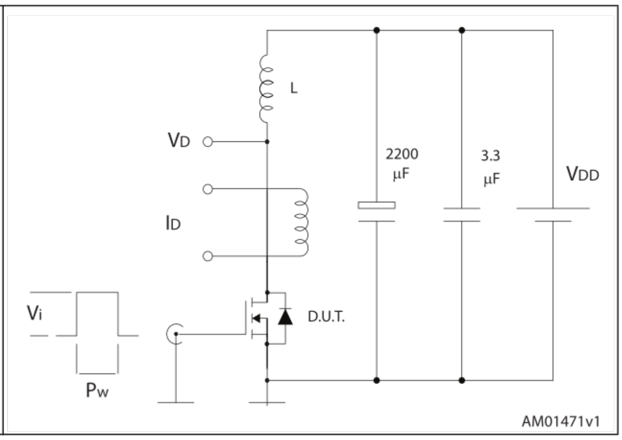



**Figure 21. Unclamped inductive waveform**

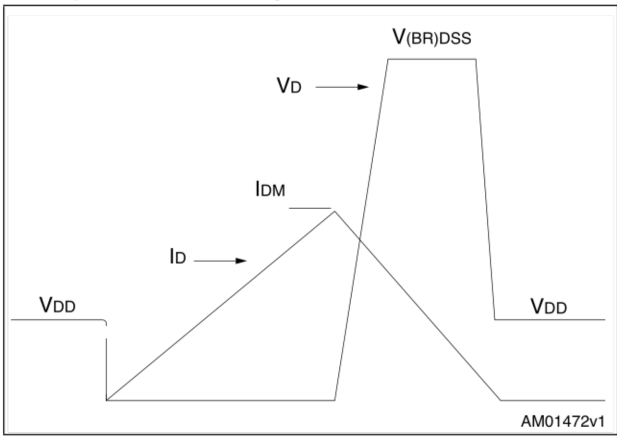
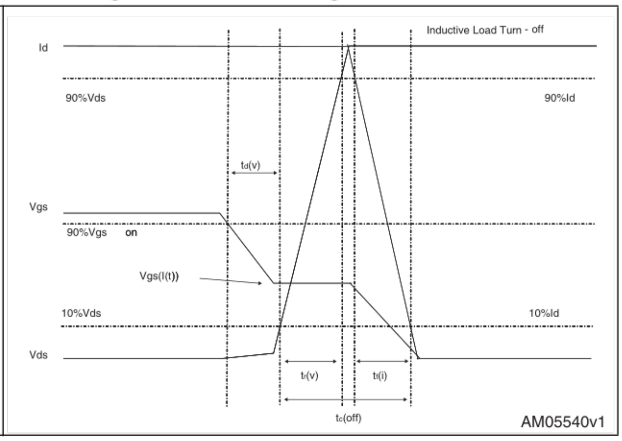



**Figure 22. Switching time waveform**



# 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

## 4.1 D²PAK, STB38N65M5

**Figure 23. D²PAK (TO-263) drawing**

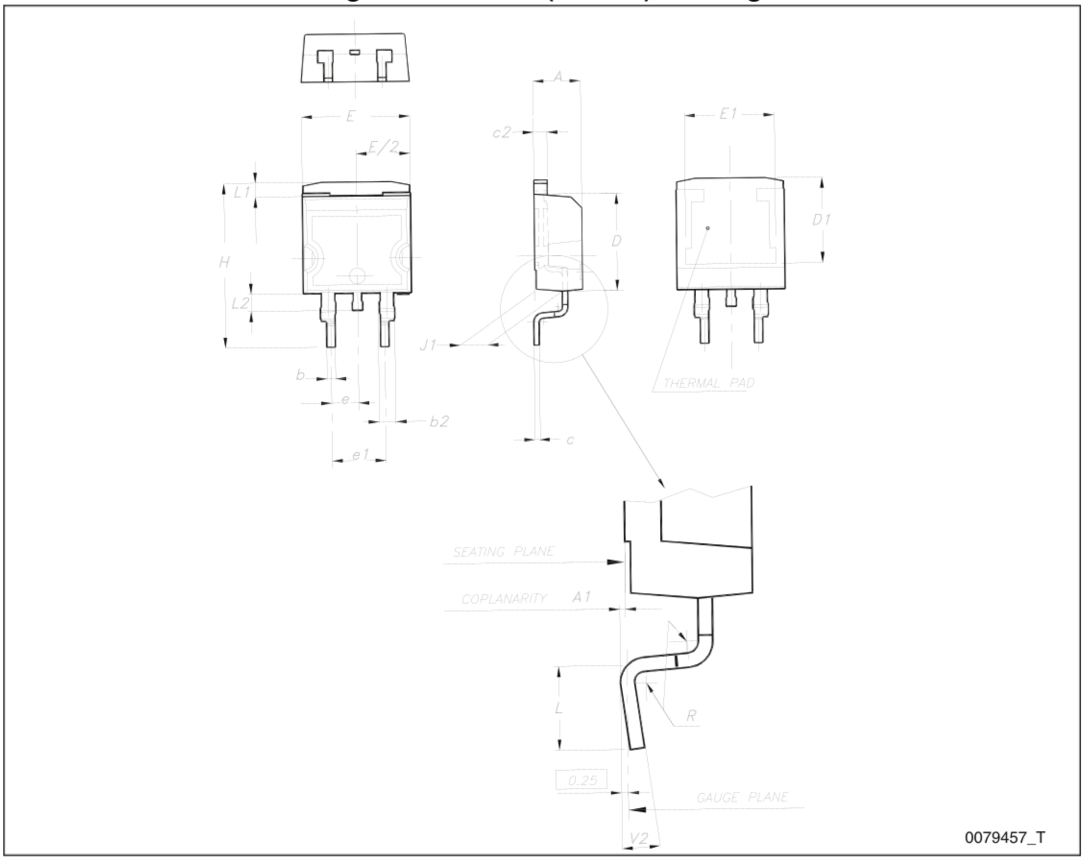
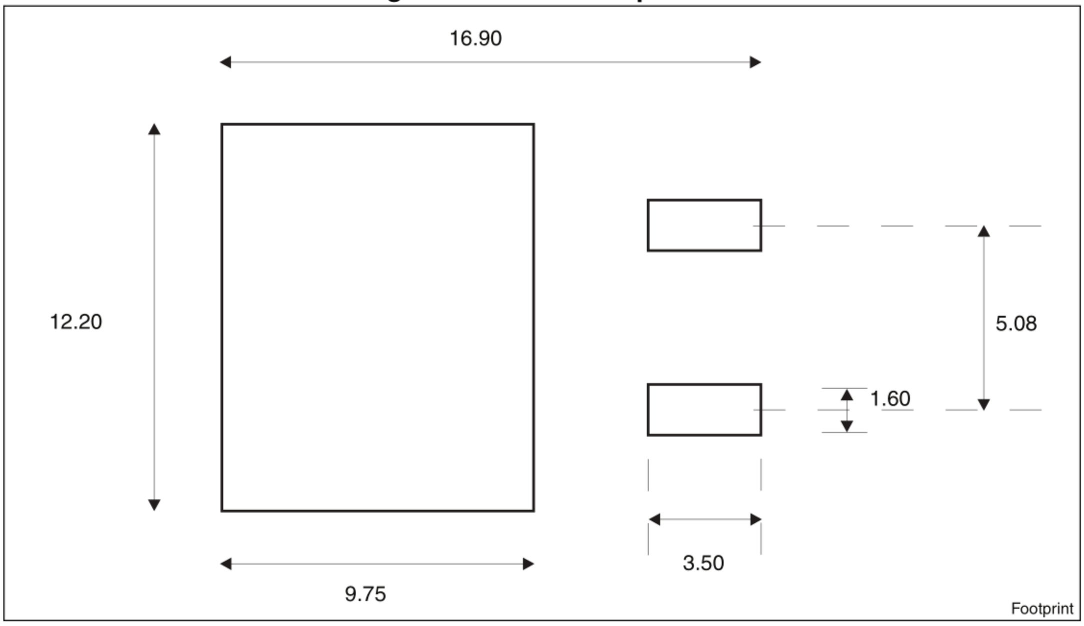


**Table 9. D²PAK (TO-263) mechanical data**

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 4.40 | | 4.60 |
| A1 | 0.03 | | 0.23 |
| b | 0.70 | | 0.93 |
| b2 | 1.14 | | 1.70 |
| c | 0.45 | | 0.60 |
| c2 | 1.23 | | 1.36 |
| D | 8.95 | | 9.35 |
| D1 | 7.50 | | |
| E | 10 | | 10.40 |
| E1 | 8.50 | | |
| e | | 2.54 | |
| e1 | 4.88 | | 5.28 |
| H | 15 | | 15.85 |
| J1 | 2.49 | | 2.69 |
| L | 2.29 | | 2.79 |
| L1 | 1.27 | | 1.40 |
| L2 | 1.30 | | 1.75 |
| R | | 0.4 | |
| V2 | 0° | | 8° |

Figure 24. D²PAK footprint[a]




a. All dimension are in millimeters

## 4.2 TO-220, STP38N65M5

**Figure 25. TO-220 type A drawing**

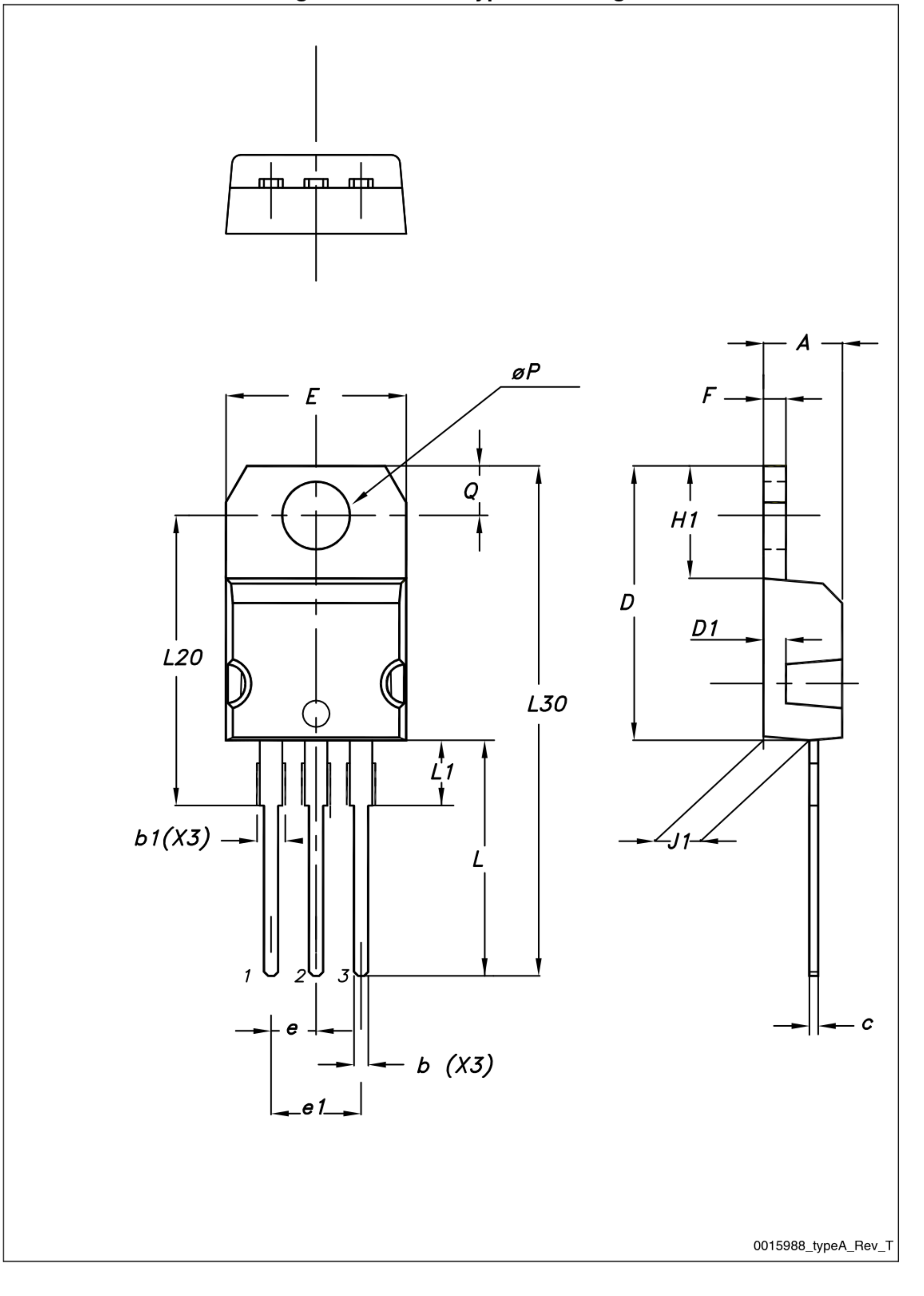


Table 10. TO-220 type A mechanical data

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 4.40 | | 4.60 |
| b | 0.61 | | 0.88 |
| b1 | 1.14 | | 1.70 |
| c | 0.48 | | 0.70 |
| D | 15.25 | | 15.75 |
| D1 | | 1.27 | |
| E | 10 | | 10.40 |
| e | 2.40 | | 2.70 |
| e1 | 4.95 | | 5.15 |
| F | 1.23 | | 1.32 |
| H1 | 6.20 | | 6.60 |
| J1 | 2.40 | | 2.72 |
| L | 13 | | 14 |
| L1 | 3.50 | | 3.93 |
| L20 | | 16.40 | |
| L30 | | 28.90 | |
| ∅P | 3.75 | | 3.85 |
| Q | 2.65 | | 2.95 |

## 4.3 TO-247, STW38N65M5

Figure 26. TO-247 drawing

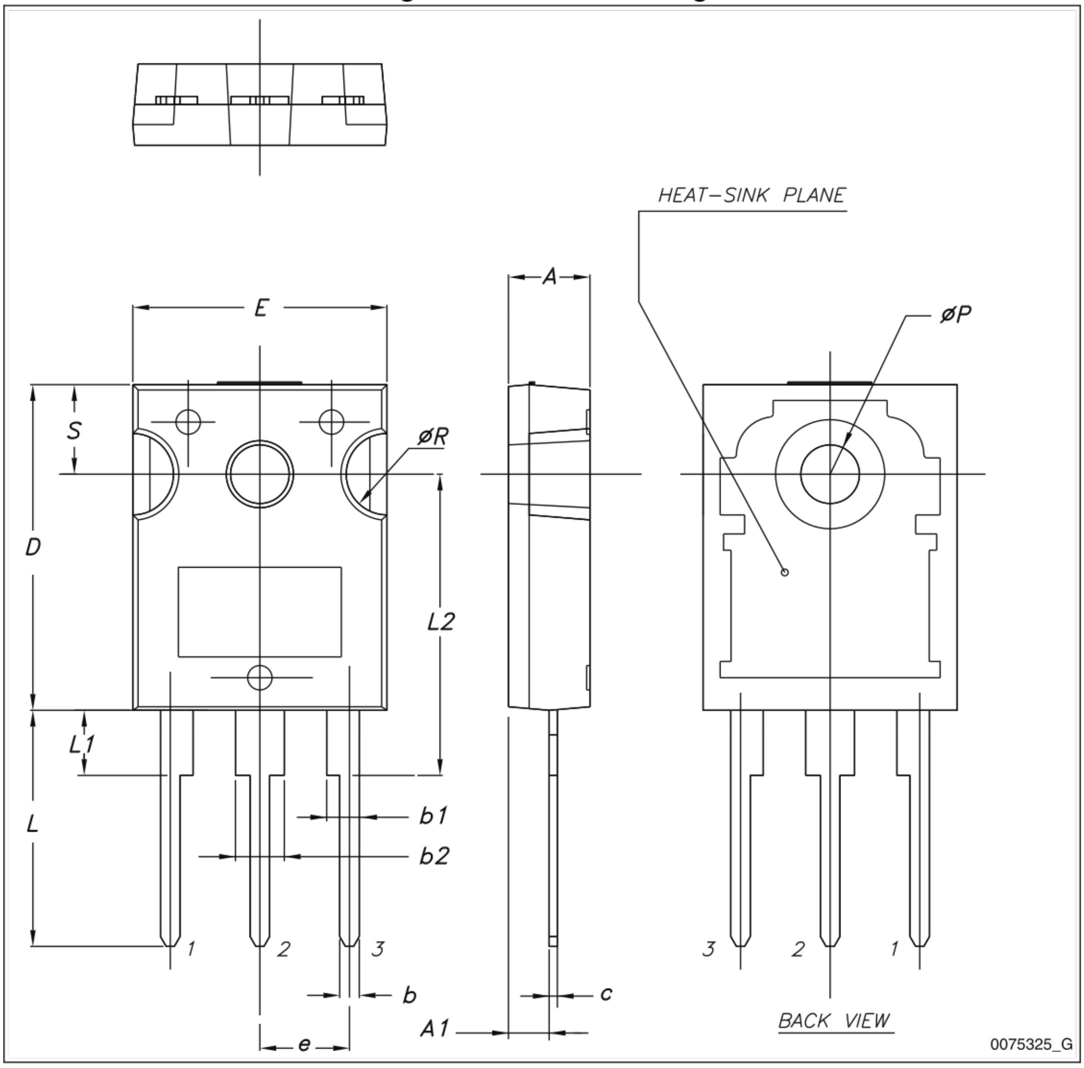


**Table 11. TO-247 mechanical data**

| Dim. | mm. | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 4.85 | | 5.15 |
| A1 | 2.20 | | 2.60 |
| b | 1.0 | | 1.40 |
| b1 | 2.0 | | 2.40 |
| b2 | 3.0 | | 3.40 |
| c | 0.40 | | 0.80 |
| D | 19.85 | | 20.15 |
| E | 15.45 | | 15.75 |
| e | 5.30 | 5.45 | 5.60 |
| L | 14.20 | | 14.80 |
| L1 | 3.70 | | 4.30 |
| L2 | | 18.50 | |
| ∅P | 3.55 | | 3.65 |
| ∅R | 4.50 | | 5.50 |
| S | 5.30 | 5.50 | 5.70 |

# 5 Packaging mechanical data

**Figure 27. Tape**

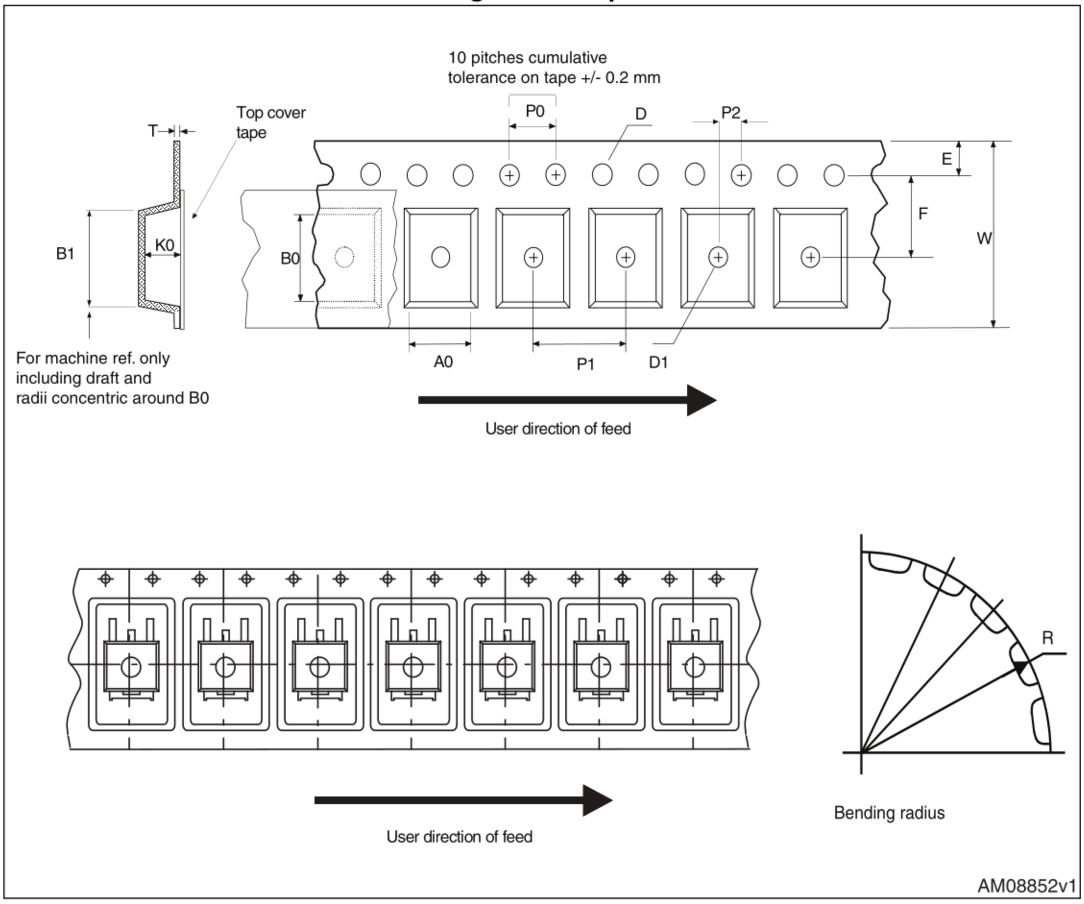


**Figure 28. Reel**

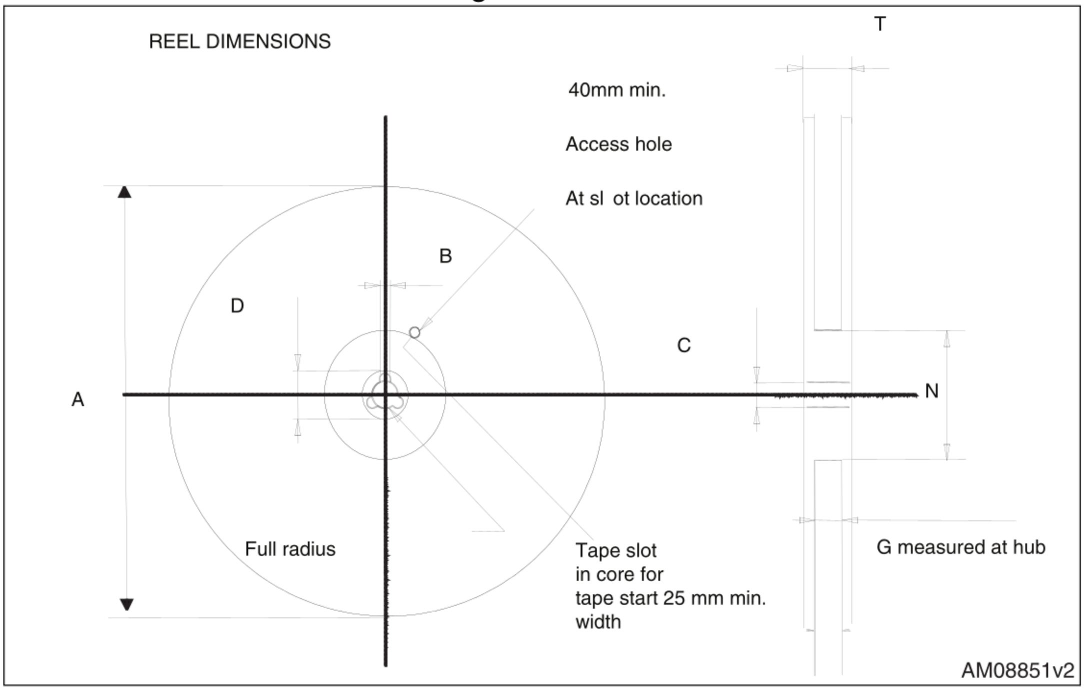



**Table 12. D²PAK (TO-263) tape and reel mechanical data**

| Tape | | | Reel | | |
|---|---|---|---|---|---|
| Dim. | mm | | Dim. | mm | |
| | Min. | Max. | | Min. | Max. |
| A0 | 10.5 | 10.7 | A | | 330 |
| B0 | 15.7 | 15.9 | B | 1.5 | |
| D | 1.5 | 1.6 | C | 12.8 | 13.2 |
| D1 | 1.59 | 1.61 | D | 20.2 | |
| E | 1.65 | 1.85 | G | 24.4 | 26.4 |
| F | 11.4 | 11.6 | N | 100 | |
| K0 | 4.8 | 5.0 | T | | 30.4 |
| P0 | 3.9 | 4.1 | | | |
| P1 | 11.9 | 12.1 | Base qty | | 1000 |
| P2 | 1.9 | 2.1 | Bulk qty | | 1000 |
| R | 50 | | | | |
| T | 0.25 | 0.35 | | | |
| W | 23.7 | 24.3 | | | |

# 6 Revision history

**Table 13. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 22-Feb-2012 | 1 | First release. |
| 21-Jun-2012 | 2 | Document status changed from preliminary data to production data.<br>Added *Section 2.1: Electrical characteristics (curves)*. |
| 05-Mar-2013 | 3 | Added dv/dt value on *Table 2: Absolute maximum ratings*. |
| 09-Apr-2014 | 4 | – The part number STF38N65M5 has been moved to a separate datasheet<br>– Minor text changes |