VN5160S-E

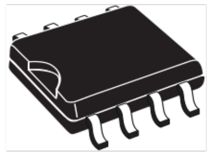
Single channel high side driver for automotive applications

Features

Max supply voltage	V_{CC}	41V
Operating voltage range	V_{CC}	4.5 to 36V
Max on-state resistance (per ch.)	R_{ON}	160 mΩ
Current limitation (typ)	I_{LIMH}	5.4 A
Off-state supply current	I_S	2 μA[1]

1. Typical value with all loads connected

- Main
  - Inrush current active management by power limitation
  - Very low stand-by current
  - 3.0V CMOS compatible input
  - Optimized electromagnetic emission
  - Very low electromagnetic susceptibility
  - In compliance with the 2002/95/EC european directive
- Diagnostic Functions
  - Open drain status output
  - On-state open load detection
  - Off-state open load detection
  - Thermal shutdown indication
- Protection
  - Undervoltage shutdown
  - Overvoltage clamp
  - Output stuck to Vcc detection
  - Load current limitation
  - Self limiting of fast thermal transients
  - Protection against loss of ground and loss of V_{CC}
  - Thermal shutdown
  - Reverse battery protection (see *Figure 28*)
  - Electrostatic discharge protection



SO-8

Applications

- All types of resistive, inductive and capacitive loads

Description

The VN5160S-E is a monolithic device made using STMicroelectronics VIPower M0-5 technology. It is intended for driving resistive or inductive loads with one side connected to ground. Active V_{CC} voltage clamp protects the device against low energy spikes.The device detects open load condition both in on and off-state, when STAT_DIS is left open or driven low. Output shorted to V_{CC} is detected in the off-state. When STAT_DIS is driven high, STATUS is in a high impedance condition. Output current limitation protects the device in overload condition. In case of long duration overload, the device limits the dissipated power to safe level up to thermal shutdown intervention. Thermal shutdown with automatic restart allows the device to recover normal operation as soon as fault condition disappears.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
SO-8	VN5160S-E	VN5160STR-E

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1 Block diagram and pins description

Figure 1. Block diagram

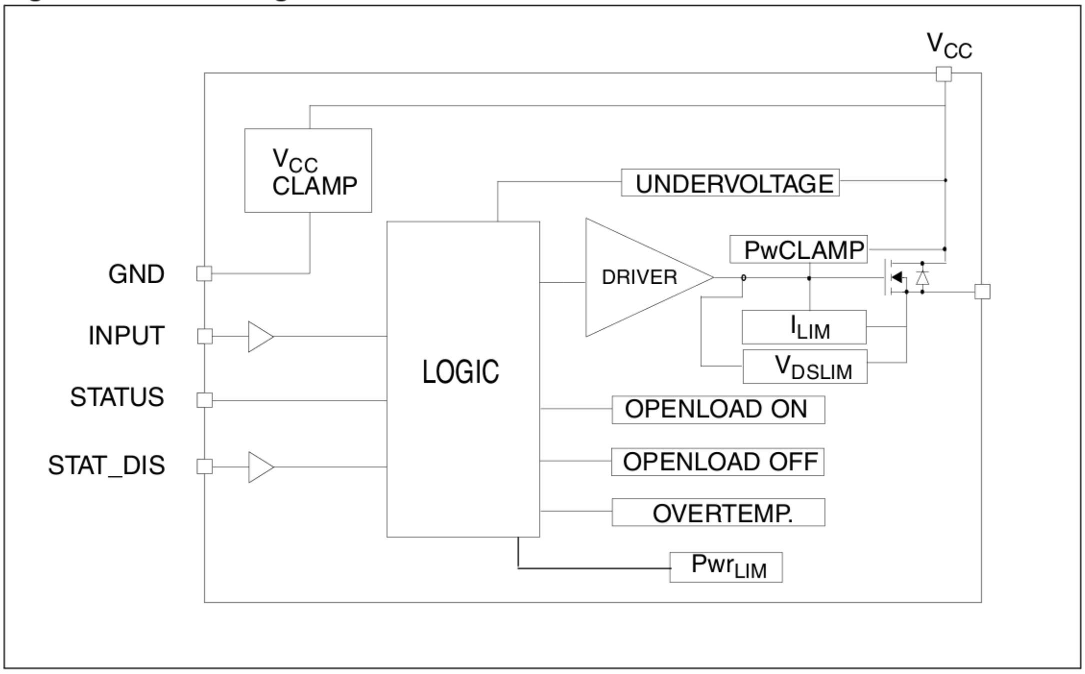


Table 2. Pins function

Name	Function
V_{CC}	Battery connection.
OUTPUT	Power output.
GND	Ground connection. Must be reverse battery protected by an external diode/resistor network.
INPUT	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state.
STATUS	Open drain digital diagnostic pin.
STAT_DIS	Active high CMOS compatible pin, to disable the STATUS pin.

Figure 2. Configuration diagram (top view)

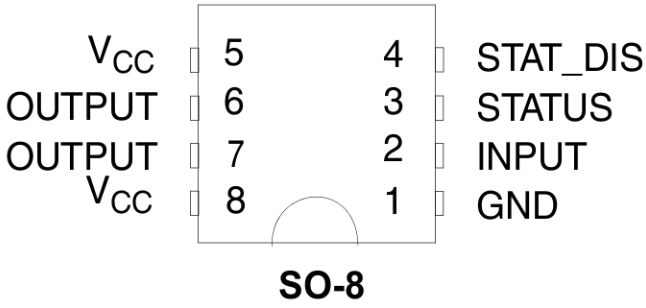


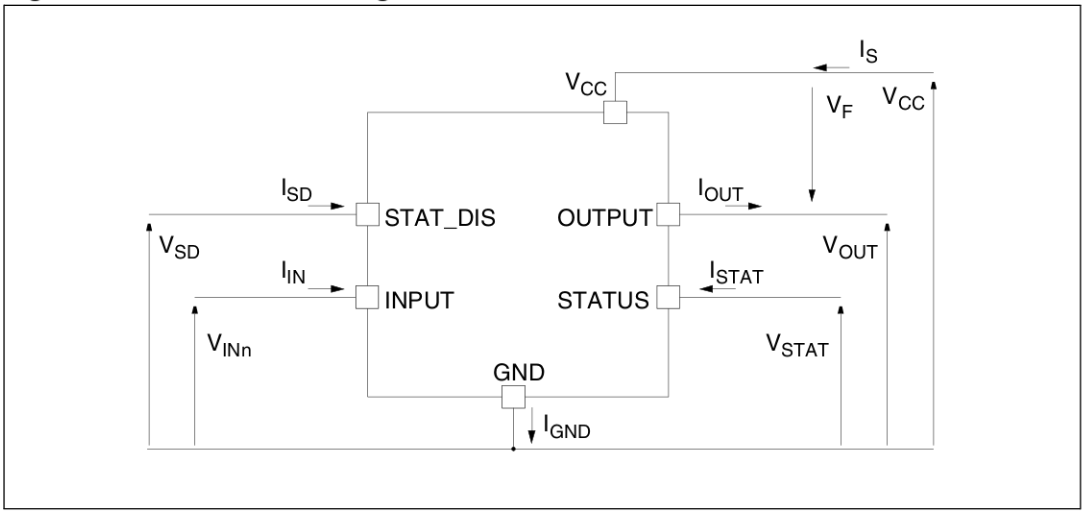
Table 3. Suggested connections for unused and N.C. pins

Connection / Pin	Status	N.C.	Output	Input	STAT_DIS
Floating	X	X	X	X	X
To ground	N.R.(1)	X	N.R.	Through 10KΩ resistor	Through 10KΩ resistor

1. Not recommended.

2 Electrical specifications

Figure 3. Current and voltage conventions



Note: $V_F = V_{OUT} - V_{CC}$ during reverse battery condition.

2.1 Absolute maximum ratings

Stressing the device above the ratings listed in the “Absolute maximum ratings” tables may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions in this section for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	0.3	V
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	6	A
I_{IN}	DC input current	+10 / -1	mA
I_{STAT}	DC status current	+10 / -1	mA
I_{STAT_DIS}	DC status disable current	+10 / -1	mA
E_{MAX}	Maximum switching energy (single pulse) ($L = 12mH$; $R_L = 0\Omega$; $V_{bat} = 13.5V$; $T_{jstart} = 150ºC$; $I_{OUT} = I_{limL}$ *(Typ.)*)	34	mJ

Table 4. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
V_{ESD}	Electrostatic discharge (Human Body Model: R=1.5KΩ; C=100pF) – INPUT – STATUS – STAT_DIS – OUTPUT – V_{CC}	 4000 4000 4000 5000 5000	 V V V V V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

2.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}pins}$	Thermal resistance junction-pins (MAX)	30	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (MAX)	See *Figure 32*	°C/W

2.3 Electrical characteristics

Values specified in this section are for 8V<V_{CC}<36V; -40°C<T_j<150°C, unless otherwise stated.

Table 6. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4.5	13	36	V
V_{USD}	Undervoltage shutdown			3.5	4.5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
R_{ON} (1)	On-state resistance	I_{OUT}=1A; T_j=25°C I_{OUT}=1A; T_j=150°C I_{OUT}=1A; V_{CC}=5V; T_j=25°C			160 320 210	mΩ mΩ mΩ
V_{clamp}	Clamp voltage	I_S= 20mA	41	46	52	V
I_S	Supply current	Off-state; V_{CC}=13V; V_{IN}=V_{OUT}=0V; T_j=25°C; On-state; V_{CC}=13V; V_{IN}=5V; I_{OUT}=0A		2 (2) 1.9	5 (1)(2) 3.5	µA mA
$I_{L(off1)}$	Off-state output current (2)	V_{IN}=V_{OUT}=0V; V_{CC}=13V; Tj=25°C V_{IN}=V_{OUT}=0V; V_{CC}=13V; T_j=125°C	0 0	0.01	3 5	µA
$I_{L(off2)}$		V_{IN}= 0V; V_{OUT}= 4V	-75		0	
V_F	Output - V_{CC} diode voltage	-I_{OUT}= 0.6A; T_j= 150°C			0.7	V

1. Guaranteed by design/characterization
2. PowerMOS leakage included

Table 7. Switching (V_{CC} = 13V; T_j = 25°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L= 13Ω (see *Figure 6*)		10		µs
$t_{d(off)}$	Turn-off delay time	R_L= 13Ω (see *Figure 6*)		15		µs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	R_L= 13Ω	See *Figure 21*			V/µs
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	R_L= 13Ω	See *Figure 22*			V/µs
W_{ON}	Switching energy losses during t_{won}	R_L= 13Ω (see *Figure 6*)		0.04		mJ
W_{OFF}	Switching energy losses during t_{woff}	R_L= 13Ω (see *Figure 6*)		0.04		mJ

Table 8. Status pin (V_{SD}=0)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{STAT}	Status low output voltage	I_{STAT}= 1.6 mA, V_{SD}= 0V			0.5	V
I_{LSTAT}	Status leakage current	Normal operation or V_{SD}= 5V, V_{STAT}= 5V			10	µA
C_{STAT}	Status pin input capacitance	Normal operation or V_{SD}=5V, V_{STAT}= 5V			100	pF
V_{SCL}	Status clamp voltage	I_{STAT}= 1mA I_{STAT}= - 1mA	5.5	 -0.7	7	V V

Table 9. Protection (1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	DC short circuit current	V_{CC}= 13V 5V<V_{CC}<36V	3.8	5.4	7.5 7.5	A A
I_{limL}	Short circuit current during thermal cycling	V_{CC}= 13V; T_R<T_j<T_{TSD}		2		A
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		T_{RS} + 1	T_{RS} + 5		°C
T_{RS}	Thermal reset of STATUS		135			°C
T_{HYST}	Thermal hysteresis (T_{TSD}-T_R)			7		°C
t_{SDL}	Status delay in overload conditions	T_j>T_{TSD}			20	µs
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT}=150mA; V_{IN}=0	V_{CC}-41	V_{CC}-46	V_{CC}-52	V
V_{ON}	Output voltage drop limitation	I_{OUT}= 0.03A; T_j=-40°C...+150°C (see *Figure 5*)		25		mV

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 10. Openload detection

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{OL}	Openload on-state detection threshold	V_{IN} = 5V, 8V<V_{CC}<18V	10	See Figure 19	40	mA
$t_{DOL(on)}$	Openload on-state detection delay	I_{OUT} = 0A, V_{CC}=13V (see Figure 4)			200	µs
t_{POL}	Delay between INPUT falling edge and STATUS rising edge in openload condition	I_{OUT} = 0A (see Figure 4)	200	500	1000	µs
V_{OL}	Openload off-state voltage detection threshold	V_{IN} = 0V, 8V<V_{CC}<16V	2	See Figure 20	4	V
t_{DSTKON}	Output short circuit to V_{cc} detection delay at turn-off	(see Figure 4)	180		t_{POL}	µs

Table 11. Logic input

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	V_{IN}= 0.9V	1			µA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	V_{IN}= 2.1V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
V_{ICL}	Input clamp voltage	I_{IN}= 1mA I_{IN}= -1mA	5.5	 -0.7	7	V V
V_{SDL}	STAT_DIS low level voltage				0.9	V
I_{SDL}	Low level STAT_DIS current	V_{CSD}= 0.9V	1			µA
V_{SDH}	STAT_DIS high level voltage		2.1			V
I_{SDH}	High level STAT_DIS current	V_{CSD}= 2.1V			10	µA
$V_{SD(hyst)}$	STAT_DIS hysteresis voltage		0.25			V
V_{SDCL}	STAT_DIS clamp voltage	I_{SD}= 1mA I_{SD}= -1mA	5.5	 -0.7	7	V V

Figure 4. Status timings

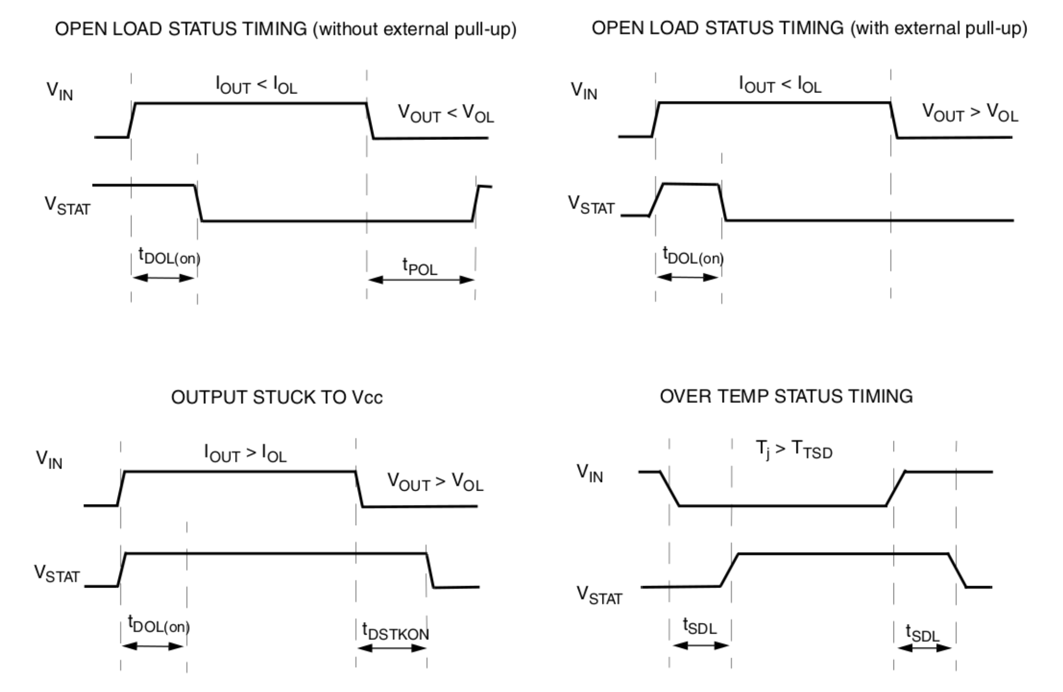


Figure 5. Output voltage drop limitation

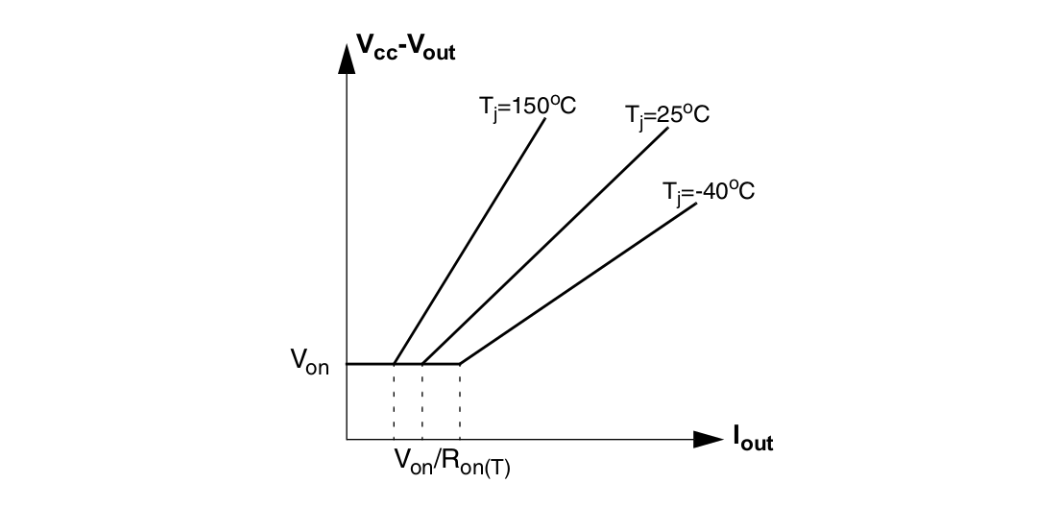


Table 12. Truth table

Conditions	INPUT	OUTPUT	STATUS (V_{SD}=0V)(1)
Normal operation	L H	L H	H H
Current limitation	L H	L X	H H
Overtemperature	L H	L L	H L
Undervoltage	L H	L L	X X
Output voltage > V_{OL}	L H	H H	L(2) H
Output current < I_{OL}	L H	L H	H(3) L

1. If the V_{SD} is high, the STATUS pin is in a high impedance.
2. The STATUS pin is low with a delay equal to t_{DSTKON} after INPUT falling edge.
3. The STATUS pin becomes high with a delay equal to t_{POL} after INPUT falling edge.

Figure 6. Switching characteristics

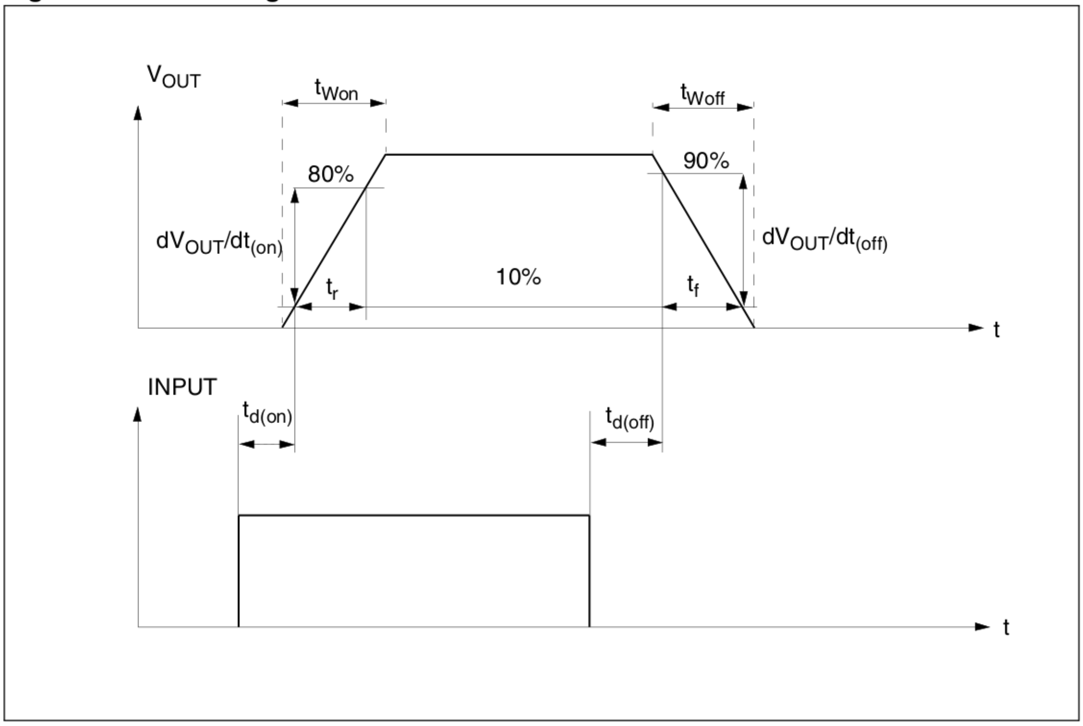


Table 13. Electrical transient requirements (part 1/3)

ISO 7637-2: 2004(E) Test pulse	Test levels		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and impedance
	III	IV				
1	-75V	-100V	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37V	+50V	5000 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	-100V	-150V	1h	90 ms	100 ms	0.1 µs, 50 Ω
3b	+75V	+100V	1h	90 ms	100 ms	0.1 µs, 50 Ω
4	-6V	-7V	1 pulse			100 ms, 0.01Ω
5b(1)	+65V	+87V	1 pulse			400 ms, 2 Ω

1. Valid in case of external load dump clamp: 40V maximum referred to ground.

Table 14. Electrical transient requirements (part 2/3)

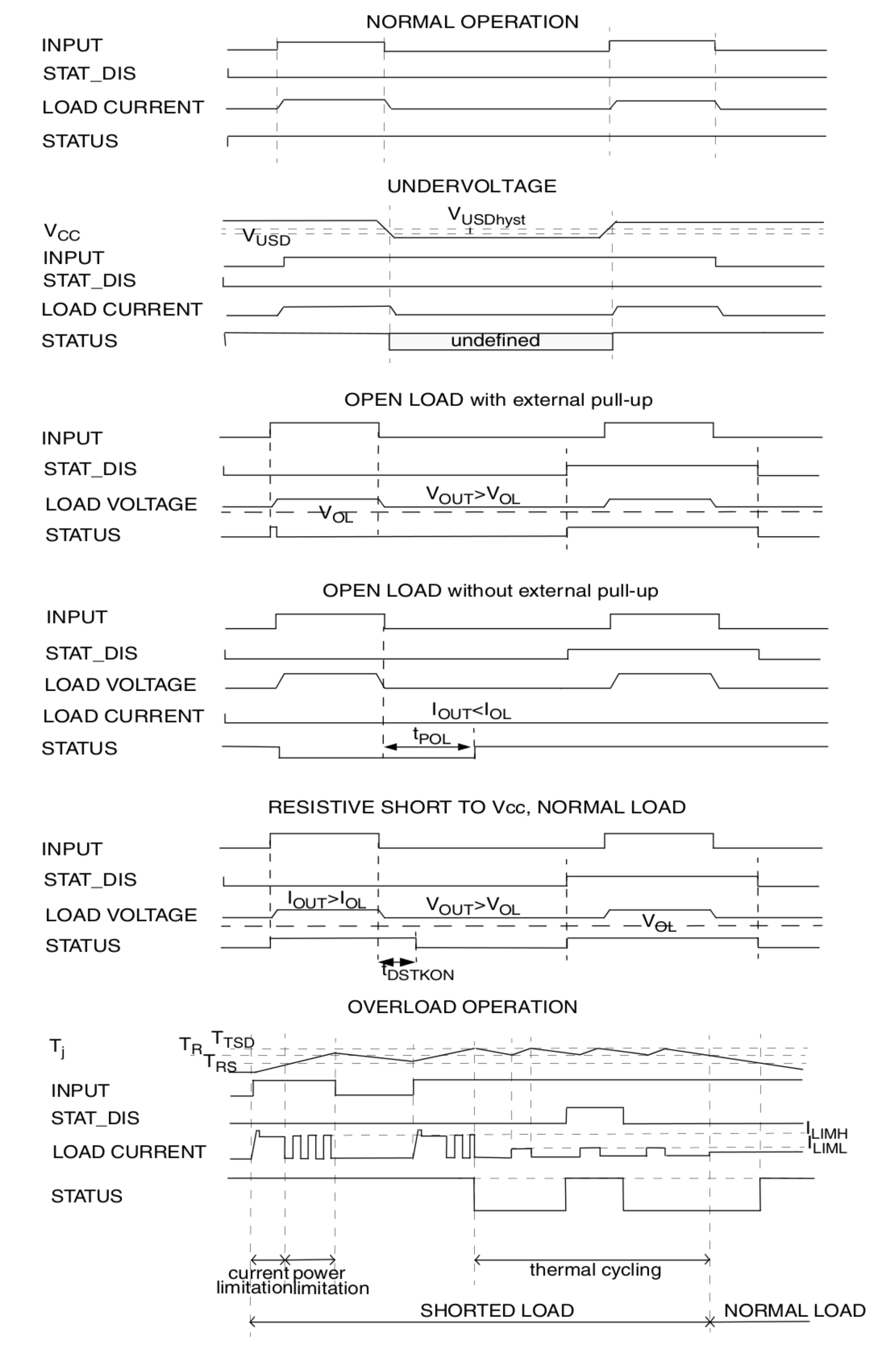
ISO 7637-2: 2004(E) Test pulse	Test level results(1)	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b(2)	C	C

1. The above test levels must be considered referred to V_{CC} = 13.5V except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to ground.

Table 15. Electrical transient requirements (part 3/3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 7. Waveforms



2.4 Electrical characteristics curves

Figure 8. Off-state output current

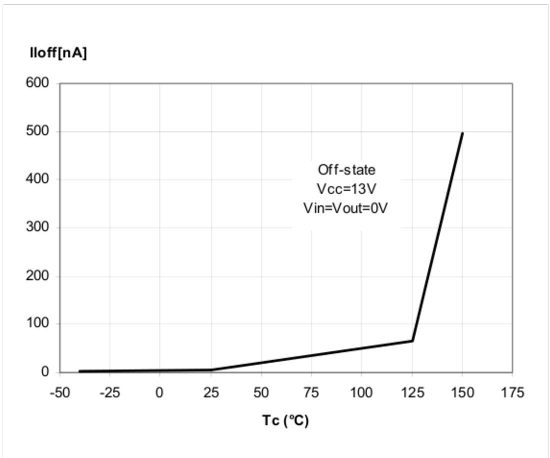


Figure 9. Input clamp voltage

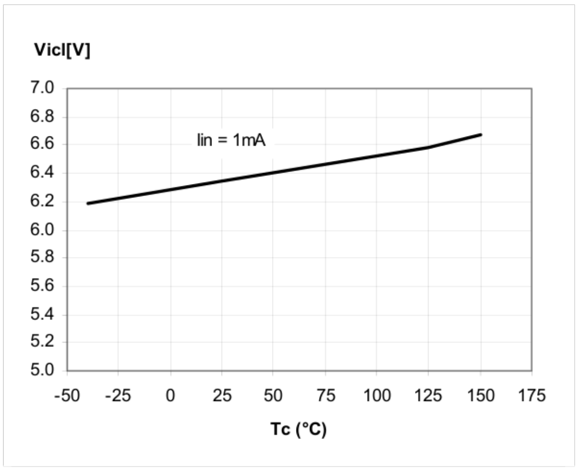


Figure 10. High-level input current

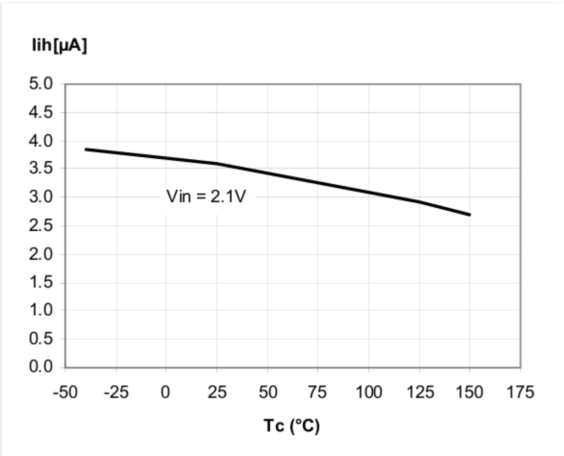


Figure 11. Input high-level voltage

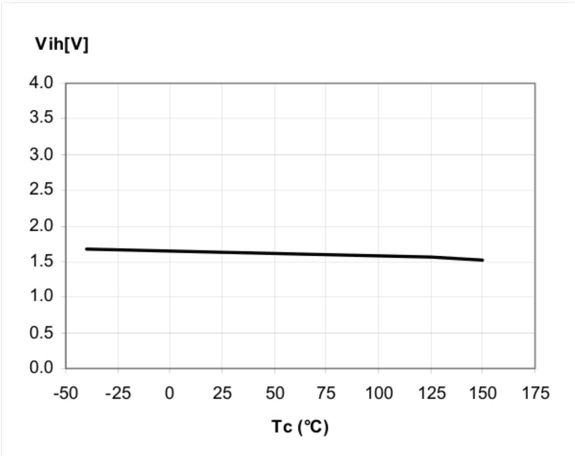


Figure 12. Input low-level voltage

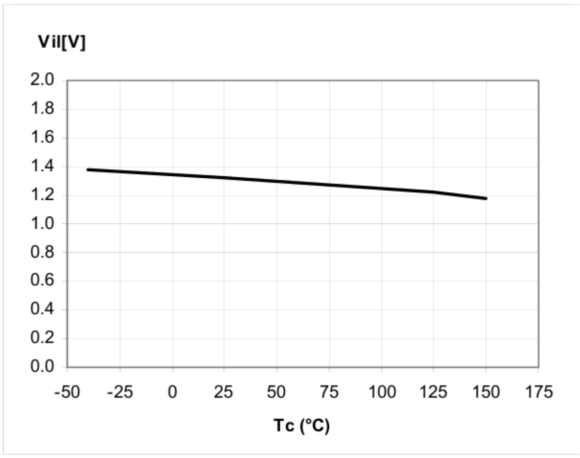


Figure 13. Input hysteresis voltage

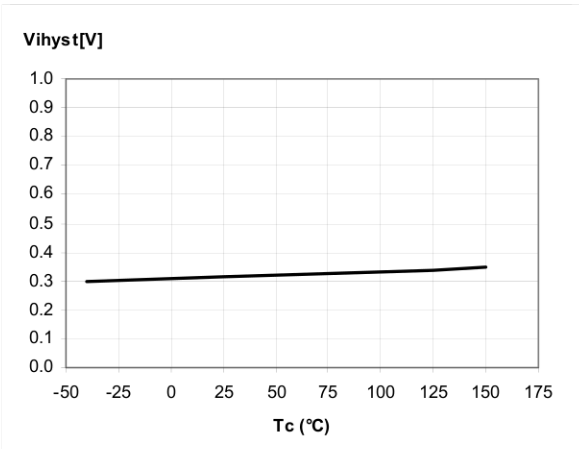


Figure 14. Status low-output voltage

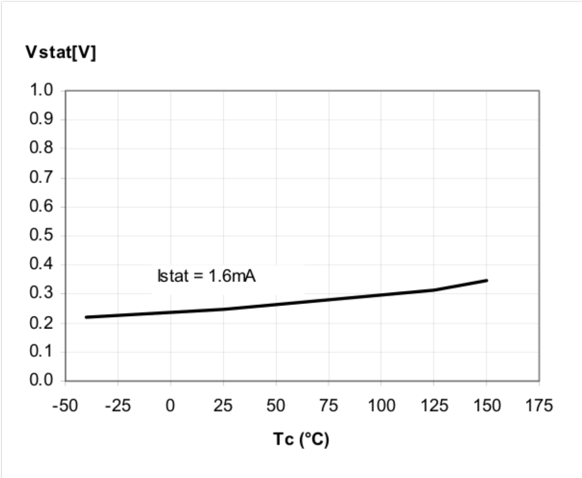


Figure 15. Status leakage current

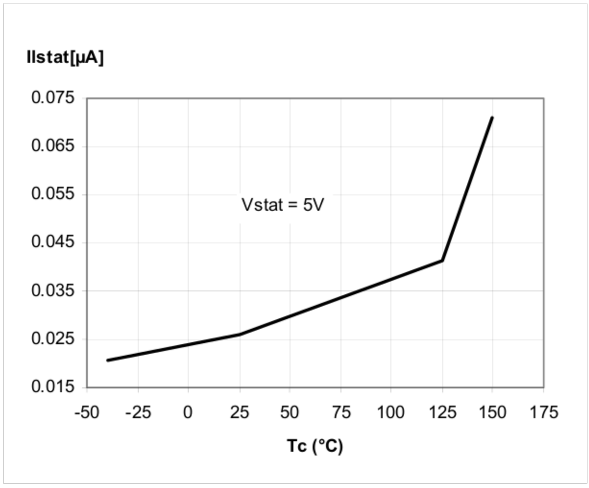


Figure 16. Status clamp voltage

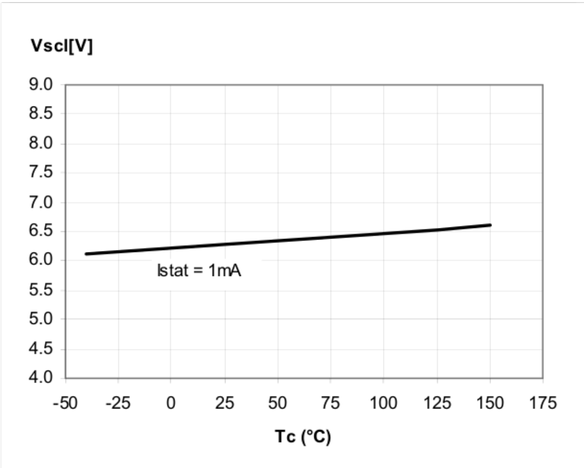


Figure 17. On-state resistance vs T_{case}

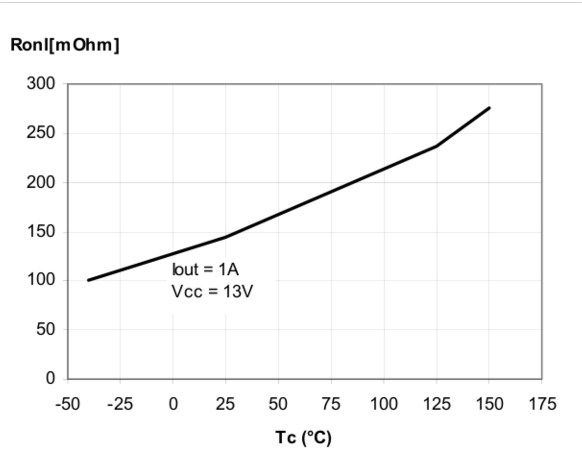


Figure 18. On-state resistance vs V_{CC}

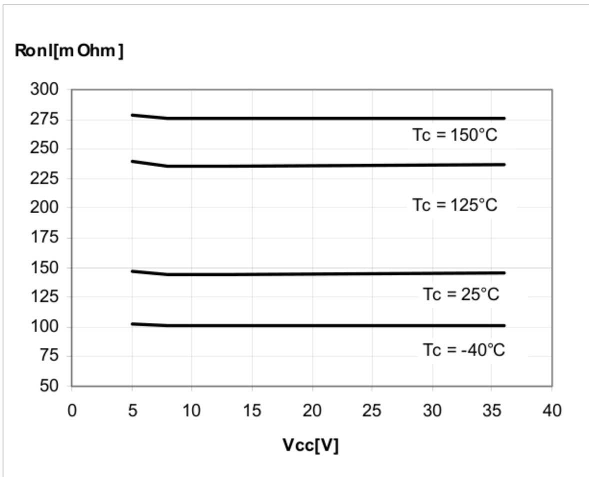


Figure 19. Open-load on-state detection threshold

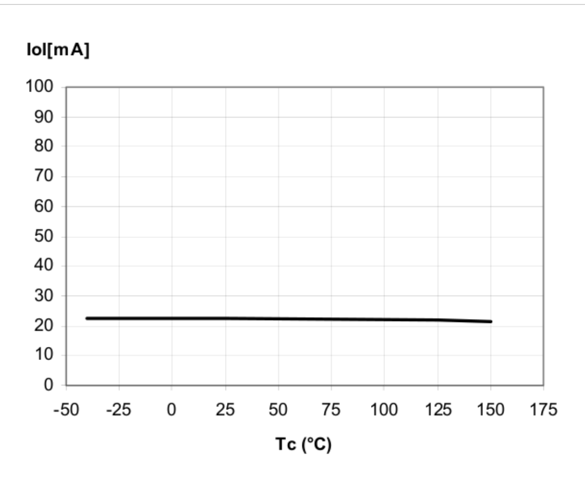


Figure 20. Open-load off-state voltage detection threshold

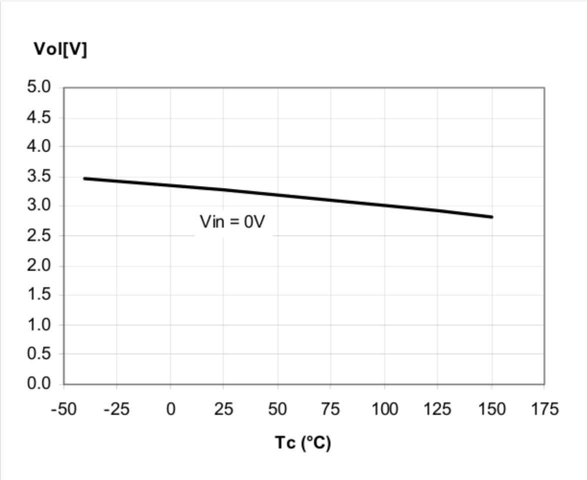


Figure 21. Turn-on voltage slope

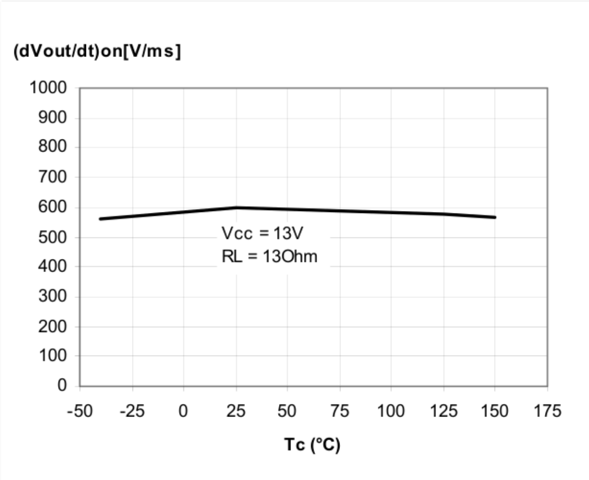


Figure 22. Turn-off voltage slope

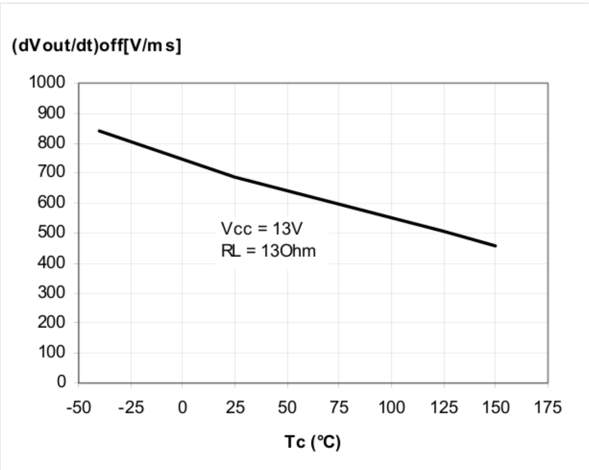


Figure 23. I_{LIM} vs T_{case}

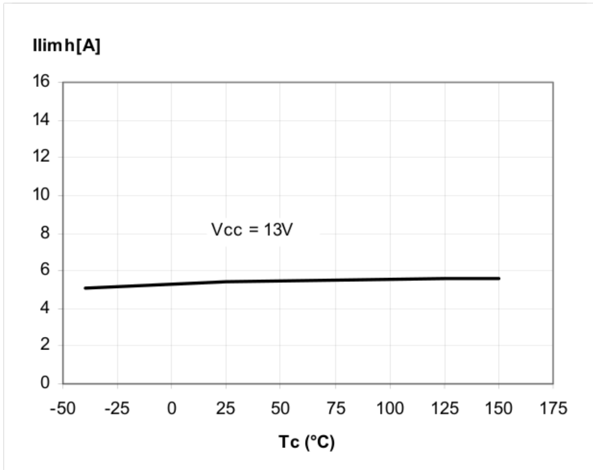


Figure 24. Undervoltage shutdown

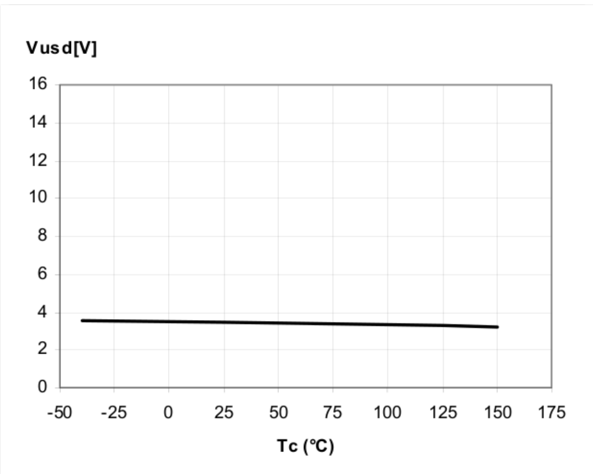


Figure 25. STAT_DIS clamp voltage

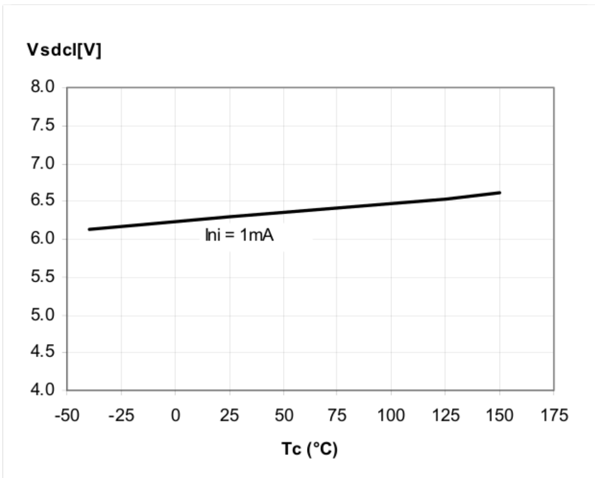


Figure 26. High-level STAT_DIS voltage

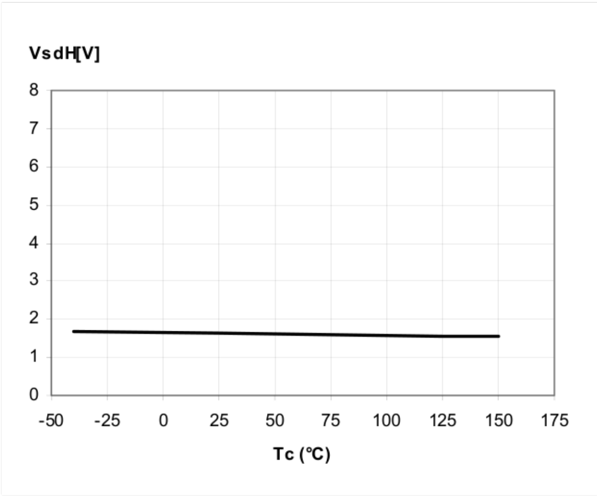
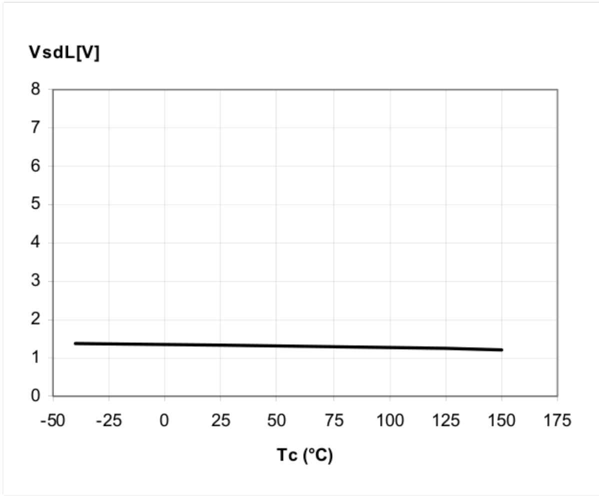
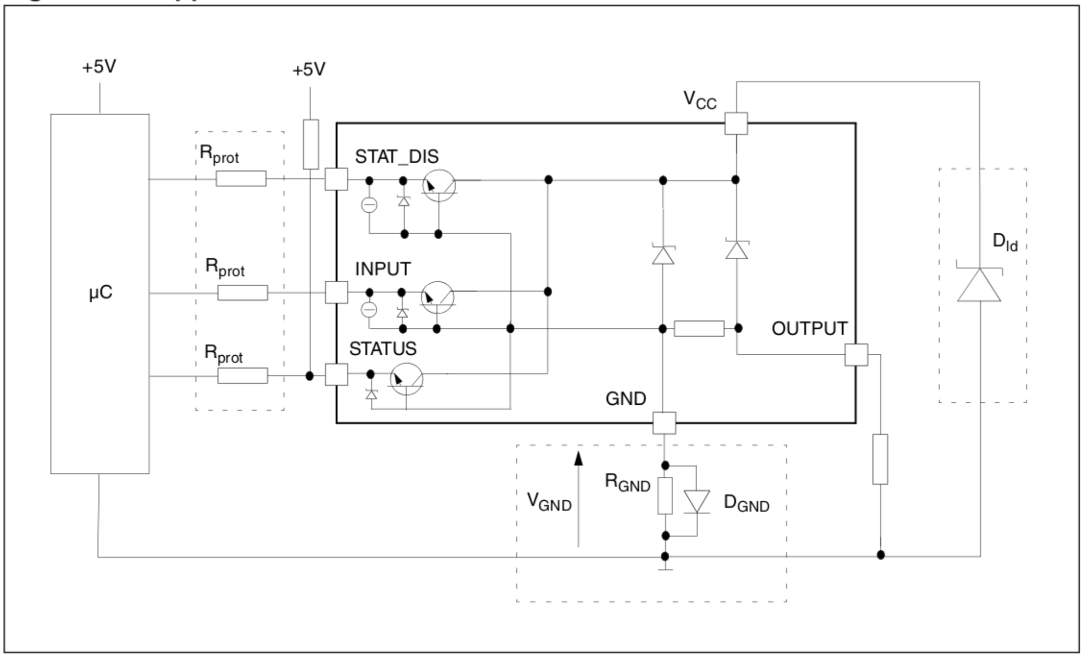


Figure 27. Low-level STAT_DIS voltage



3 Application Information

Figure 28. Application schematic



3.1 GND protection network against reverse battery

3.1.1 Solution 1: resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

1. $R_{GND} \leq 600mV / (I_{S(on)max})$
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power dissipation in R_{GND} (when V_{CC}<0: during reverse battery situations) is:

$P_D = (-V_{CC})^2 / R_{GND}$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum On-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_{GND} will produce a shift ($I_{S(on)max}$ * R_{GND}) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see below).

3.1.2 Solution 2: a diode (D_{GND}) in the ground line

A resistor (R_{GND}=1kΩ) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network will produce a shift (≈600mV) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

3.2 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

3.3 MCU I/Os protection

If a ground protection network is used and negative transient are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the µC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of µC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of µC I/Os.

$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$

Calculation example:

For V_{CCpeak}= - 100V and $I_{latchup} \geq$ 20mA; $V_{OH\mu C} \geq$ 4.5V

5k$\Omega \leq R_{prot} \leq$ 180kΩ.

Recommended R_{prot} values is 10kΩ.

3.4 Open load detection in off-state

Off-state open load detection requires an external pull-up resistor (R_{PU}) connected between OUTPUT pin and a positive supply voltage (V_{PU}) like the +5V line used to supply the microprocessor.

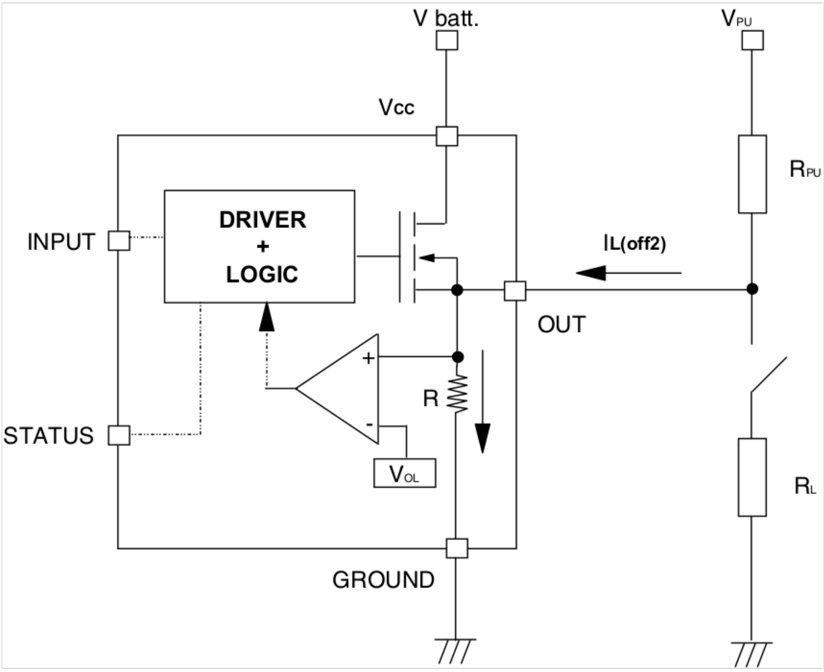
The external resistor has to be selected according to the following requirements:

1. no false open load indication when load is connected: in this case we have to avoid V_{OUT} to be higher than V_{Olmin}; this results in the following condition $V_{OUT}= (V_{PU}/(R_L+R_{PU}))R_L<V_{Olmin}$.
2. no misdetection when load is disconnected: in this case the V_{out} has to be higher than V_{OLmax}; this results in the following condition $R_{PU}<(V_{PU}–V_{OLmax})/I_{L(off2)}$.

Because $I_{s(OFF)}$ may significantly increase if V_{out} is pulled high (up to several mA), the pull-up resistor R_{PU} should be connected to a supply that is switched OFF when the module is in standby.

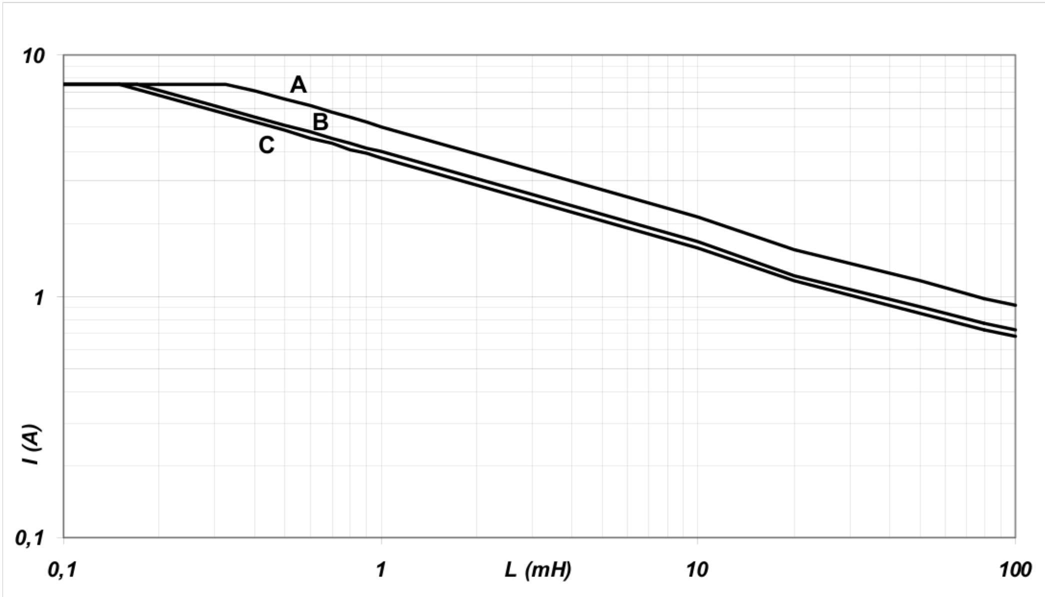
The values of V_{OLmin}, V_{OLmax} and $I_{L(off2)}$ are available in the Electrical characteristics section.

Figure 29. Open-load detection in off-state



3.5 Maximum demagnetization energy (V_{CC} = 13.5V)

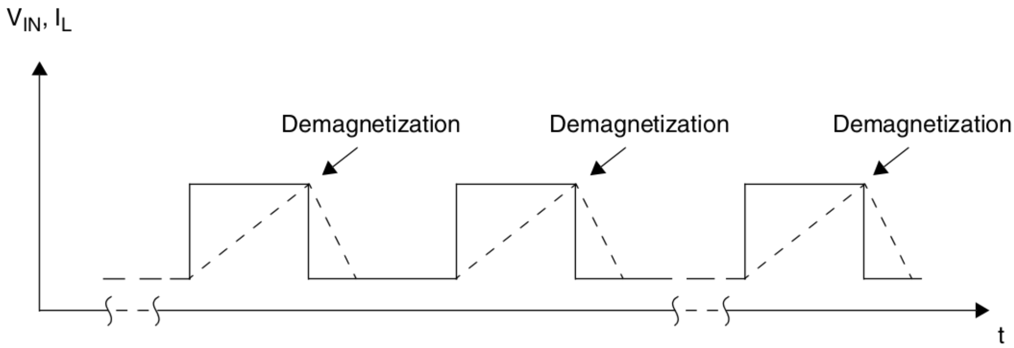
Figure 30. Maximum turn-off current versus inductance



A: T_{jstart} = 150°C single pulse

B: T_{jstart} = 100°C repetitive pulse

C: T_{jstart} = 125°C repetitive pulse

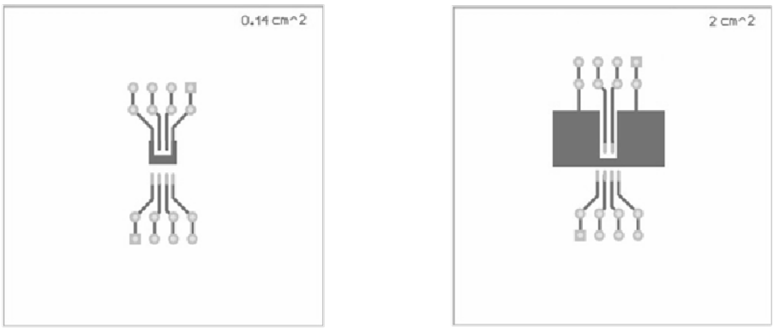


Note: Values are generated with R_L =0 Ω. In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PCB thermal data

4.1 SO-8 thermal data

Figure 31. SO-8 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB: FR4 area= 4.8 mm x 4.8 mm, PCB thickness=2 mm, Cu thickness= 35 µm, Copper areas: from minimum pad lay-out to 2 cm^2).

Figure 32. $R_{thj-amb}$ vs PCB copper area in open box free air condition

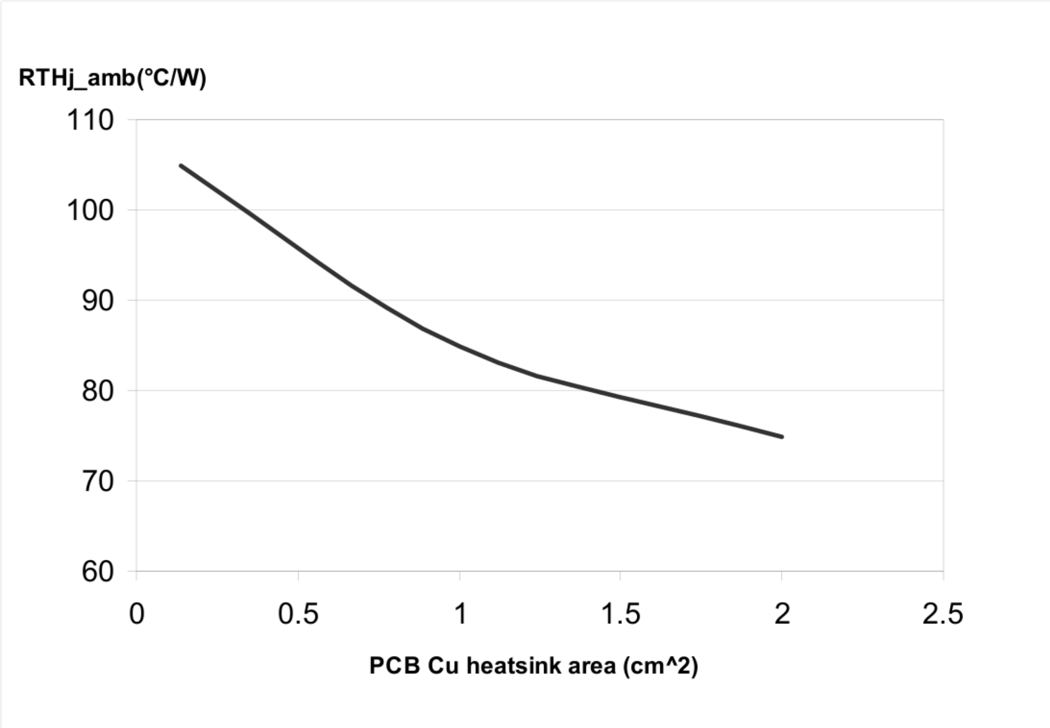
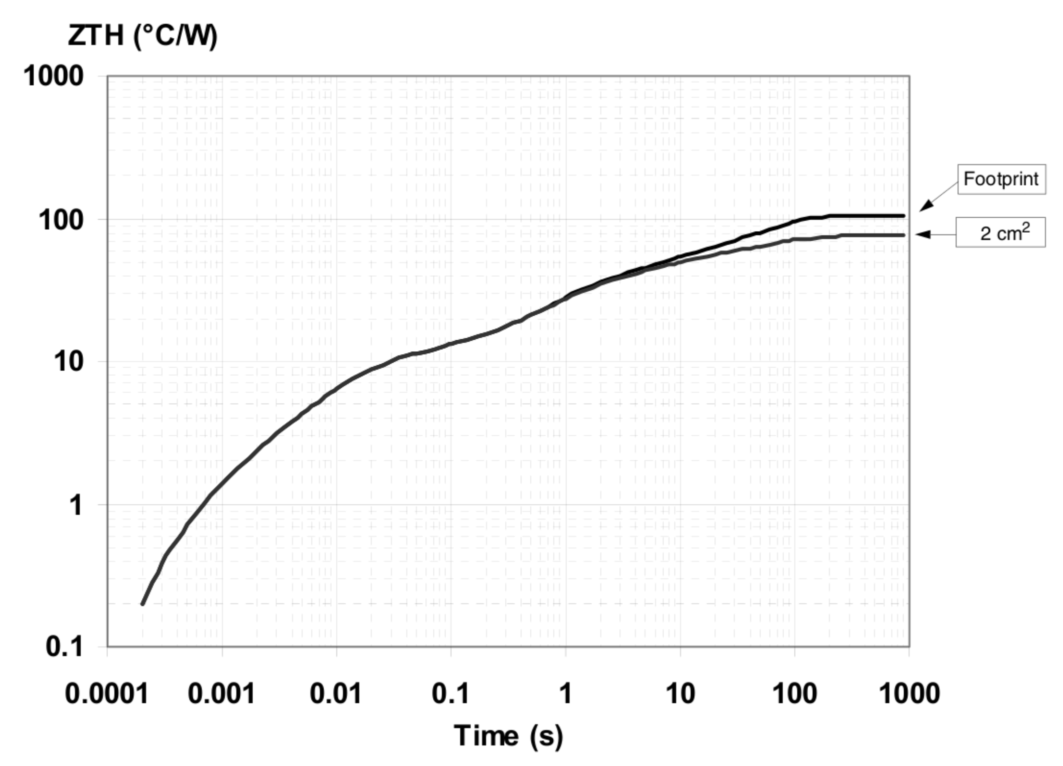


Figure 33. SO-8 Thermal impedance junction ambient single pulse

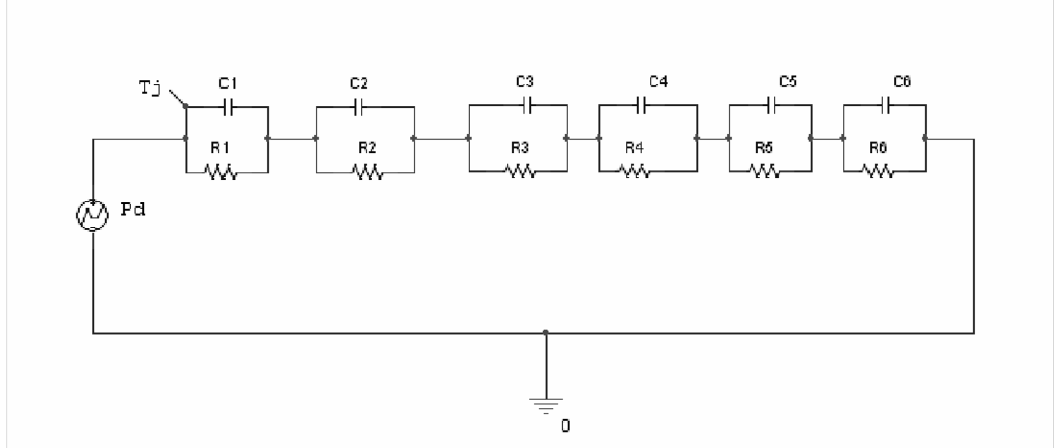


Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Figure 34. Thermal fitting model of a single-channel HSD in SO-8(1)



1. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 16. Thermal parameter

Area/island (cm^2)	Footprint	2
R1 (°C/W)	1.2	
R2 (°C/W)	6	
R3 (°C/W)	3.5	
R4 (°C/W)	21	
R5 (°C/W)	16	
R6 (°C/W)	58	28
C1 (W.s/°C)	0.0008	
C2 (W.s/°C)	0.0016	
C3 (W.s/°C)	0.0075	
C4 (W.s/°C)	0.045	
C5 (W.s/°C)	0.35	
C6 (W.s/°C)	1.05	2

5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

5.2 Package mechanical data

Figure 35. SO-8 package dimensions

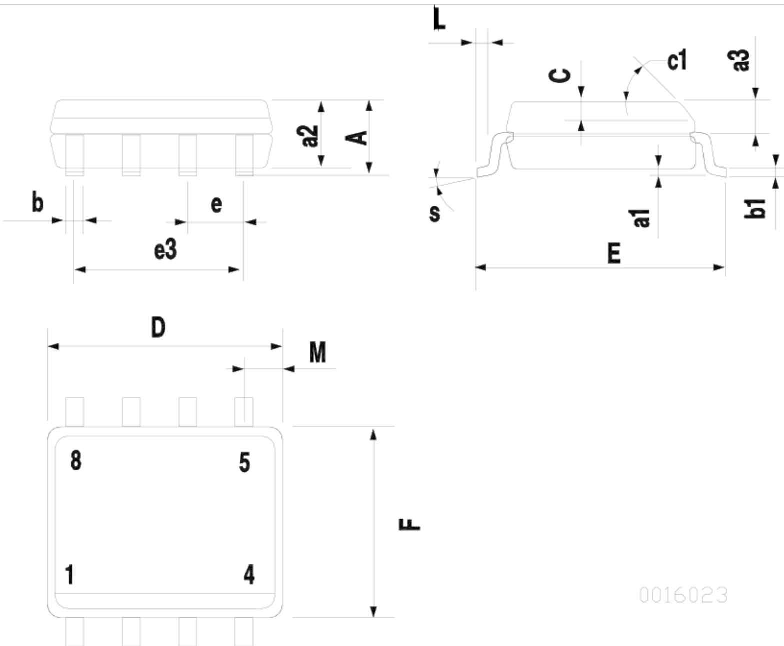
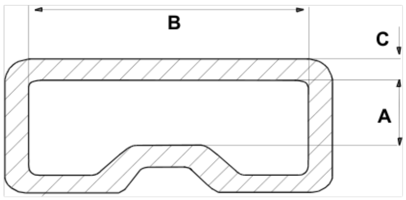


Table 17. SO-8 mechanical data

Dim.	Millimeter		
	Min.	Typ.	Max.
A			1.75
a1	0.1		0.25
a2			1.65
a3	0.65		0.85
b	0.35		0.48
b1	0.19		0.25
C	0.25		0.5
c1	45 (typ.)		
D	4.8		5
E	5.8		6.2
e		1.27	
e3		3.81	
F	3.8		4
L	0.4		1.27
M			0.6
S	8 (max.)		
L1	0.8		1.2

5.3 Packing information

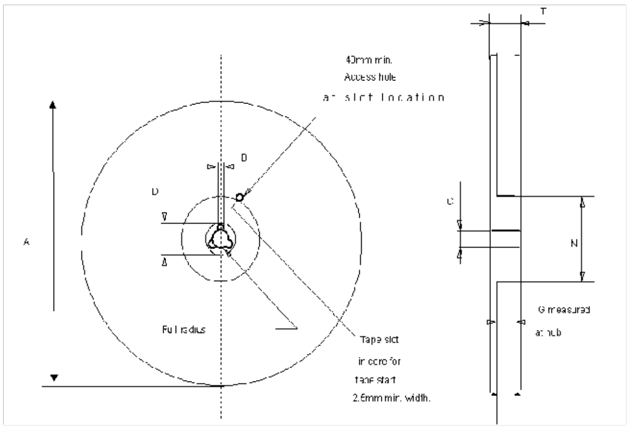
Figure 36. SO-8 tube shipment (no suffix)



Base Q.ty	100
Bulk Q.ty	2000
Tube length (± 0.5)	532
A	3.2
B	6
C (± 0.1)	0.6

All dimensions are in mm.

Figure 37. SO-8 tape and reel shipment (suffix "TR")



Reel dimensions

Base Q.ty	2500
Bulk Q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	12.4
N (min)	60
T (max)	18.4

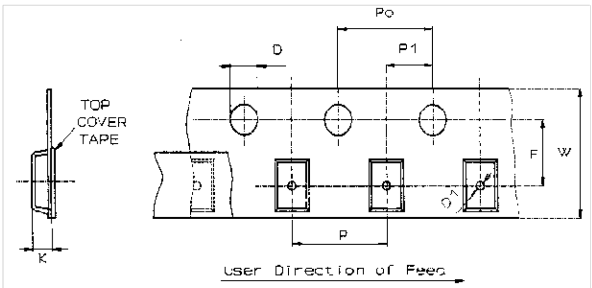
All dimensions are in mm.

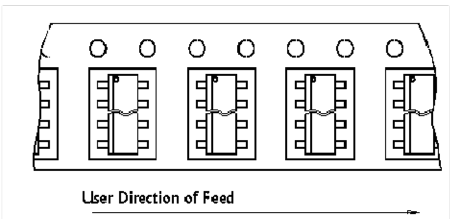
Tape dimensions

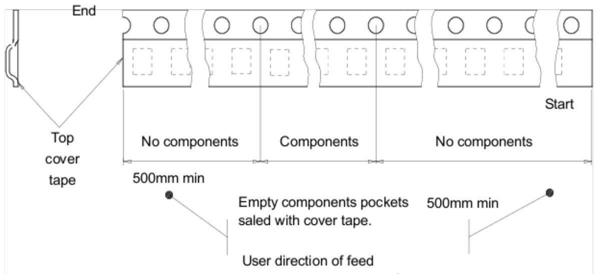
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	12
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	8
Hole Diameter	**D (+ 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	5.5
Compartment Depth	**K (max)**	4.5
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.







6 Revision history

Table 18. Document revision history

Date	Revision	Changes
Feb-2007	1	Initial release.
May-2007	2	Document rewritten, restructured and put in corporate technical literature template.
17-Dec-2007	3	*Table 4: Absolute maximum ratings*: changed E_{MAX} value from 14 to 34 mJ. *Table 13: Electrical transient requirements (part 1/3)*: updated test level values III and IV for test pulse 5b and notes. Added *Section 3.5: Maximum demagnetization energy (VCC = 13.5V)*. *Figure 34: Thermal fitting model of a single-channel HSD in SO-8*(1): added note.
23-Nov-2009	4	Updated *Section 2.3: Electrical characteristics*. Updated *Section 2.4: Electrical characteristics curves*. Updated *Table 6: Power section*.
20-Sep-2013	5	Updated Disclaimer