

CSD17575Q3 30-V N-Channel NexFET™ Power MOSFET

1 Features

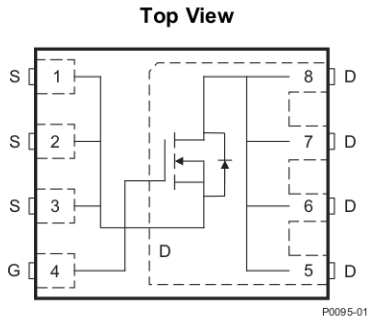
- Low Q_g and Q_{gd}
- Low $R_{DS(on)}$
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 3.3 mm × 3.3 mm Plastic Package

2 Applications

- Point of Load Synchronous Buck Converter for Applications in Networking, Telecom, and Computing Systems
- Optimized for Synchronous FET Applications

3 Description

This 1.9 mΩ, 30 V, SON 3×3 NexFET™ power MOSFET is designed to minimize losses in power conversion applications.



Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	30		V
Q_g	Gate Charge Total (4.5V)	23		nC
Q_{gd}	Gate Charge Gate-to-Drain	5.4		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = 4.5\text{ V}$	2.6	mΩ
		$V_{GS} = 10\text{ V}$	1.9	
V_{th}	Threshold Voltage	1.4		V

Ordering Information⁽¹⁾

Device	Media	Qty	Package	Ship
CSD17575Q3	13-Inch Reel	2500	SON 3.3 × 3.3 mm Plastic Package	Tape and Reel
CSD17575Q3T	13-Inch Reel	250		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current (Package Limit)	60	A
	Continuous Drain Current (Silicon Limit), $T_C = 25^\circ\text{C}$	182	
	Continuous Drain Current ⁽¹⁾	27	
I_{DM}	Pulsed Drain Current ⁽²⁾	240	A
P_D	Power Dissipation ⁽¹⁾	2.8	W
	Power Dissipation, $T_C = 25^\circ\text{C}$	108	
T_J, T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150	°C
E_{AS}	Avalanche Energy, single pulse $I_D = 48, L = 0.1\text{ mH}, R_G = 25\ \Omega$	115	mJ

(1) Typical $R_{\theta JA} = 45^\circ\text{C/W}$ on 1-inch² Cu (2 oz.) on 0.060-inch thick FR4 PCB.

(2) Max $R_{\theta JC} = 1.5^\circ\text{C/W}$, pulse duration ≤100 μs, duty cycle ≤1%

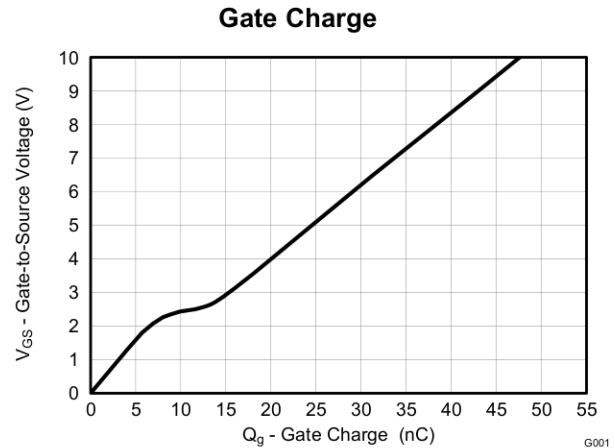
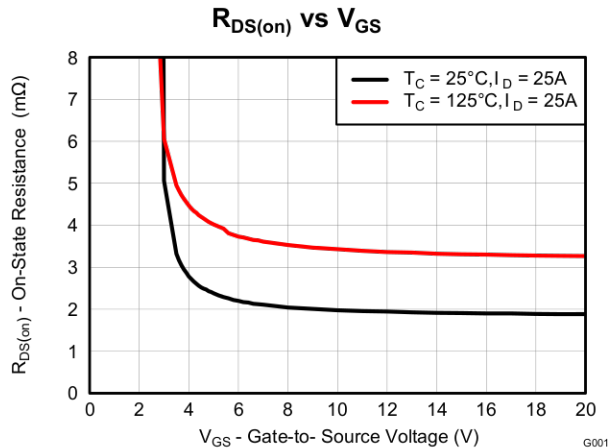


Table of Contents

1 Features 1 2 Applications 1 3 Description 1 4 Revision History 2 5 Specifications 3 5.1 Electrical Characteristics 3 5.2 Thermal Information 3 5.3 Typical MOSFET Characteristics..... 4 6 Device and Documentation Support 7	6.1 Trademarks 7 6.2 Electrostatic Discharge Caution 7 6.3 Glossary 7 7 Mechanical, Packaging, and Orderable Information 8 7.1 Q3 Package Dimensions 8 7.2 Recommended PCB Pattern 9 7.3 Recommended Stencil Opening 9 7.4 Q3 Tape and Reel Information..... 10
---	---

4 Revision History

Changes from Original (June 2014) to Revision A	Page
<ul style="list-style-type: none"> • Added b1, d, d1, and K dimensions to the mechanical information table 8 	8

5 Specifications

5.1 Electrical Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
I_{DSS}	Drain-to-Source Leakage Current	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$			1	μA
I_{GSS}	Gate-to-Source Leakage Current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.1	1.4	1.8	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = 4.5\text{ V}, I_D = 25\text{ A}$		2.6	3.2	m Ω
		$V_{GS} = 10\text{ V}, I_D = 25\text{ A}$		1.9	2.3	
g_{fs}	Transconductance	$V_{DS} = 3\text{ V}, I_D = 25\text{ A}$		118		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 15\text{ V}, f = 1\text{ MHz}$		3400	4420	pF
C_{OSS}	Output Capacitance			393	511	pF
C_{RSS}	Reverse Transfer Capacitance			157	204	pF
R_g	Series Gate Resistance	$V_{DS} = 15\text{ V}, I_D = 25\text{ A}$		0.9	1.8	Ω
Q_g	Gate Charge Total (4.5 V)			23	30	nC
Q_{gd}	Gate Charge Gate-to-Drain			5.4		nC
Q_{gs}	Gate Charge Gate-to-Source			8.5		nC
$Q_{g(th)}$	Gate Charge at V_{th}			4.6		nC
Q_{OSS}	Output Charge	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}$		11.6		nC
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 25\text{ A}$ $R_G = 2\ \Omega$		4		ns
t_r	Rise Time			10		ns
$t_{d(off)}$	Turn Off Delay Time			20		ns
t_f	Fall Time			3		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	$I_S = 25\text{ A}, V_{GS} = 0\text{ V}$		0.8	1	V
Q_{rr}	Reverse Recovery Charge	$V_{DD} = 15\text{ V}, I_F = 25\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		15		nC
t_{rr}	Reverse Recovery Time			13		ns

5.2 Thermal Information

($T_A = 25^\circ\text{C}$ unless otherwise stated)

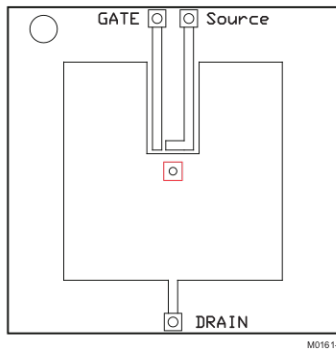
THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance ⁽¹⁾			1.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance ⁽¹⁾⁽²⁾			55	

- (1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch² (6.45-cm²), Cu pad on a 1.5-inches × 1.5-inches thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch² 2-oz.Cu.

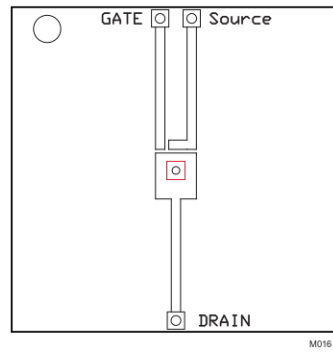
CSD17575Q3

SLPS489A – JUNE 2014 – REVISED AUGUST 2014

www.ti.com



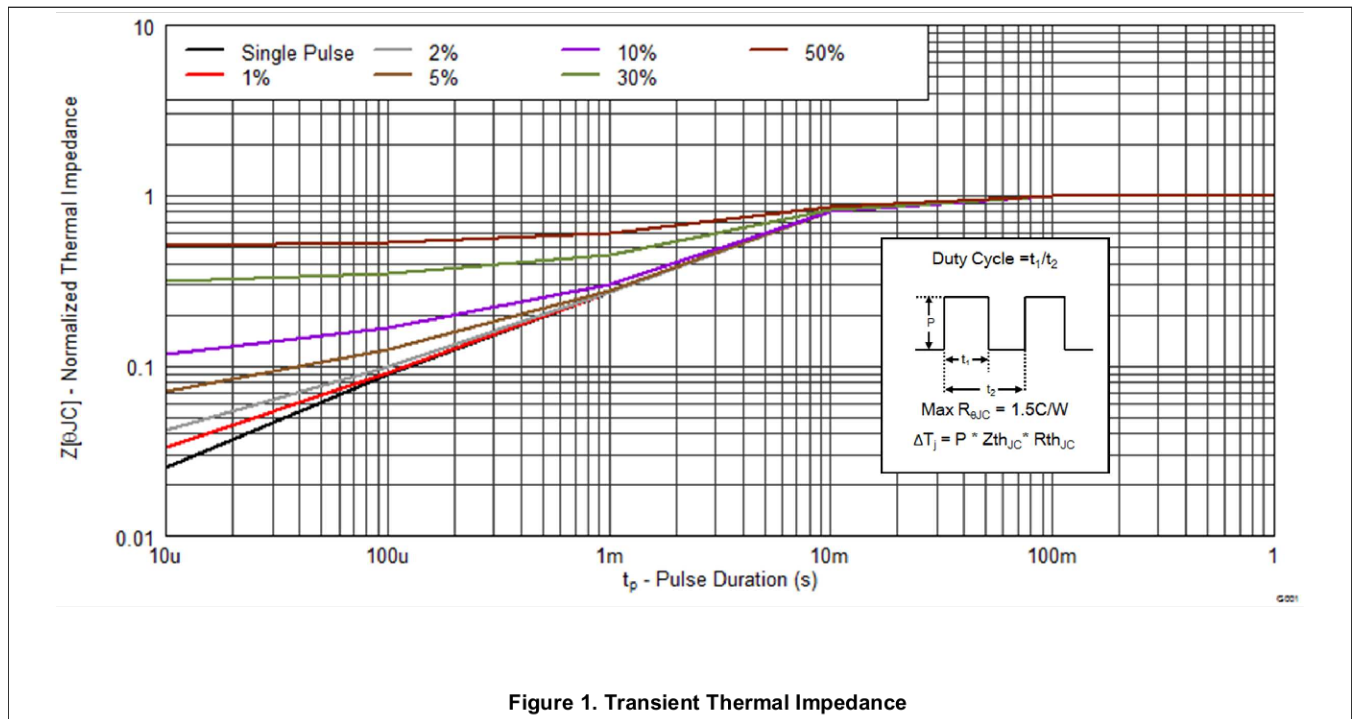
Max $R_{\theta JA} = 55^{\circ}\text{C/W}$
when mounted on
1 inch² of 2 oz. Cu.



Max $R_{\theta JA} = 160^{\circ}\text{C/W}$
when mounted on
minimum pad area of
2 oz. Cu.

5.3 Typical MOSFET Characteristics

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)



Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

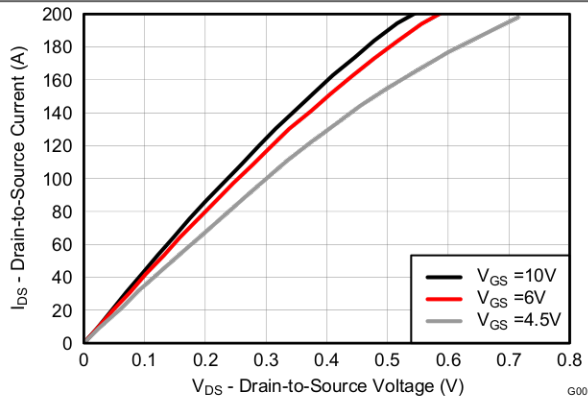


Figure 2. Saturation Characteristics

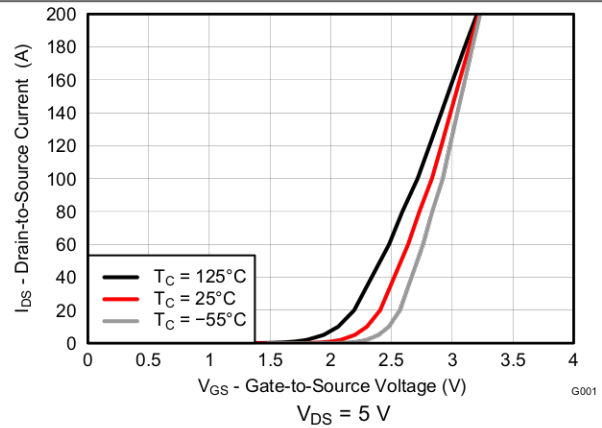


Figure 3. Transfer Characteristics

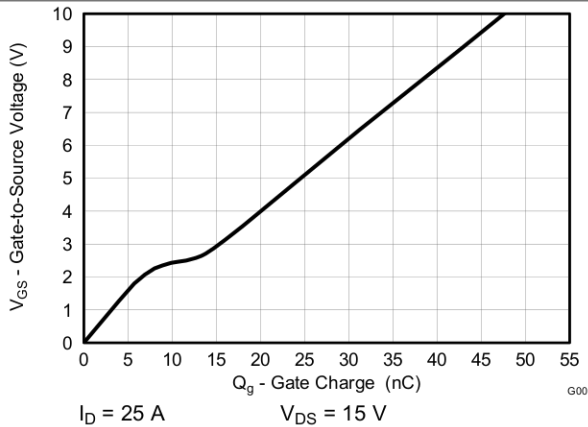


Figure 4. Gate Charge

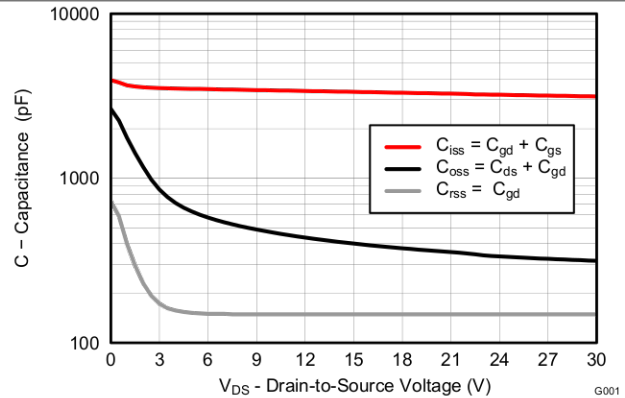


Figure 5. Capacitance

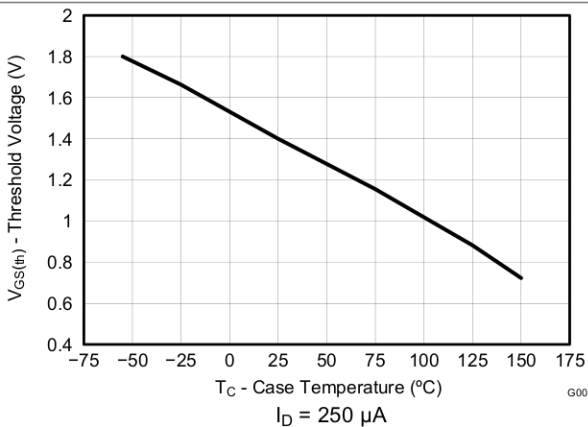


Figure 6. Threshold Voltage vs Temperature

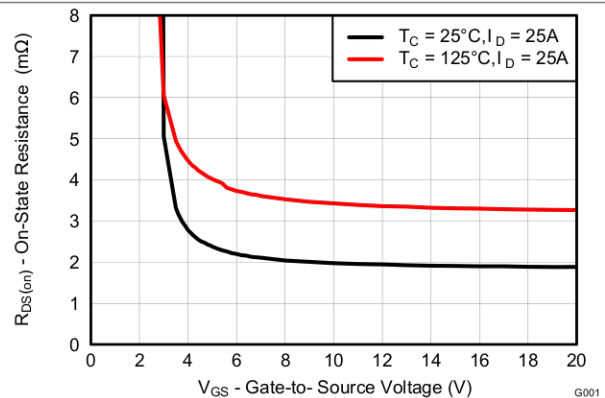


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

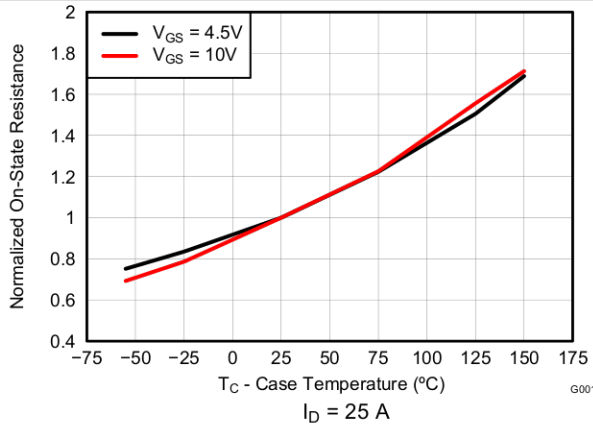


Figure 8. Normalized On-State Resistance vs Temperature

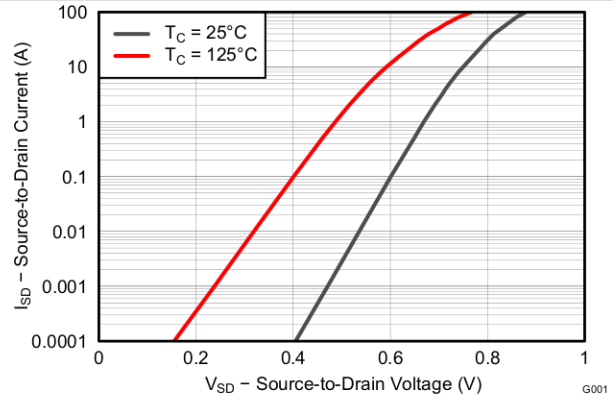


Figure 9. Typical Diode Forward Voltage

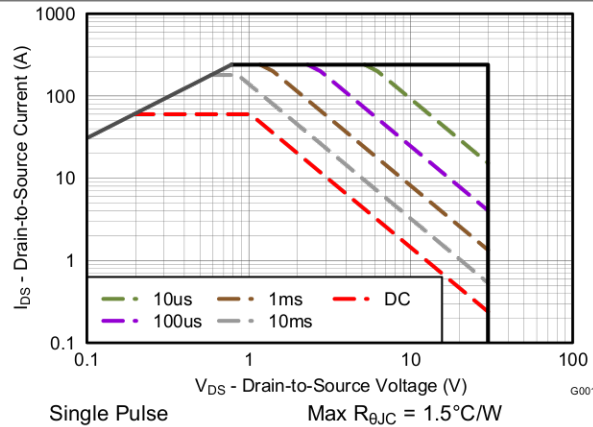


Figure 10. Maximum Safe Operating Area

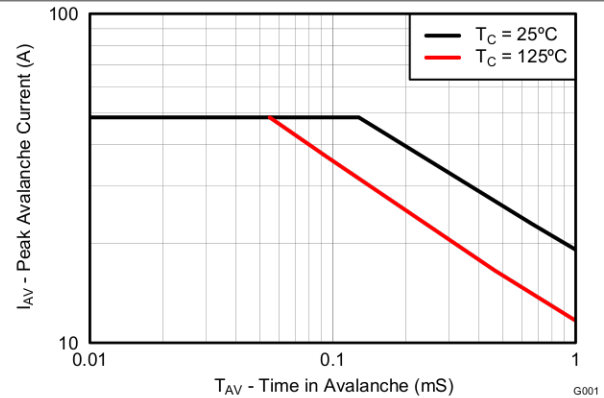


Figure 11. Single Pulse Unclamped Inductive Switching

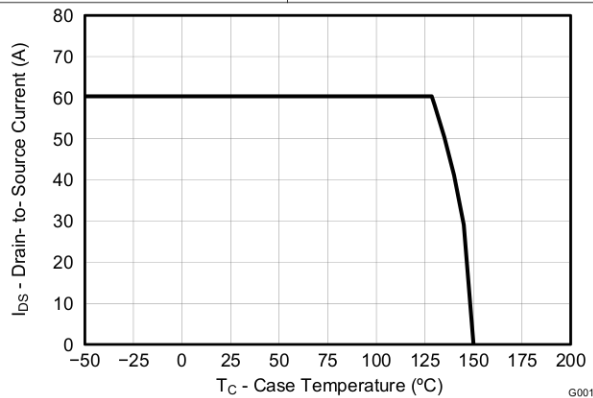


Figure 12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Trademarks

NexFET is a trademark of Texas Instruments.

6.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 Glossary

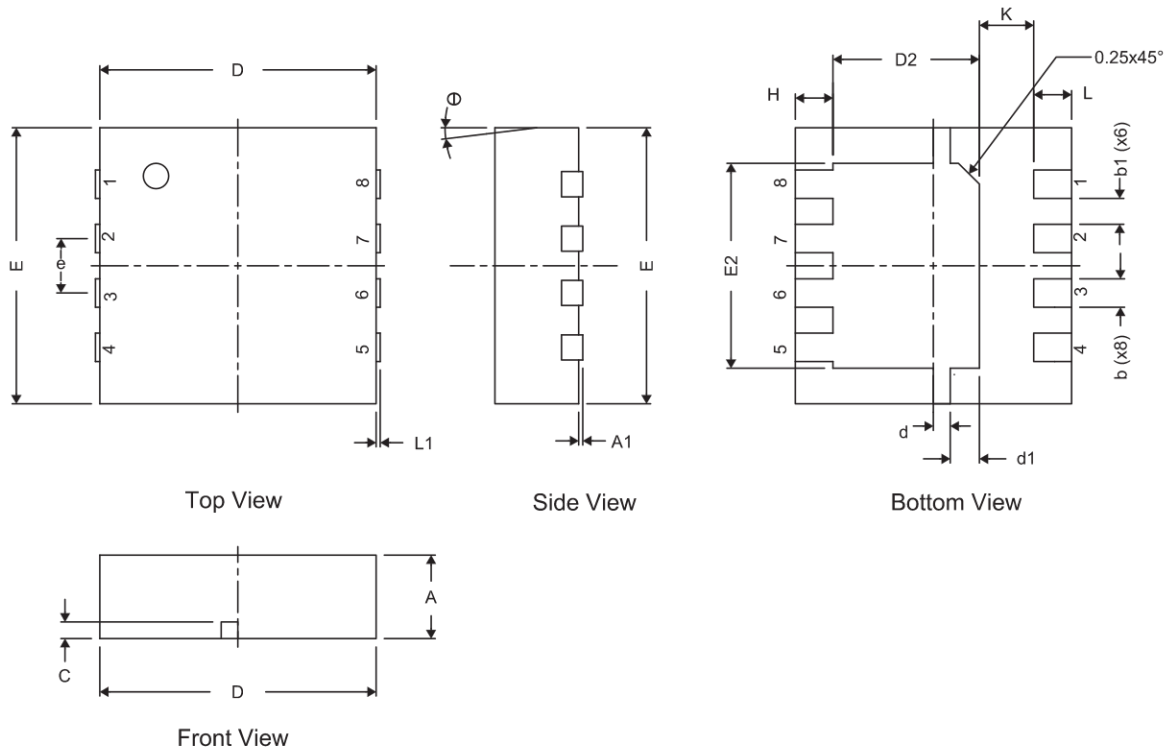
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

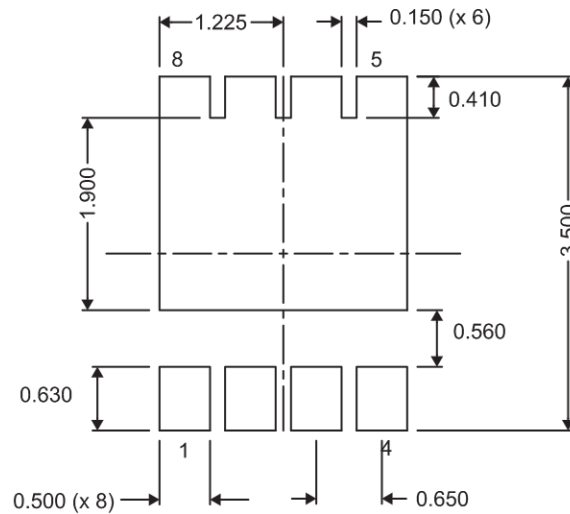
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Q3 Package Dimensions



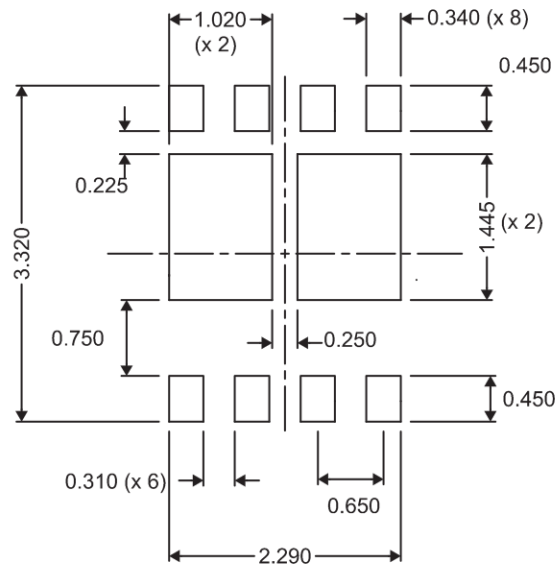
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.950	1.000	1.100	0.037	0.039	0.043
A1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.280	0.340	0.400	0.011	0.013	0.016
b1	0.310 NOM			0.012 NOM		
c	0.150	0.200	0.250	0.006	0.008	0.010
D	3.200	3.300	3.400	0.126	0.130	0.134
D2	1.650	1.750	1.800	0.065	0.069	0.071
d	0.150	0.200	0.250	0.006	0.008	0.010
d1	0.300	0.350	0.400	0.012	0.014	0.016
E	3.200	3.300	3.400	0.126	0.130	0.134
E2	2.350	2.450	2.550	0.093	0.096	0.100
e	0.650 TYP			0.026		
H	0.35	0.450	0.550	0.014	0.018	0.022
K	0.650 TYP			0.026 TYP		
L	0.35	0.450	0.550	0.014	0.018	0.022
L1	0	—	0	0	—	0
θ	0	—	0	0	—	0

7.2 Recommended PCB Pattern



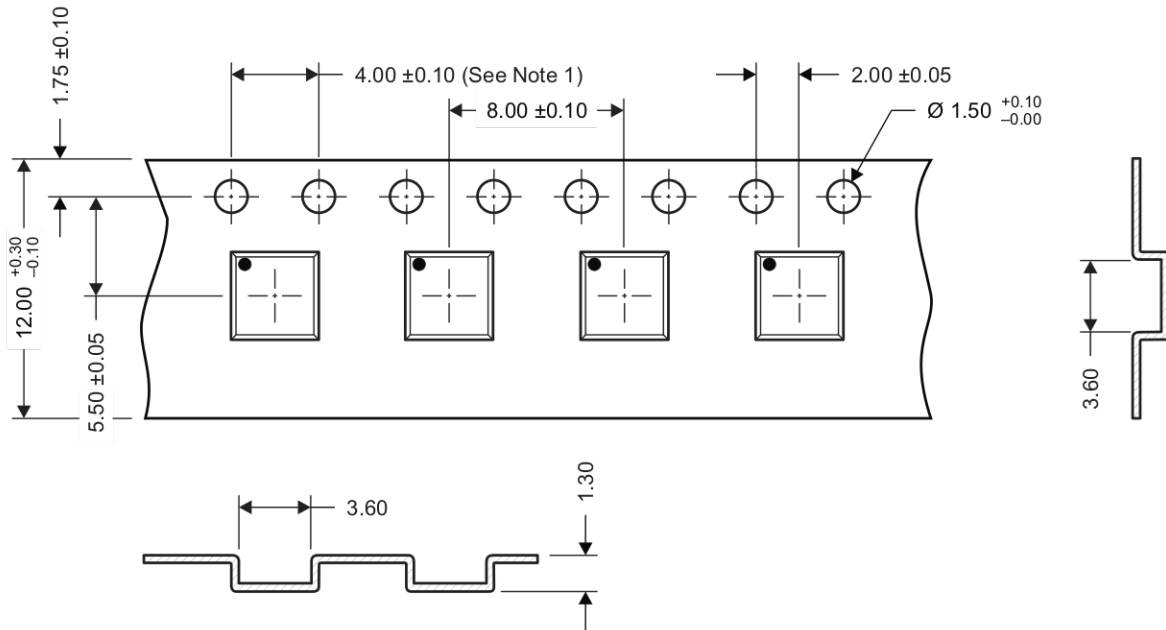
For recommended circuit layout for PCB designs, see application note [SLPA005](#) – *Reducing Ringing Through PCB Layout Techniques*.

7.3 Recommended Stencil Opening



All dimensions are in mm, unless otherwise specified.

7.4 Q3 Tape and Reel Information



M0144-01

Notes:

1. 10 sprocket hole pitch cumulative tolerance ± 0.2
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
3. Material: black static dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified).
5. Thickness: 0.30 ± 0.05 mm
6. MSL1 260°C (IR and Convection) PbF Reflow Compatible

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD17575Q3	ACTIVE	VSON-CLIP	DQG	8	2500	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM		CSD17575	Samples
CSD17575Q3T	ACTIVE	VSON-CLIP	DQG	8	250	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD17575	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



www.ti.com

10-Dec-2020

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated