National Semiconductor Corporation

PRELIMINARY

INS8243 Input/Output Expander

General Description

The INS8243 is an input/output device specifically designed to furnish input/output expansion capabilities for the INS8048, INS8049 and NS8050 single chip microcomputer family. The INS8243 is fabricated using XMOS™ (high density N-channel silicon gate) technology, operates from a single 5V supply and is TTL compatible. It is housed in a 24-pin, dual-in-line package and provides high drive current capabilities at low cost.

The INS8243 expander consists of five, 4-bit bidirectional ports. One port provides the interface with the INS8048/49/50 microcomputer. The remaining four ports provide the input/output expansion.

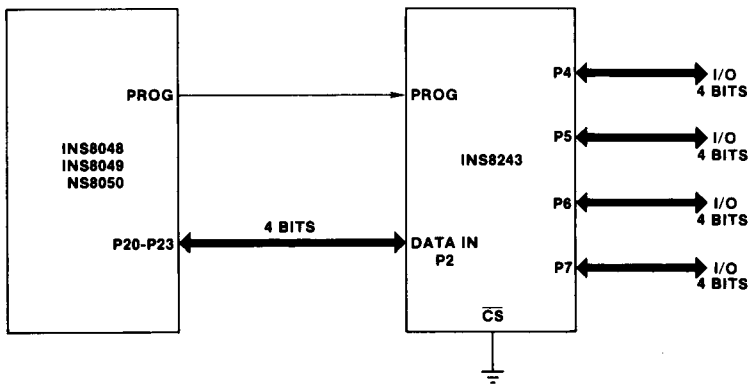
The INS8243 I/O ports function as a direct extension for the resident I/O port of the INS8048/49/50 microcomputer series and are accessed by the MOV, ANL or ORL instructions of the INS8048/49/50.

Features

- XMOS technology
- Single 5V supply
- Low cost I/O expansion
- Easy interface with INS8048/49/50 microcomputers
- High fanout capability
- 24-Pin DIP
- Direct extension of INS8048/49/50 I/O ports

Basic System Configuration

Single Expander Interface



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Absolute Maximum Ratings

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Voltage on Any Pin with Respect to GND	−0.5V to +7.0V

Note: *Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Electrical Characteristics.*

DC Electrical Characteristics T_A = 0°C to +70°C, V_{CC} = +5V ±10%, GND = 0V

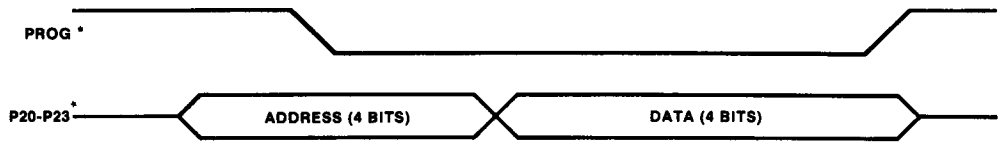
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Voltage		−0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC}+0.5	V
V_{OL1}	Output Low Voltage Ports 4–7	I_{OL} = 5 mA			0.45	V
V_{OL2}	Output Low Voltage Port 7	I_{OL} = 20 mA			1	V
V_{OH1}	Output High Voltage Ports 4–7	I_{OH} = 240 μA	2.4			V
I_{IL1}	Input Leakage Ports 4–7	V_{IN} = V_{CC} to 0V	−10		20	μA
I_{IL2}	Input Leakage Port 2, $\overline{CS}$, PROG	V_{IN} = V_{CC} to 0V	−10		10	μA
V_{OL3}	Output Low Voltage Port 2	I_{OL} = 0.6 mA			0.45	V
I_{CC}	V_{CC} Supply Current			10	20	mA
V_{OH2}	Output Voltage Port 2	I_{OH} = 100 μA	2.4			V
I_{OL}	Sum of all I_{OL} from 16 Output Ports	At 5 mA per pin			100	mA

AC Electrical Characteristics T_A = 0°C to +70°C, V_{CC} = +5V ±10%, GND = 0V

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
t_{SC}	Code Valid Before PROG	80 pF Load	100			ns
t_{HC}	Code Valid After PROG	20 pF Load	60			ns
t_{SD}	Data Valid Before PROG	80 pF Load	200			ns
t_{HD}	Data Valid After PROG	20 pF Load	20			ns
t_{FLT}	TRI-STATE After PROG	20 pF Load	0		150	ns
t_W	PROG Negative Pulse Width		700			ns
t_{CS}	$\overline{CS}$ Valid Before/After PROG		50			ns
t_{PO}	Ports 4–7 Valid After PROG	100 pF Load			700	ns
t_{LP1}	Ports 4–7 Valid Before/After PROG		100			ns
t_{ACC}	Port 2 Valid After PROG	80 pF Load			650	ns

Timing Waveforms (*These signals are generated by the INS8048/49/50.)

Expander Input Timing



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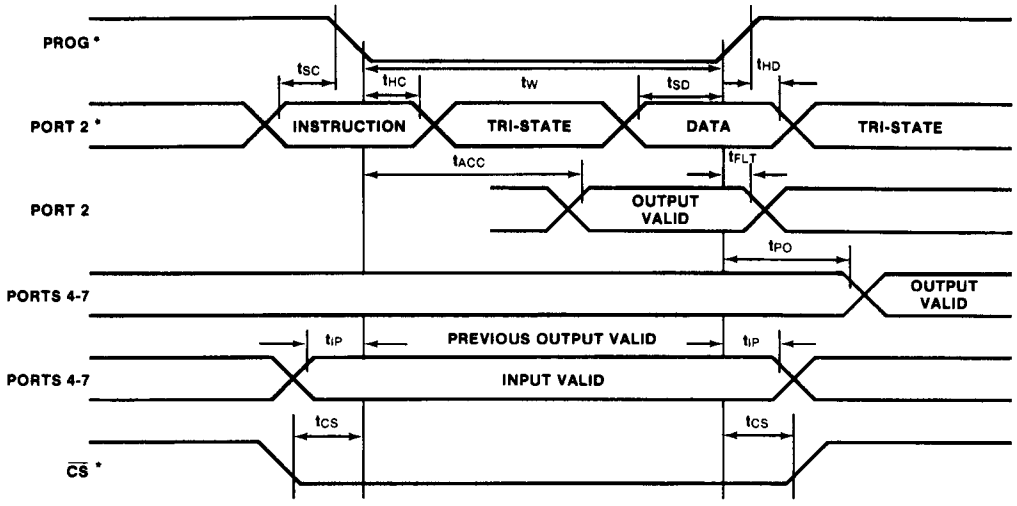
Input/Output Waveforms



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Functional Pin Descriptions

The following describes the function of the INS8243 input/output pins. Some of these descriptions reference internal circuits.

CONTROL SIGNALS

Chip Select ($\overline{CS}$): When $\overline{CS}$ is low (negative true), the 4-bit input to port 2 is enabled. A high on $\overline{CS}$ inhibits any input to port 2 and no change to internal status and output can occur.

Strobe Input (PROG): The low to high transition on the PROG indicates data is available at port 2; a high to low transition on PROG signifies command and address information is at port 2.

INPUT/OUTPUT SIGNALS

Port 2: Port 2 is a 4-bit bidirectional port that provides the interface between the INS8048/49/50 and the input/output ports 4–7. Communication between the INS8048/49/50 and the INS8243 is accomplished with 4-bit nibbles. A 4-bit nibble consists of two bits that comprise a functional command and two bits that indicate the address of a specific input/output port (P4–P7), or it consists of four data bits. The high to low transition of the PROG input indicates address and command bits are present at port P2. The low to high transition of the PROG input indicates that data bits are present at port P2. If the operation is a read function, data from a selected port (P4–P7) is read to the microcomputer via port 2, prior to the low to high transition of the PROG input. The tables below show the binary inputs for port and command selection.

Port Selection Table

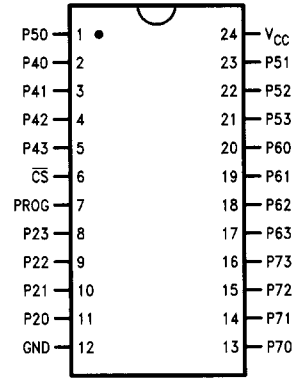
Input/Output Address Code		Selected Input/Output Port
P21	P20	
0	0	4
0	1	5
1	0	6
1	1	7

Functional Command Selection Table

Command Code		Function
P23	P22	
0	0	Read
0	1	Write
1	0	ORLD
1	1	ANLD

Ports 4–7 (PI): These are four, 4-bit bidirectional input/output ports. Each port is addressable and may be programmed to perform a read (input data) or write (output data) via a low impedance latched output. Data presented to port 2 during a write operation may be output directly to the addressed output port or logically ANDed or ORed with data existing in the selected port. For a read operation, data at the addressed port (P4–P7) is transferred to port 2.

Connection Diagram



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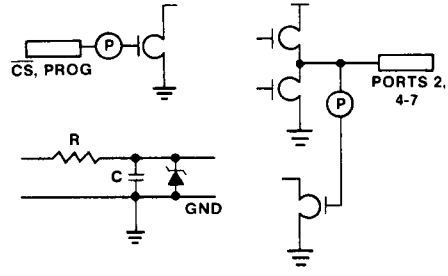
Order Number INS8243J
See NS Package J24A
Order Number INS8243N
See NS Package N24A

PROTECTION CIRCUITS

Figure 1 illustrates the protection circuits for the input and output pins.



P = Protection Device
τ = 10 ns = RC

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FIGURE 1. Protection Circuits for I/O Pins

Functional Description

The INS8243 *(Figure 2)* consists of four, 4-bit I/O ports that function as the extension of the INS8048/49/50 on-chip input/output port. The four I/O ports (P4 through P7) are addressable and the following programmed INS8048/49/50 instructions are used to access these ports. The instructions move data to/from the INS8048/49/50 accumulator via the INS8243. Timing for the transfer of data is provided by the INS8048/49/50 PROG output.

a. MOVD Pi,A—Shift accumulator data to the addressed port.

b. MOVD A,PI—Shift addressed port data to the accumulator.

c. ANLD Pi,A—ANDing accumulator data to addressed port.

d. ORLD Pi,A—ORing accumulator data to addressed port.

Port 2 of the INS8243 provides the communication interface between the expander and the INS8048/49/50 processor. Each communications exchange is comprised of two, 4-bit nibbles, one nibble consisting of command and address information, the second is a 4-bit data nibble. Timing for the I/O expander is provided by the processor on the PROG input pin.

POWER-ON INITIALIZING MODE

Application of DC power to the chip forces I/O port 2 to the input mode and I/O ports 4 through 7 to the TRI-STATE® output mode (high impedance state). The power-on sequence is initiated when V_{CC} falls below 1V. The input level on the PROG may be high or low when DC is first applied. The initial high to low transition of the PROG input forces the chip to exit the power-on mode.

READ MODE

The INS8243 I/O expander has one read mode that is initialized by the following instruction:

- MOVDA,Pi—instruction from INS8048/49/50 takes data from the addressed I/O port (P4–P7) and moves the data into the accumulator.

The command code and port address code are latched from the input port 2 on the high to low transition of the PROG input pin. When the read command and the port address are decoded, the data from the addressed port is presented back to the INS8048/49/50 on port P2. Termination of the read command occurs on the low to high transition of the PROG input. The port (4, 5, 6 or 7) that was addressed switches to the high impedance state and port 2 reverts to the input (read) mode. A port will normally be in either write (output) mode or read (input) mode. To allow for the settling of the external driver on the port, the first read following a write should be discounted when modes are changed during operation. All succeeding reads are valid.

WRITE MODES

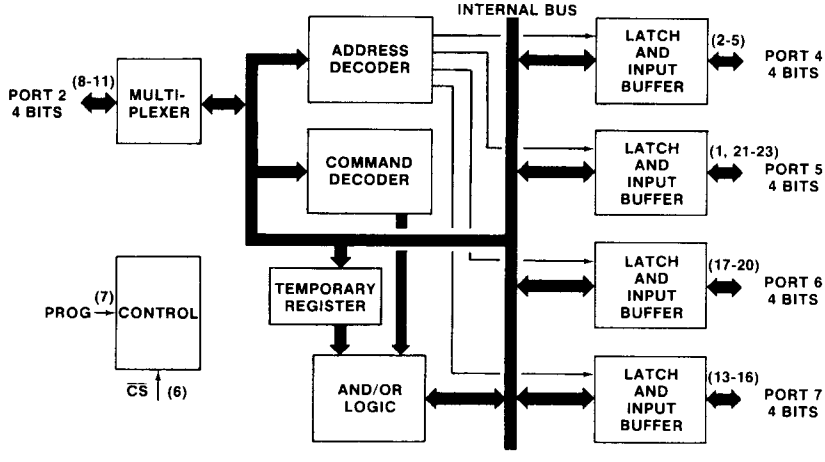
The INS8243 has three write modes that are initialized by the following instructions:

a. MOVD Pi,A—Instruction from the INS8048/49/50 writes new data directly into the addressed port. Existing data is lost.

b. ORLD Pi,A—Instruction from the INS8048/49/50 takes port P2 data, logically ORing it with the existing data in the addressed port and writes the resultant data into the port.

c. ANLD Pi,A—Instruction from the INS8048/49/50 takes port P2 data, logically ANDing it with the existing data in the addressed port and writes the ANDed data into the port.

Command and port address codes are latched from the port 2 input on the high to low transition of the PROG input. Data on port 2 is deposited in the logic circuits of the addressed port. When the logic manipulation has been performed, data is latched and output. Old data stays latched until valid new outputs are written.



Note: Applicable pinout numbers are included within parentheses.

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FIGURE 2. INS8243 I/O Expander Block Diagram

Functional Description (Continued)

MULTIPLE INS8243 I/O EXPANDER USE

To expand the resident I/O port capabilities of the INS8048/49/50 microcomputer series sixteen times, four INS8243 expanders may be connected to the microcomputer, as shown in *Figure 3*. By using the high order bit outputs P24 through P27 as the chip select ($\overline{CS}$) input to the I/O expanders, no additional logic circuits are required. A negative true input (low) on the $\overline{CS}$ line will enable the port 2 input for the selected I/O expander. A single INS8048/49/50 microcomputer may use many (up to twenty) I/O expanders without additional logic circuits on the same bus, limited only by the availability of chip select lines and loading restrictions.

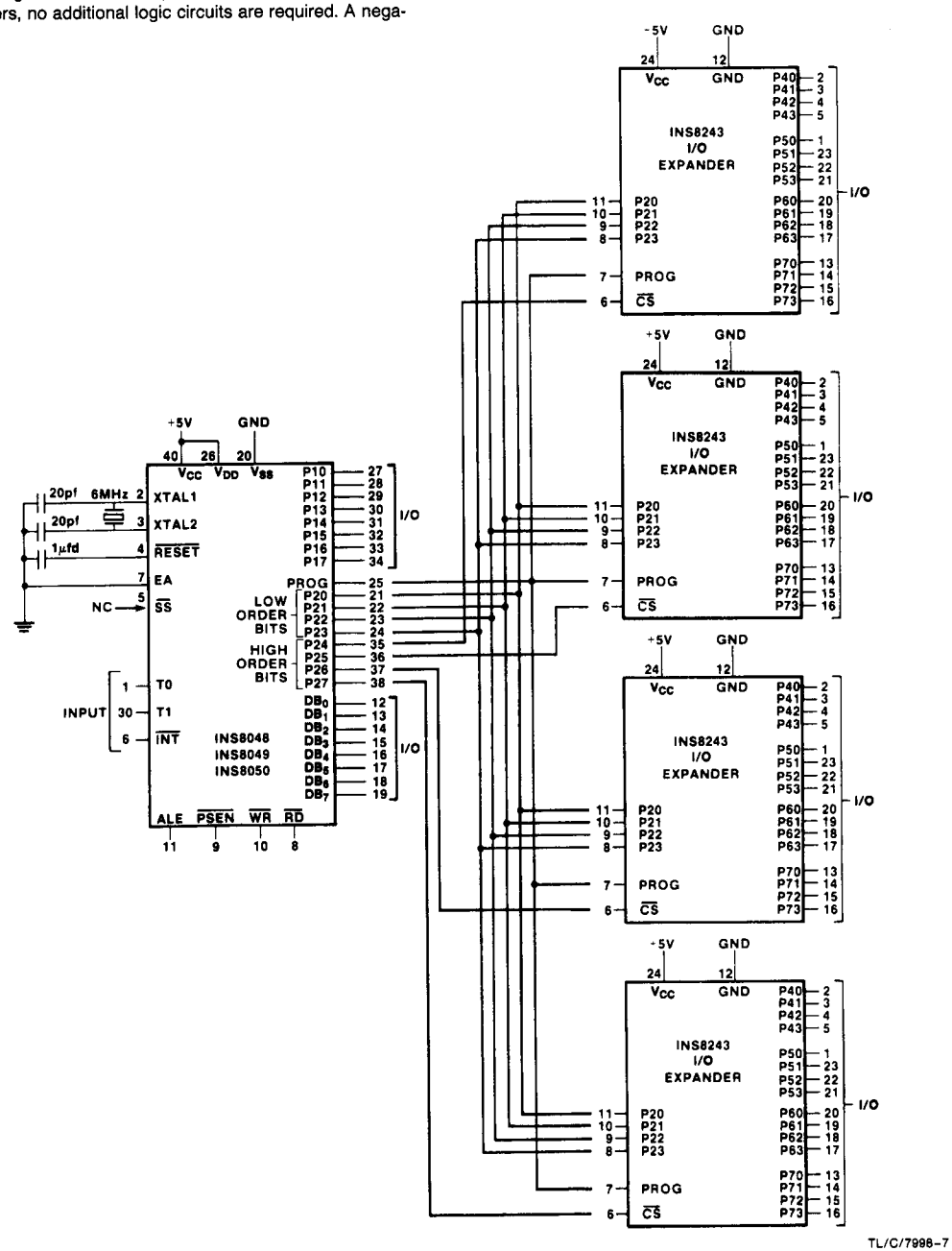

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FIGURE 3. Typical Connections Using INS8243 I/O Expander

Functional Description (Continued)

Larger numbers of INS8243 expanders would require chip select decoder chips to conserve miocrocomputer I/O pins.

Operation of the INS8243 expander selected in the same as was explained in the functional description. *Figure 4* is a typical system application.

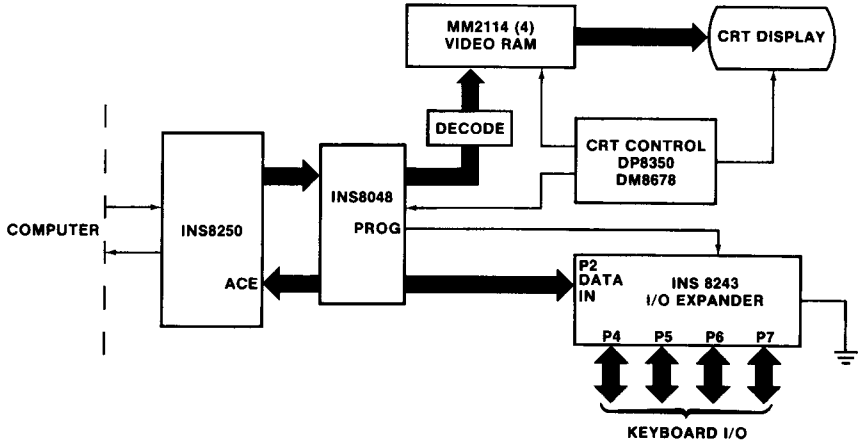

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FIGURE 4. Typical System Application