TEXAS INSTRUMENTS

SN54HC594, SN74HC594

SCLS040G – DECEMBER 1982 – REVISED MARCH 2015

SNx4HC594 8-Bit Shift Registers With Output Registers

1 Features

- Wide Operating Voltage Range of 2 V to 6 V
- High-Current Outputs Can Drive up to 15 LSTTL Loads
- Low Power Consumption, 80-μA Maximum I_{CC}
- Typical t_{pd} = 15 ns
- ±6-mA Output Drive at 5 V
- Low Input Current of 1 μA Maximum
- 8-Bit Serial-In, Parallel-Out Shift Registers With Storage
- Independent Direct Overriding Clears on Shift and Storage Registers
- Independent Clocks for Both Shift and Storage Registers

2 Applications

- Pro Audio Mixer
- Elevators and Escalators
- Human Machine Interface (HMI): Industrial Monitor
- Entertainment Systems
- Grid Infrastructure: Grid Control
- Access Control and Security: DVR and DVS

3 Description

The SNx4HC594 devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks and direct overriding clear (RCLR, SRCLR) inputs are provided on both the shift and storage registers. A serial ($Q_{H'}$) output is provided for cascading purposes.

Both the shift register (SRCLK) and storage register (RCLK) clocks are positive edge triggered. If both clocks are connected together, the shift register always is one count pulse ahead of the storage register.

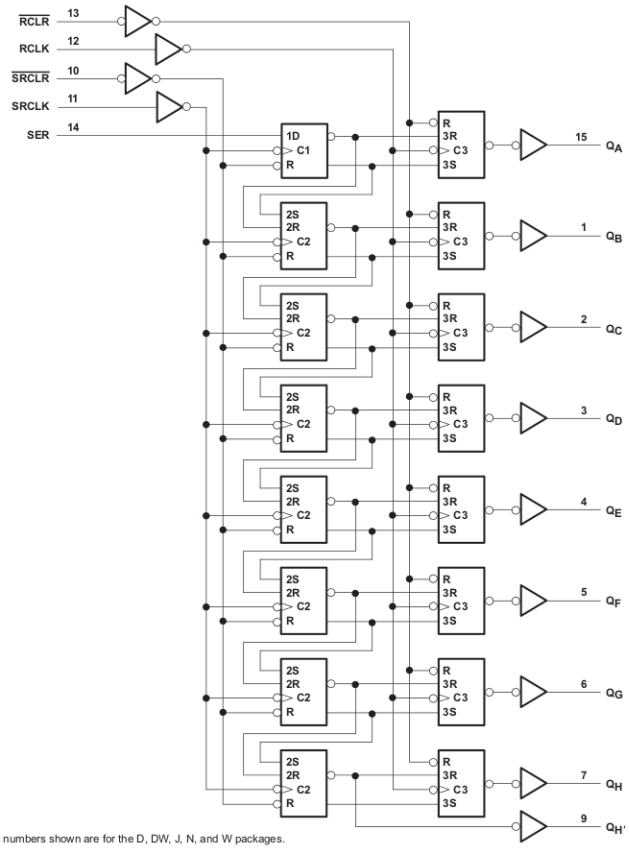
The parallel (Q_A – Q_H) outputs have high-current capability. $Q_{H'}$ is a standard output.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74HC594	PDIP (16)	19.30 mm × 6.35 mm
	SOIC (16)	9.00 mm × 9.00 mm
		10.30 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Logic Diagram (Positive Logic)



Pin numbers shown are for the D, DW, J, N, and W packages.

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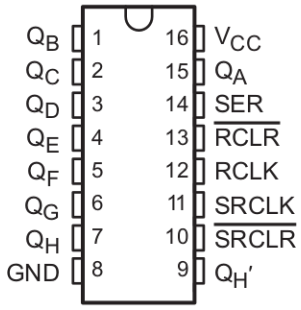
4 Revision History

Changes from Revision F (October 2003) to Revision G **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Removed ordering information. ... 1
- ESD warning added. ... 1

5 Pin Configuration and Functions

D, DW, or N Package
16-PIN PDIP or SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	Q_B	O	Output B
2	Q_C	O	Output C
3	Q_D	O	Output D
4	Q_E	O	Output E
5	Q_F	O	Output F
6	Q_G	O	Output G
7	Q_H	O	Output H
8	GND	–	Ground
9	$Q_{H'}$	O	Q_H inverted
10	$\overline{SRCLR}$	I	Serial clear
11	SRCLK	I	Serial clock
12	RCLK	I	Storage clock
13	$\overline{RCLK}$	I	Storage clear
14	SER	I	Serial input
15	Q_A	O	Output A
16	Vcc	–	Power pin

6 Specifications

6.1 Absolute Maximum Ratings (1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input clamp current (2)	$V_I < 0$ or $V_I > V_{CC}$	–20	20	mA
I_{OK}	Output clamp current (2)	$V_O < 0$ or $V_O > V_{CC}$	–20	20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}	–35	35	mA
	Continuous current through V_{CC} or GND		–70	70	mA
θ_{JA}	Package thermal impedance (3)	D package		73	°C/W
		DW package		57	
		N package		67	
T_{stg}	Storage temperature		–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)

			SN54HC594 (2)			SN74HC594			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V			0.5			0.5	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 6 V			1.8			1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) rate	V_{CC} = 2 V			1000			1000	ns
		V_{CC} = 4.5 V			500			500	
		V_{CC} = 6 V			400			400	
T_A	Operating free-air temperature		–55		125	–40		125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.
(2) Product Preview

6.4 Thermal Information

THERMAL METRIC[1]		SN74HC594			UNIT
		N (PDIP)	D (SOIC)	DW (SOIC)	
		16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.3	72.3	71	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28	33.2	32.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	21.3	29.9	35.9	
ψ_{JT}	Junction-to-top characterization parameter	12.6	5.3	6.7	
ψ_{JB}	Junction-to-board characterization parameter	21.1	29.6	35.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			V_{CC}	T_A = 25°C			SN54HC594[1] –55°C to 125°C		SN74HC594 –40°C to 85°C		SN74HC594 –40°C to 125°C		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 µA		2 V	1.9	1.998		1.9		1.9		1.9		V
				4.5 V	4.4	4.499		4.4		4.4		4.4		
				6 V	5.9	5.999		5.9		5.9		5.9		
		$Q_{H'}$	I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		3.84		
		Q_A – Q_H	I_{OH} = –6 mA		3.98	4.3		3.7		3.84		3.84		
		$Q_{H'}$	I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		5.34		
		Q_A – Q_H	I_{OH} = –7.8 mA		5.48	5.8		5.2		5.34		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 µA		2 V		0.002	0.1		0.1		0.1		0.1	V
				4.5 V		0.001	0.1		0.1		0.1		0.1	
				6 V		0.001	0.1		0.1		0.1		0.1	
		$Q_{H'}$	I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33		0.33	
		Q_A – Q_H	I_{OL} = 6 mA			0.17	0.26		0.4		0.33		0.33	
		$Q_{H'}$	I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33		0.33	
		Q_A – Q_H	I_{OL} = 7.8 mA			0.15	0.26		0.4		0.33		0.33	
I_I	V_I = V_{CC} or 0			6 V		±0.1	±100		±1000		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0		6 V			8		160		80		80	µA
C_i				2 V to 6 V		3	10		10		10			pF

(1) Product Preview

6.6 Switching Characteristics: C_L = 50 pF

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC594[1] –55°C to 125°C		SN74HC594 –40°C to 85°C		SN74HC594 –40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	5	8		3.3		4		4		MHz
			4.5 V	25	35		17		20		20		
			6 V	29	40		20		24		24		
t_{pd}	SRCLK	$Q_{H'}$	2 V		50	150		225		185		200	ns
			4.5 V		20	30		45		37		42	
			6 V		15	25		38		31		36	
	RCLK	Q_A – Q_H	2 V		50	150		225		185		200	
			4.5 V		20	30		45		37		42	
			6 V		15	25		38		31		36	
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$	2 V		50	150		225		185		200	ns
			4.5 V		20	30		45		37		42	
			6 V		15	25		38		31		36	
	$\overline{RCLR}$	Q_A – Q_H	2 V		50	125		185		155		170	
			4.5 V		20	25		37		31		36	
			6 V		15	21		31		26		31	
t_t		$Q_{H'}$	2 V		38	75		110		95		110	ns
			4.5 V		8	15		22		19		21	
			6 V		6	13		19		16		18	
		Q_A – Q_H	2 V		38	60		90		75		85	
			4.5 V		8	12		18		15		17	
			6 V		6	10		15		13		15	

(1) Product Preview

6.7 Switching Characteristics: C_L = 150 pF

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC594[1] –55°C to 125°C		SN74HC594 –40°C to 85°C		SN74HC594 –40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	RCLK	Q_A – Q_H	2 V		90	200		300		250		270	ns
			4.5 V		23	40		60		50		55	
			6 V		19	34		51		43		48	
t_{PHL}	$\overline{RCLR}$	Q_A – Q_H	2 V		90	200		300		250		270	ns
			4.5 V		23	40		60		50		55	
			6 V		19	34		51		43		48	
t_t		Q_A – Q_H	2 V		45	210		315		265		285	ns
			4.5 V		17	42		63		53		58	
			6 V		13	36		53		45		50	

(1) Product Preview

6.8 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC594 (1) –55°C to 125°C		SN74HC594 –40°C to 85°C		SN74HC594 –40°C to 125°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V		5		3.3		4		4	MHz
			4.5 V		25		17		20		20	
			6 V		29		20		24		24	
t_w	Pulse duration	SRCLK or RCLK high or low	2 V	100		150		125		130		ns
			4.5 V	20		30		25		27		
			6 V	17		25		21		23		
		$\overline{SRCLR}$ or $\overline{RCLR}$ low	2 V	100		150		125		130		
			4.5 V	20		30		25		27		
			6 V	17		25		21		23		
t_{su}	Setup time before CLK↑	SER before SRCLK↑	2 V	90		135		110		115		ns
			4.5 V	18		27		22		24		
			6 V	15		23		19		21		
		SRCLK↑ before RCLK↑ (2)	2 V	90		135		110		115		
			4.5 V	18		27		22		24		
			6 V	15		23		19		21		
		$\overline{SRCLR}$ low before RCLK↑	2 V	50		75		63		68		ns
			4.5 V	10		15		13		15		
			6 V	9		13		11		13		
		$\overline{SRCLR}$ high (inactive) before SRCLK↑	2 V	20		20		20		20		
			4.5 V	10		10		10		10		
			6 V	10		10		10		10		
		$\overline{RCLR}$ high (inactive) before SRCLK↑	2 V	5		5		5		5		
			4.5 V	5		5		5		5		
			6 V	5		5		5		5		
t_h	Hold time, SER after SRCLK↑		2 V	5		5		5		5		ns
			4.5 V	5		5		5		5		
			6 V	5		5		5		5		

(1) Product Preview
(2) This setup time ensures that the output register receives stable data from the shift-register outputs. The clocks may be tied together, in which case the output register is one clock pulse behind the shift register.

6.9 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	395	pF

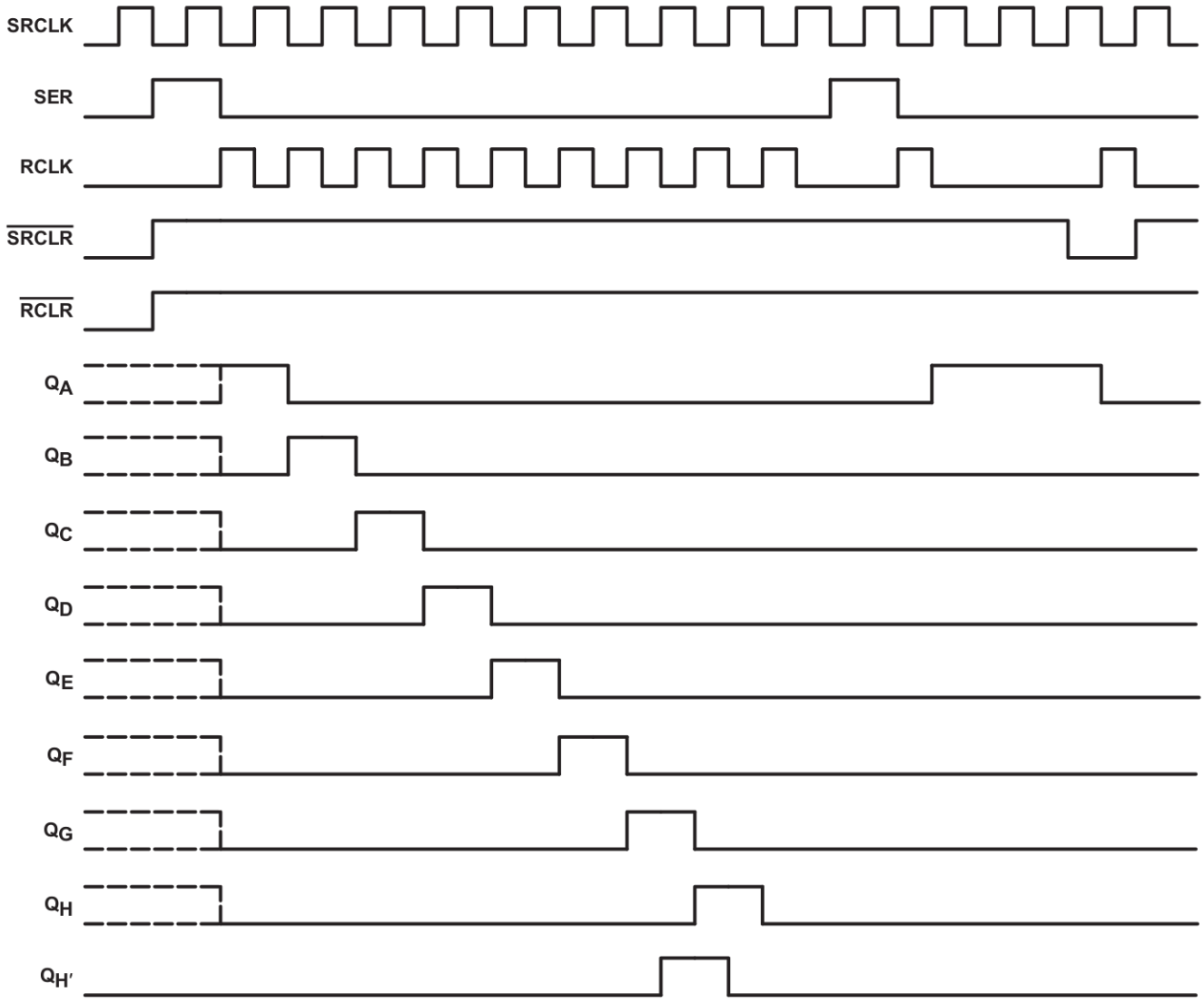


Figure 1. Timing Diagram

6.10 Typical Characteristics

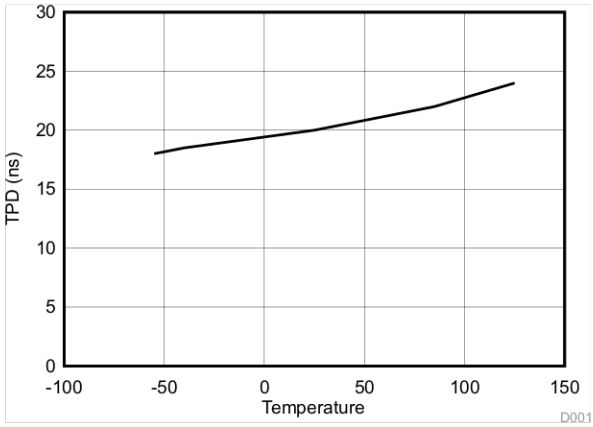


Figure 2. SN74HC594 TPD vs. Temperature

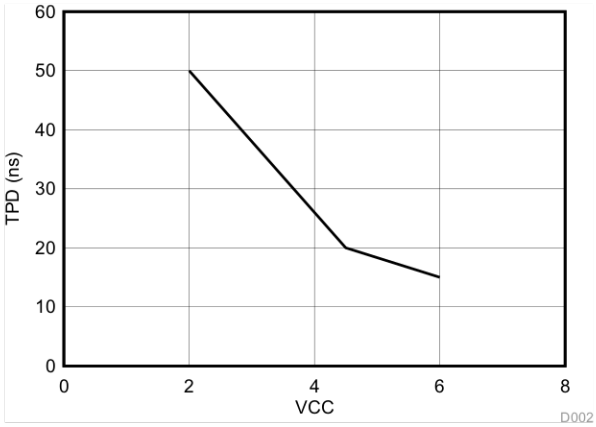
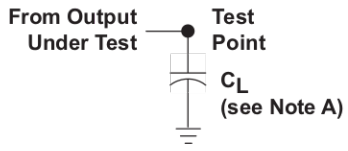
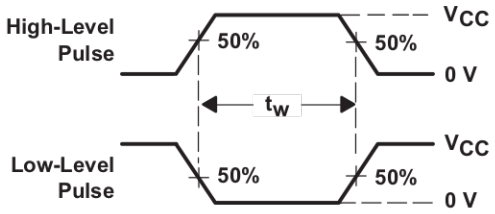


Figure 3. SN74HC594 TPD vs. VCC

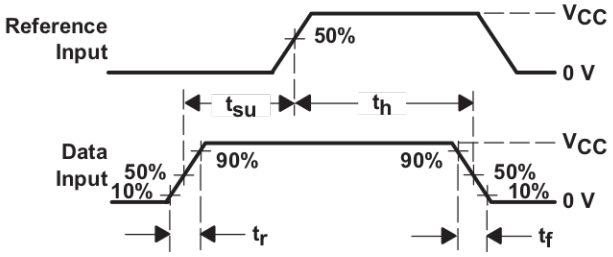
7 Parameter Measurement Information



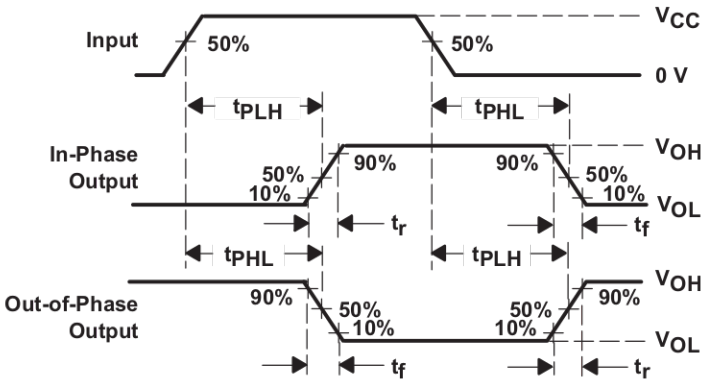
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

A. C_L includes probe and test-fixture capacitance.

B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.

C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.

D. The outputs are measured one at a time with one input transition per measurement.

E. t_{PLH} and t_{PHL} are the same as t_{pd}.

F. t_f and t_r are the same as t_t.

Figure 4. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SNx4HC594 devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks and direct overriding clear ($\overline{RCLR}$, $\overline{SRCLR}$) inputs are provided on both the shift and storage registers. A serial ($Q_{H'}$) output is provided for cascading purposes.

Both the shift register (SRCLK) and storage register (RCLK) clocks are positive edge triggered. If both clocks are connected together, the shift register always is one count pulse ahead of the storage register.

The parallel ($Q_A - Q_H$) outputs have high-current capability. $Q_{H'}$ is a standard output.

8.2 Functional Block Diagram

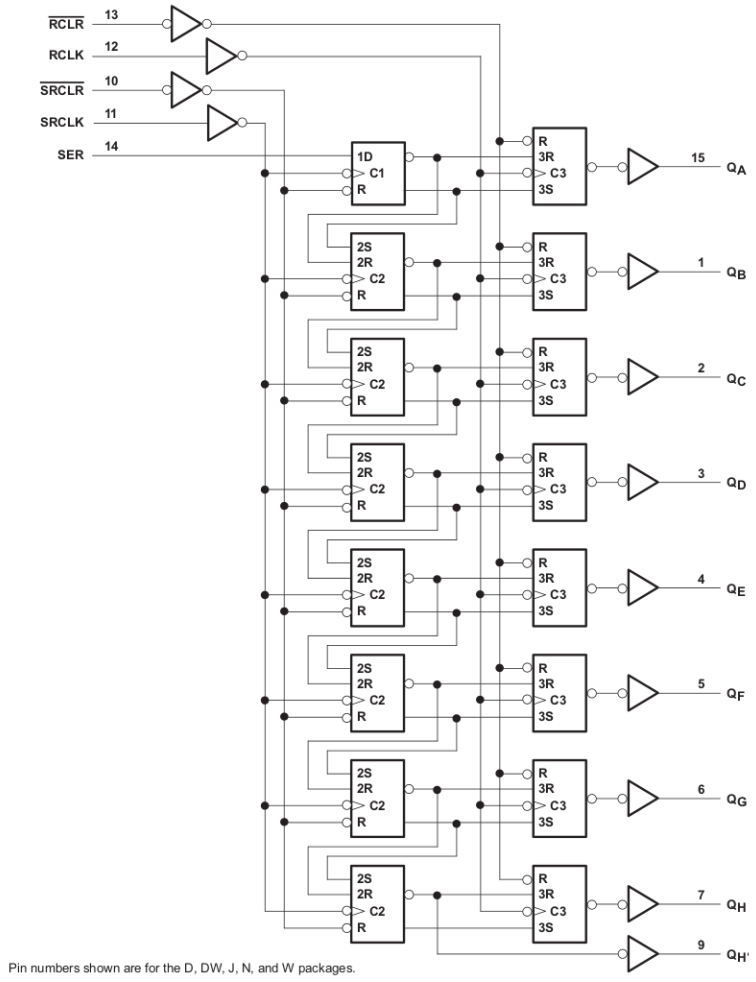


Figure 5. Logic Diagram (Positive Logic)

8.3 Feature Description

The wide operating range allows the device to be used in a variety of systems that use different logic levels. The high-current outputs allow the device to drive medium loads without significant drops in output voltage. In addition, the low power consumption makes this device a good choice for portable and battery power-sensitive applications.

8.4 Device Functional Modes

Table 1. Function Table

INPUTS					FUNCTION
SER	SRCLK	$\overline{\text{SRCLR}}$	RCLK	$\overline{\text{RCLR}}$	
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of shift register goes high. Other stages store the data of previous stage, respectively.
L	↓	H	X	X	Shift register state is not changed.
X	X	X	X	L	Storage register is cleared.
X	X	X	↑	H	Shift register data is stored in the storage register.
X	X	X	↓	H	Storage register state is not changed.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74HC594 is a low drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs.

9.2 Typical Application

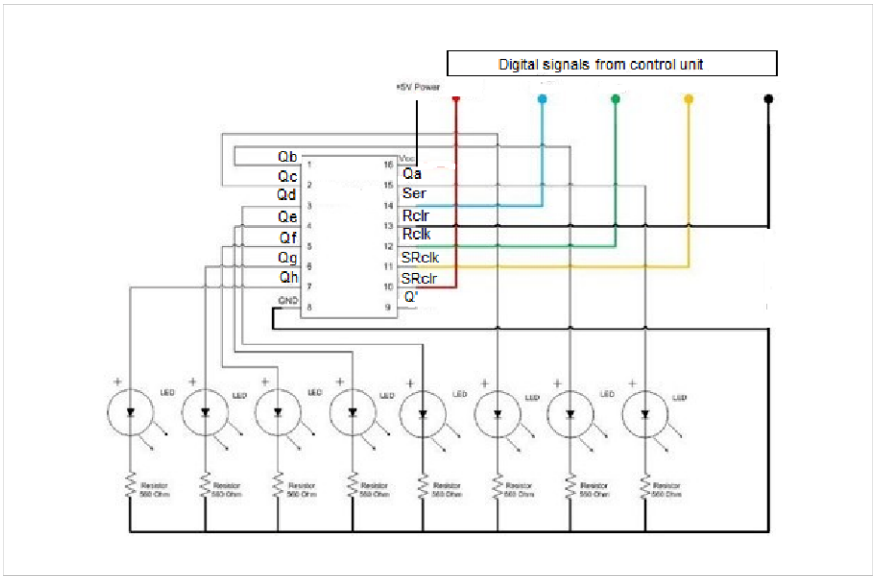


Figure 6. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so consider routing and load conditions to prevent ringing.

Typical Application (continued)

9.2.2 Detailed Design Procedure

- Recommended input conditions:
  - Rise time and fall time specs see (Δt/ΔV) in *Recommended Operating Conditions* table.
  - Specified High and low levels. See (V_{IH} and V_{IL}) in *Recommended Operating Conditions* table.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}
- Recommended output conditions:
  - Load currents should not exceed 35 mA per output and 70 mA total for the part
  - Outputs should not be pulled above V_{CC}

9.2.3 Application Curves

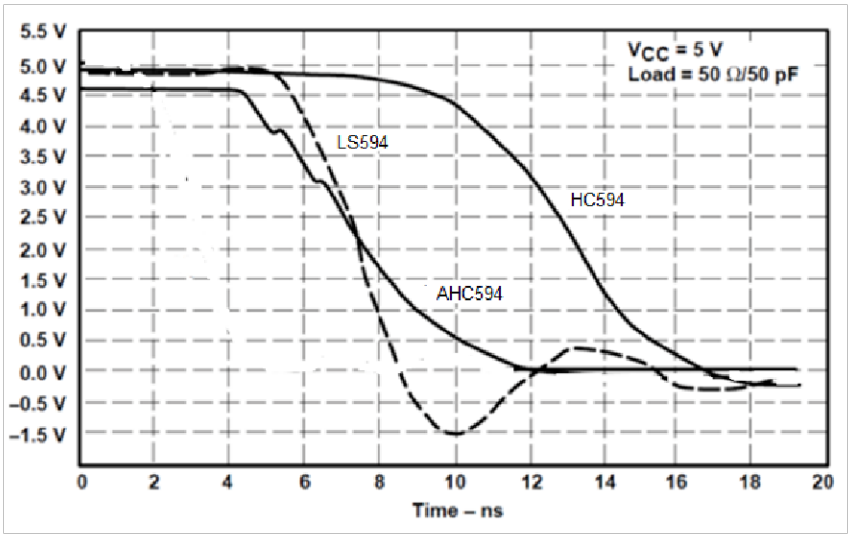


Figure 7. Switching Characteristics Comparison

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-µF capacitor and if there are multiple V_{CC} terminals then TI recommends a 0.01-µF or 0.022-µF capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close as possible to the power terminal for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. Floating outputs is generally acceptable, unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the I.O's so they also cannot float when disabled.

11.2 Layout Example

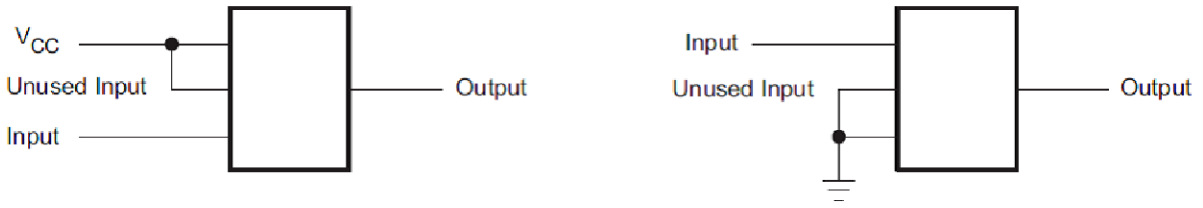


Figure 8. Layout Recommendation

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

Implications of Slow or Floating CMOS Inputs, SCBA004

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HC594D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC594	Samples
SN74HC594DG4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC594	Samples
SN74HC594DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC594	Samples
SN74HC594DT	ACTIVE	SOIC	D	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC594	Samples
SN74HC594DW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC594	Samples
SN74HC594DWE4	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC594	Samples
SN74HC594DWG4	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC594	Samples
SN74HC594DWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC594	Samples
SN74HC594DWRE4	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC594	Samples
SN74HC594DWRG4	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC594	Samples
SN74HC594N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	SN74HC594N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

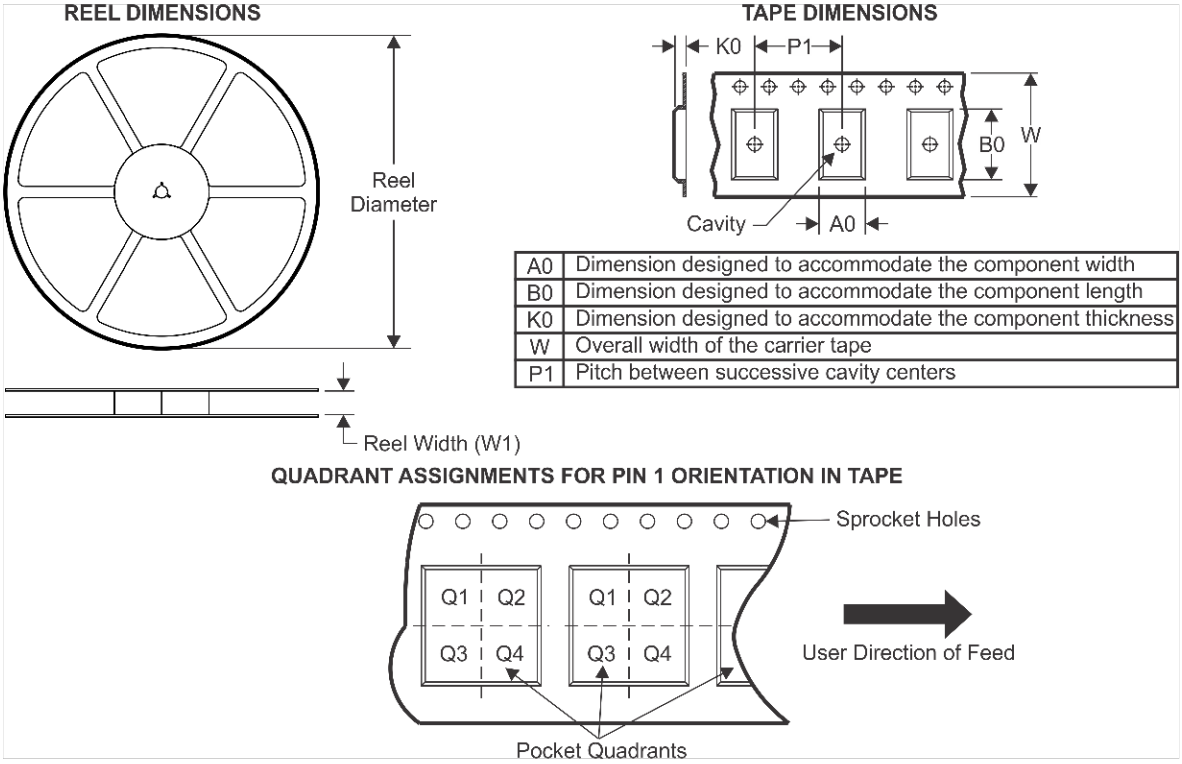
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

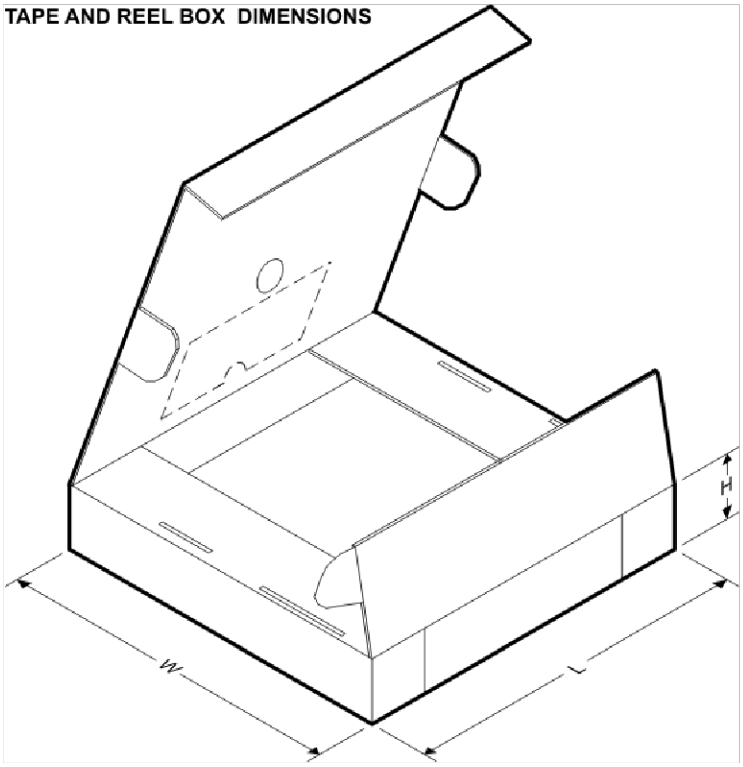


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC594DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC594DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
SN74HC594DWRG4	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

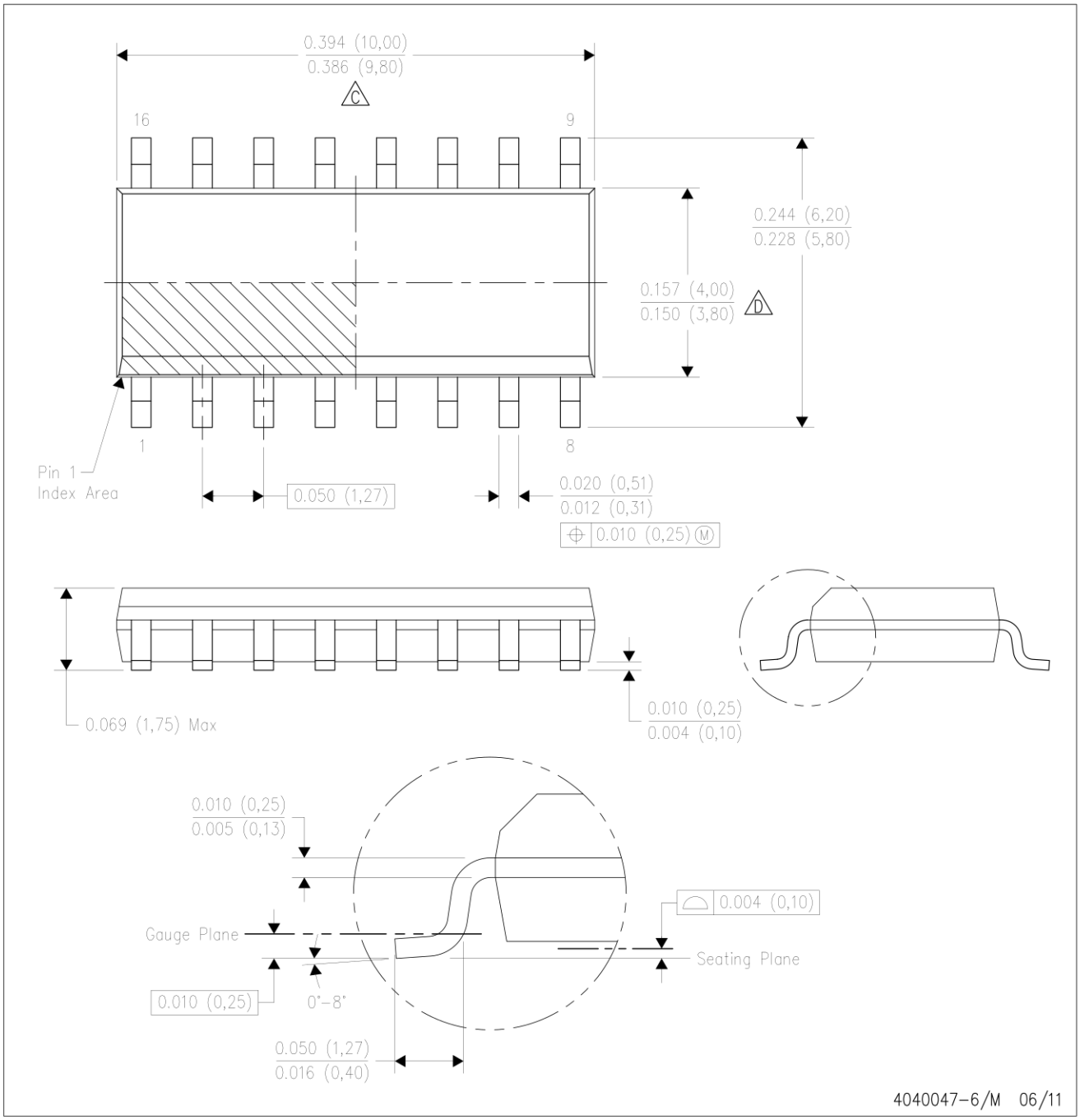
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

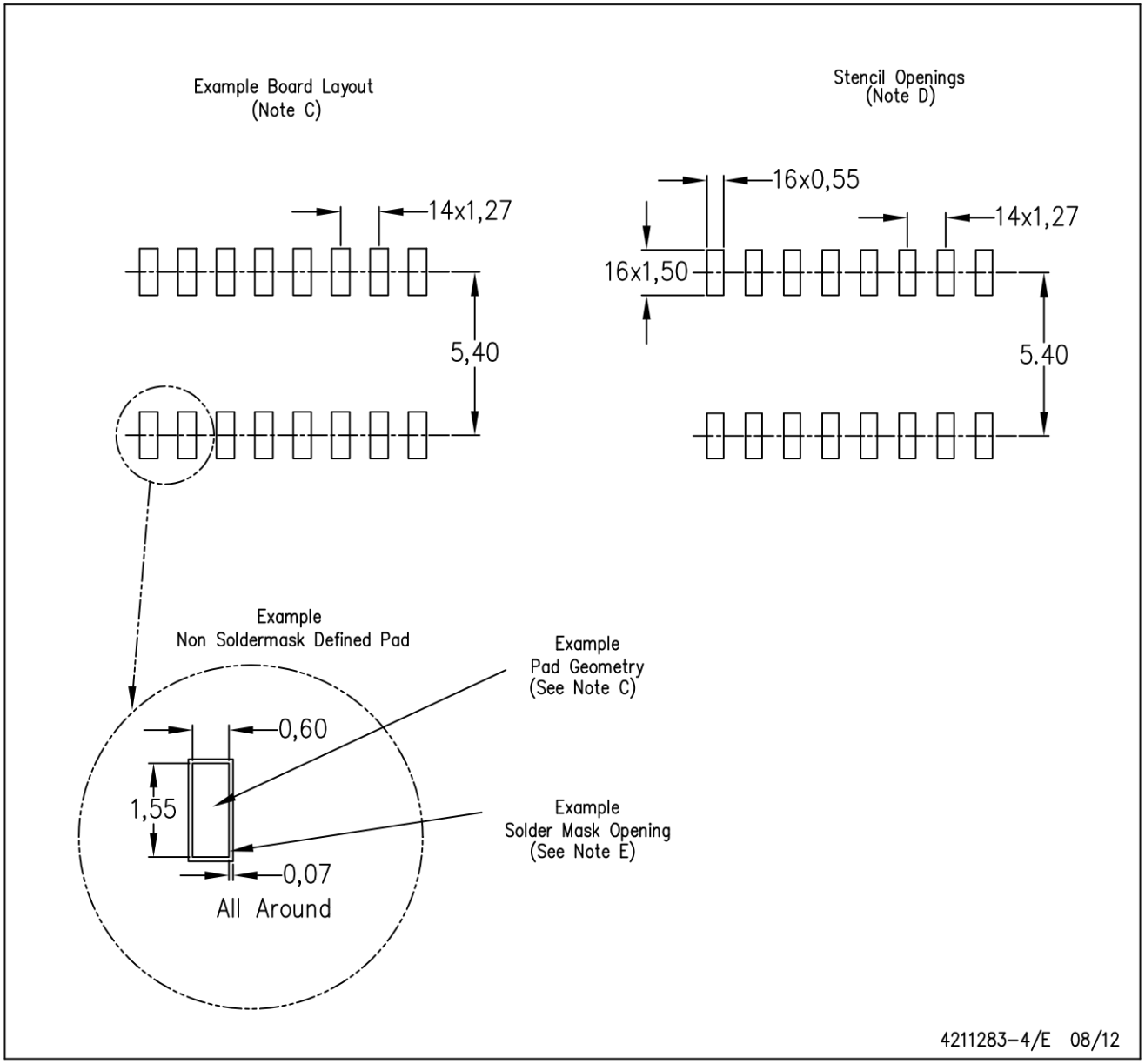
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC594DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74HC594DWR	SOIC	DW	16	2000	350.0	350.0	43.0
SN74HC594DWRG4	SOIC	DW	16	2000	350.0	350.0	43.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

GENERIC PACKAGE VIEW

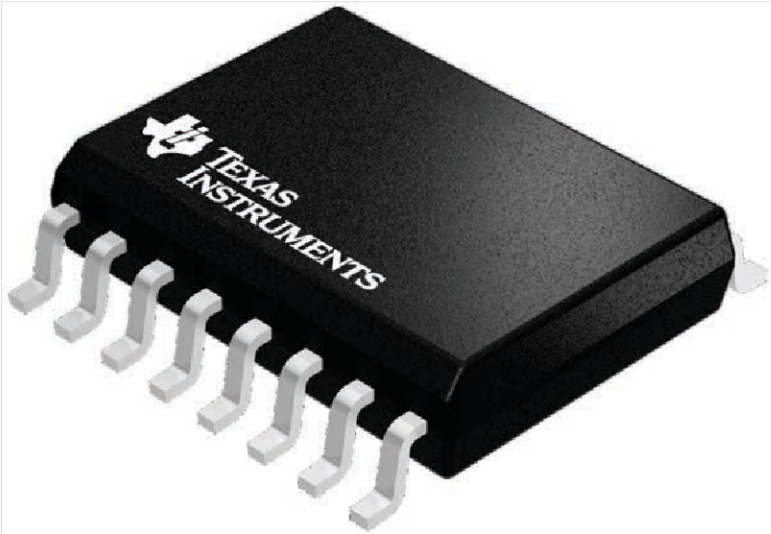
DW 16

SOIC - 2.65 mm max height

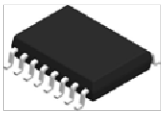
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

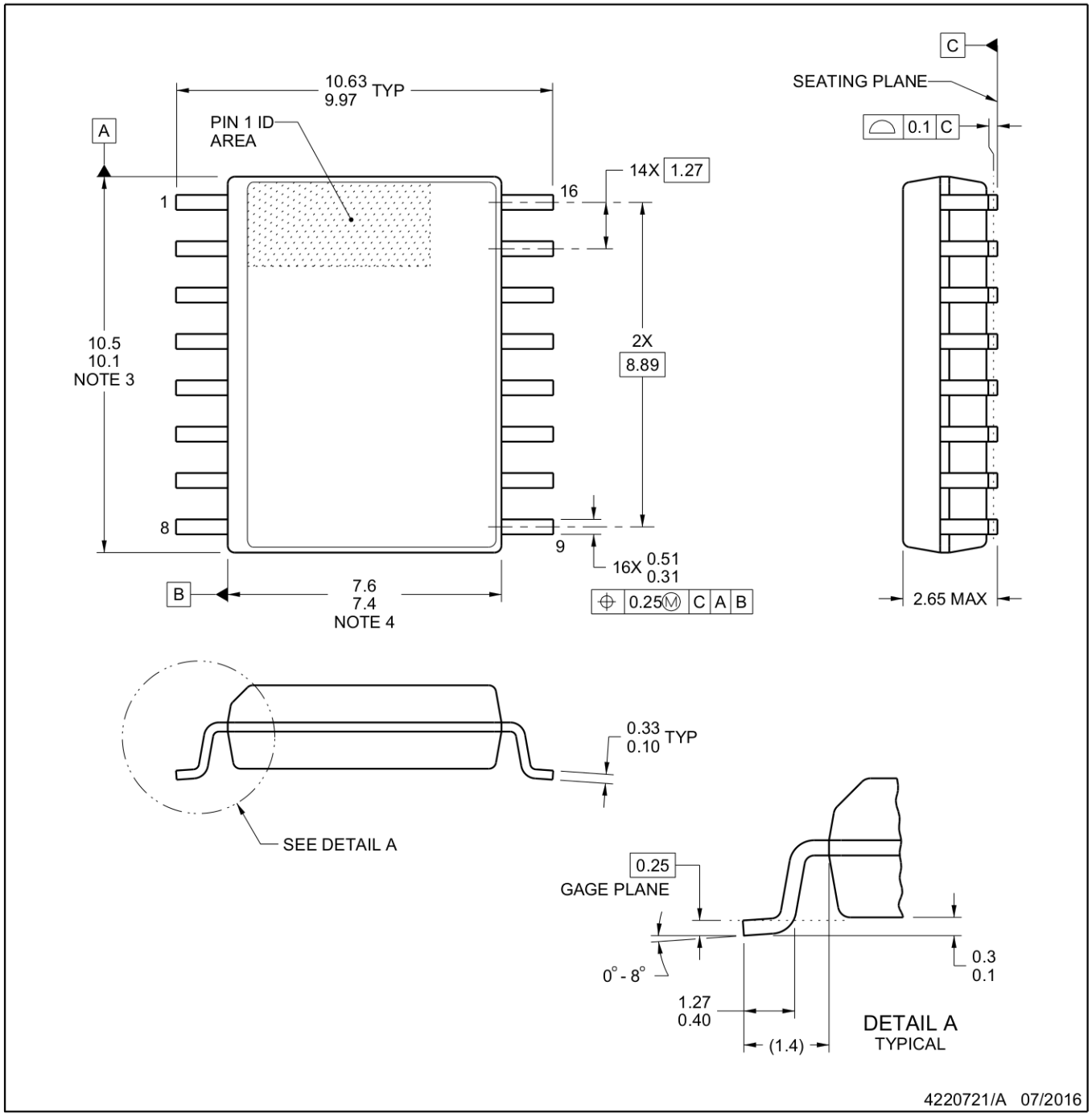


PACKAGE OUTLINE

DW0016A

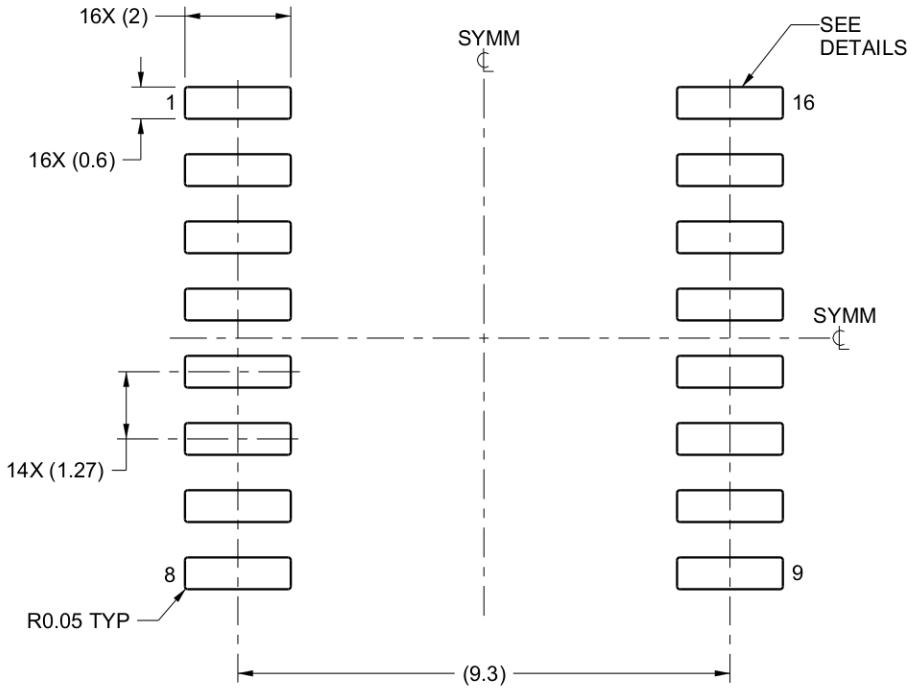
SOIC - 2.65 mm max height

SOIC

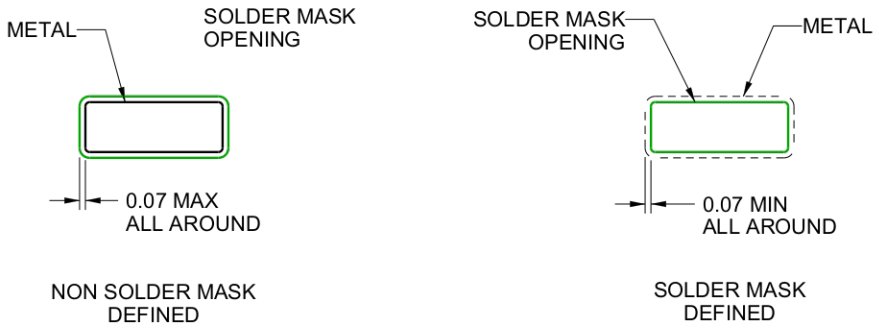


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

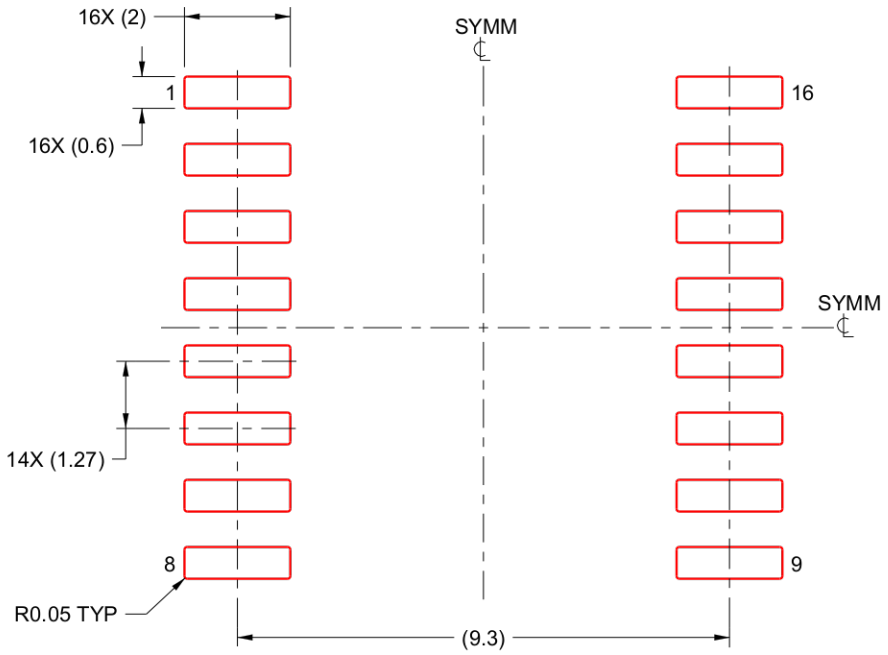


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

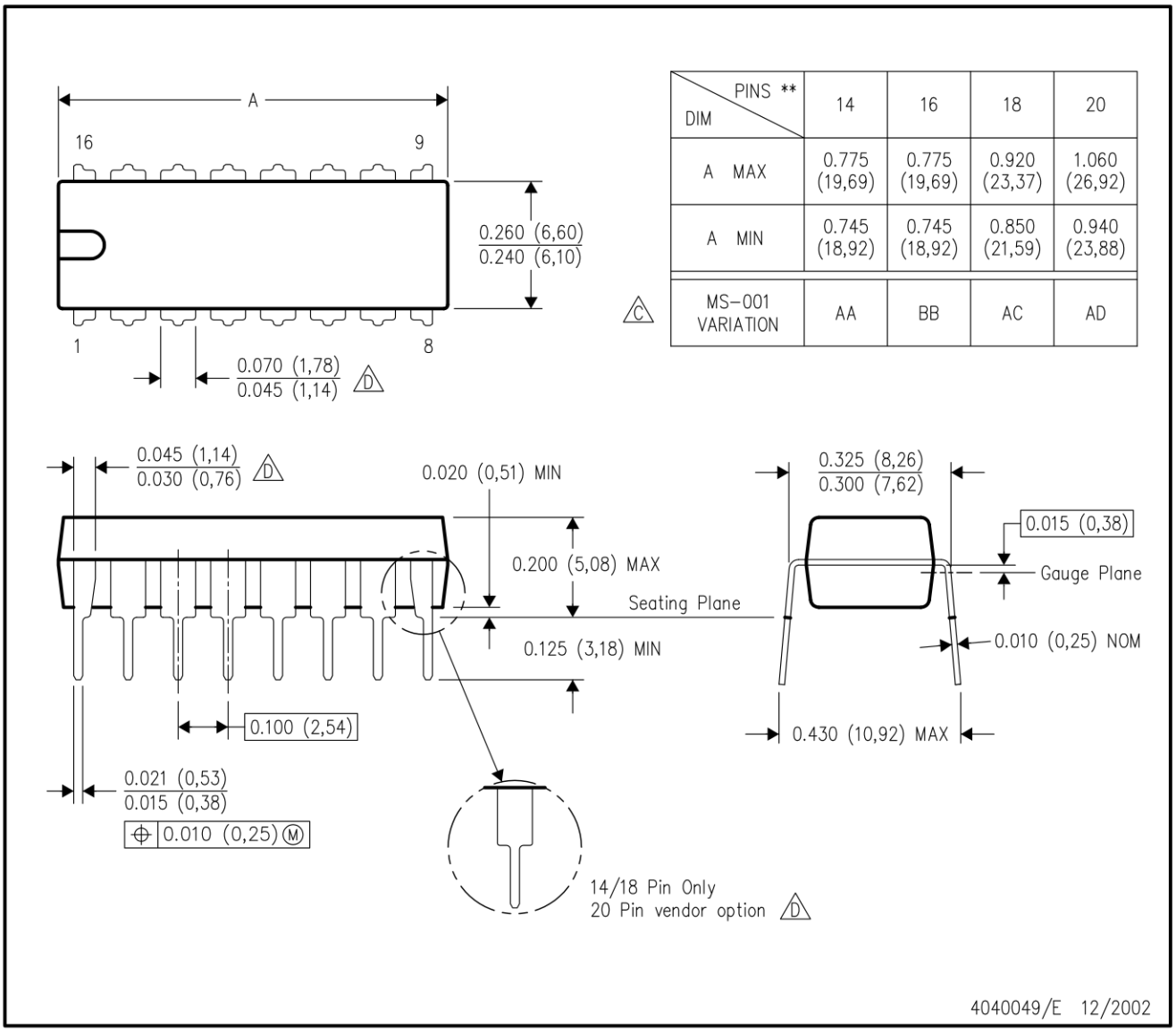
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION	AA	BB	AC	AD

4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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