ISO122 Precision Lowest-Cost Isolation Amplifier

1 Features

- 100% Tested for High-Voltage Breakdown
- Rated 1500 Vrms
- High IMR: 140 dB at 60 Hz
- Bipolar Operation: V_O = ±10 V
- 16-Pin Plastic DIP and 28-Lead SOIC
- Ease of Use: Fixed Unity Gain Configuration
- 0.020% Maximum Nonlinearity
- ±4.5-V to ±18-V Supply Range

2 Applications

- Industrial Process Control:
  - Transducer Isolator, Isolator for Thermocouples, RTDs, Pressure Bridges, and Flow Meters, 4-mA to 20-mA Loop Isolation
- Ground Loop Elimination
- Motor and SCR Control
- Power Monitoring
- PC-Based Data Acquisition
- Test Equipment

3 Description

The ISO122 is a precision isolation amplifier incorporating a novel duty cycle modulation-demodulation technique. The signal is transmitted digitally across a 2-pF differential capacitive barrier. With digital modulation the barrier characteristics do not affect signal integrity, thus resulting in excellent reliability and good high-frequency transient immunity across the barrier. Both barrier capacitors are imbedded in the plastic body of the package.

The ISO122 is easy to use. No external components are required for operation. The key specifications are 0.020% maximum nonlinearity, 50-kHz signal bandwidth, and 200-V/°C V_{OS} drift. A power supply range of 4.5 V to 18 V and quiescent currents of 5 mA on V_{S1} and ±5.5 mA on V_{S2} make the ISO122 ideal for a wide range of applications.

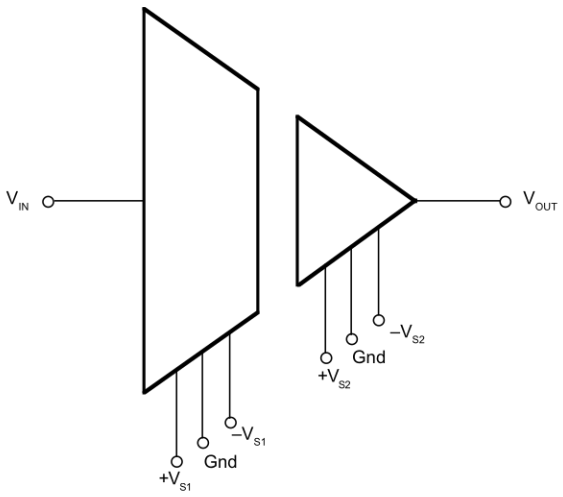
The ISO122 is available in 16-pin plastic DIP and 28-lead plastic surface-mount packages.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO122	PDIP (16)	17.90 mm × 7.50 mm
	SOIC (28)	20.01 mm × 6.61 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic



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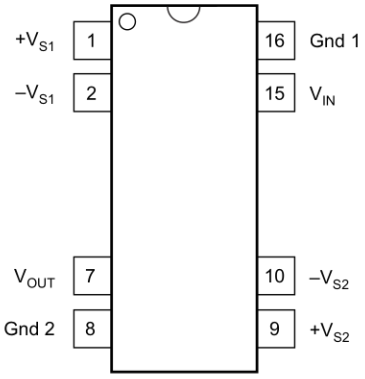
5 Revision History

Changes from Original (November1993) to Revision A **Page**

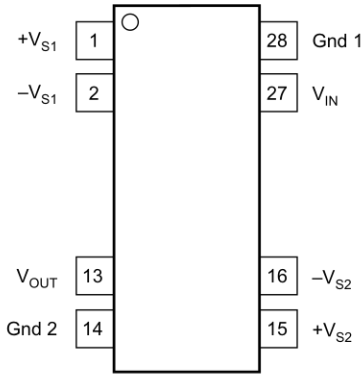
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

6 Pin Configuration and Functions

16 Pins PDIP
NVF Package
Top View



28 Pins SOIC
DVA Package
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	PDIP	SOIC		
GND	8	14	-	Low-side ground reference
GND	16	28	-	High-side ground reference
V_{IN}	15	27	I	High-side analog input
V_{OUT}	7	13	O	Low-side analog output
$+V_{S1}$	1	1	-	High-side positive analog supply
$-V_{S1}$	2	2	-	High-side negative analog supply
$+V_{S2}$	9	15	-	Low-side positive analog supply
$-V_{S2}$	10	16	-	Low-side negative analog supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Supply voltage		±18	V
V_{IN}		100	V
Continuous isolation voltage		1500	Vrms
Junction temperature		150	°C
Output short to common		Continuous	
Storage temperature, T_{stg}	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
TA	–25		85	°C
+VS1		15		
-VS1		–15		
+VS2		15		
-VS2		–15		
VIN		±10		

7.4 Thermal Information

THERMAL METRIC (1)		ISO122		UNIT
		NVF (PDIP)	DVA (SOIC)	
		16 PINS	28 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	51.0	79.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.4	32.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	29.5	42.2	
ψ_{JT}	Junction-to-top characterization parameter	10.4	6.6	
ψ_{JB}	Junction-to-board characterization parameter	29.0	40.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

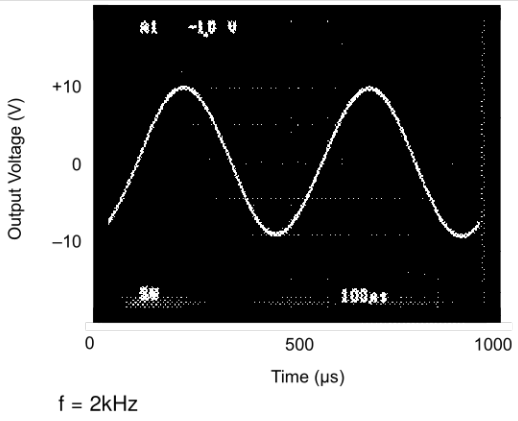
At T_A = +25°C , V_{S1} = V_{S2} = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ISO122P/U			ISO122JP/JU			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
ISOLATION									
	Voltage rated continuous ac 60Hz		1500			1500			Vac
	100% Test(1)	1s, 5pc PD	2400			2400			Vac
	Isolation Mode Rejection	60Hz		140			140		dB
	Barrier Impedance			10^{14} || 2			10^{14} || 2		Ω || pF
	Leakage Current at 60Hz	V_{ISO} = 240Vrms		0.18	0.5		0.18	0.5	µArms
GAIN									
	Nominal Gain	V_O = ±10V		1			1		V/V
	Gain Error			±0.05	±0.50		±0.05	±0.50	%FSR
	Gain vs Temperature			±10			±10		ppm/°C
	Nonlinearity(2)			±0.016	±0.020		±0.025	±0.050	%FSR
INPUT OFFSET VOLTAGE									
	Initial Offset			±20	±50		±20	±50	mV
	vs Temperature			±200			±200		µV/°C
	vs Supply			±2			±2		mV/V
	Noise			4					µV/√Hz
INPUT									
	Voltage Range		±10	±12.5		±10	±12.5		V
	Resistance			200			200		kΩ
OUTPUT									
	Voltage Range		±10	±12.5		±10	±12.5		V
	Current Drive		±5	±15		±5	±15		mA
	Capacitive Load Drive			0.1			0.1		µF
	Ripple Voltage(3)			20			20		mVp-p
FREQUENCY RESPONSE									
	Small-Signal Bandwidth			50			50		kHz
	Slew Rate			2			2		V/µs
	Settling Time 0.10%	V_O = ±10V		50			50		µs
	Settling Time 0.01%			350			350		µs
	Overload Recovery Time			150			150		µs
POWER SUPPLIES									
	Rated Voltage			±15			±15		V
	Voltage Range		±4.5		±18	±4.5		±18	V
V_{S1}	Quiescent Current			±5	±7		±5	±7	mA
V_{S2}				±5.5	±7		±5.5	±7	
TEMPERATURE RANGE									
	Specification		–25		85	–25		85	°C
	Operating		–25		85	–25		85	°C
	Storage		–40		125	–40		125	°C
θ_{JA}	Thermal Resistance			100			100		°C/W
θ_{JC}				65			65		°C/W

(1) Tested at 1.6 X rated, fail on 5pC partial discharge.
(2) Nonlinearity is the peak deviation of the output voltage from the best-fit straight line. It is expressed as the ratio of deviation to FSR.
(3) Ripple frequency is at carrier frequency (500kHz).

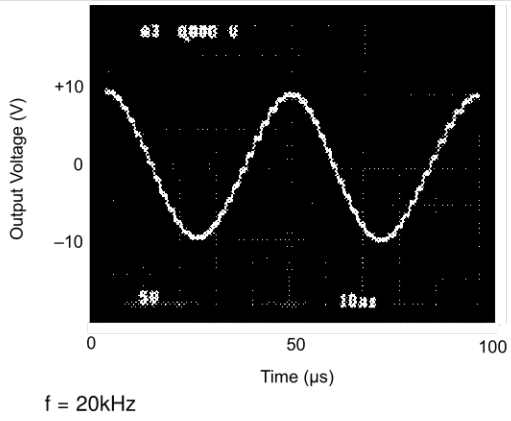
7.6 Typical Characteristics

At T_A = +25°C, and V_S = ±15 V, unless otherwise noted.



f = 2kHz

Figure 1. Sine Response



f = 20kHz

Figure 2. Sine Response

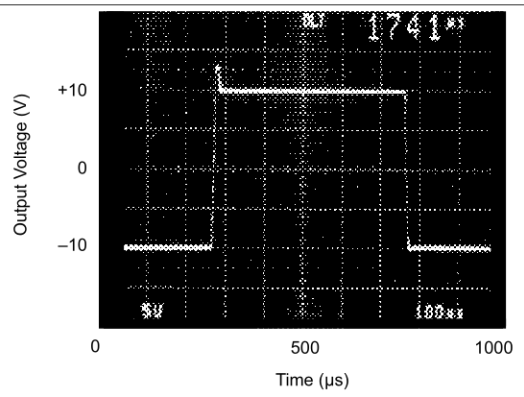


Figure 3. Step Response

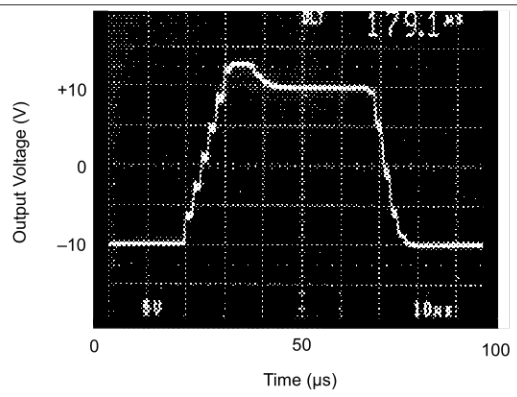


Figure 4. Step Response

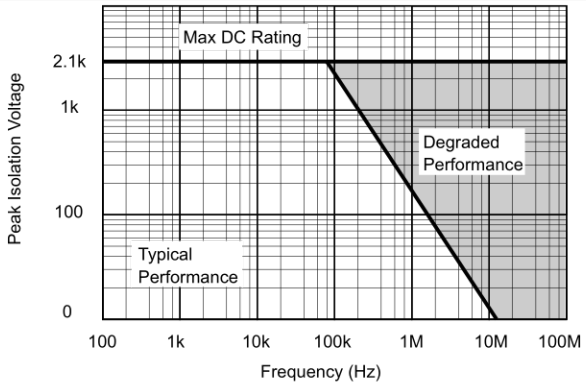


Figure 5. Isolation Voltage vs Frequency

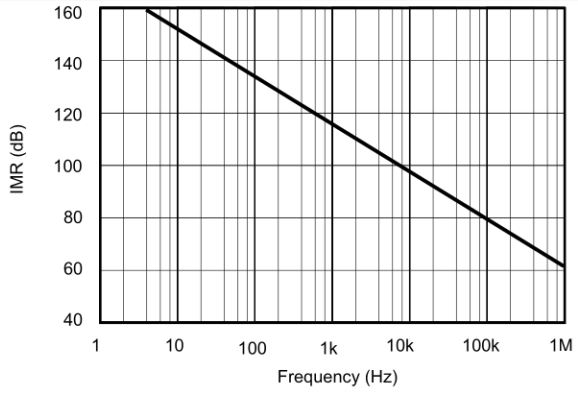


Figure 6. IMR vs Frequency

Typical Characteristics (continued)

At T_A = +25°C, and V_S = ±15 V, unless otherwise noted.

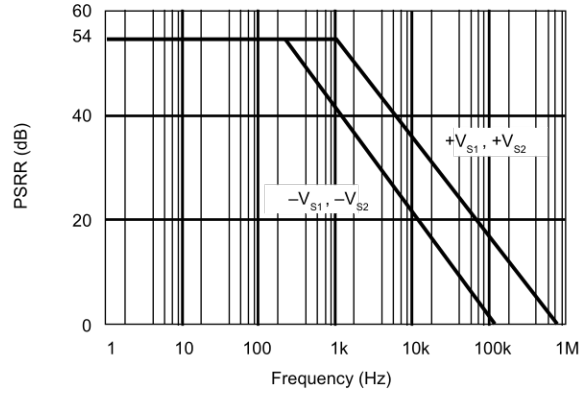


Figure 7. PSRR vs Frequency

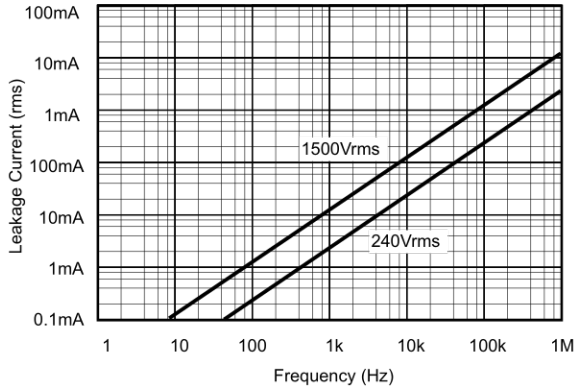
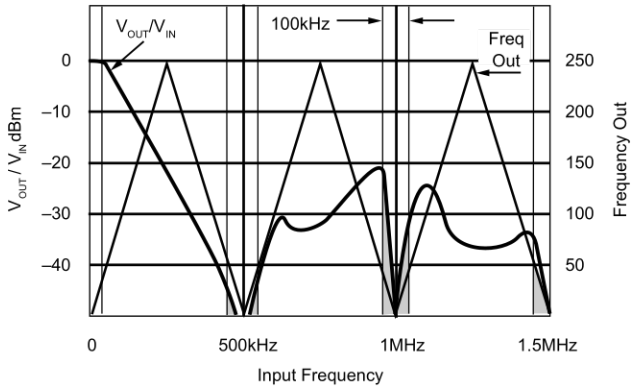


Figure 8. Isolation Leakage Current vs Frequency



NOTE: Shaded area shows aliasing frequencies that cannot be removed by a low-pass filter at the output.

Figure 9. Signal Response to Inputs Greater than 250 kHz

8 Detailed Description

8.1 Overview

The ISO122 isolation amplifier uses an input and an output section galvanically isolated by matched 1-pF isolating capacitors built into the plastic package. The input is duty-cycle modulated and transmitted digitally across the barrier. The output section receives the modulated signal, converts it back to an analog voltage and removes the ripple component inherent in the demodulation. Input and output sections are fabricated, then laser trimmed for exceptional circuitry matching common to the input and output sections. The sections are then mounted on opposite ends of the package with the isolating capacitors mounted between the two sections. The ISO122 contains 250 transistors.

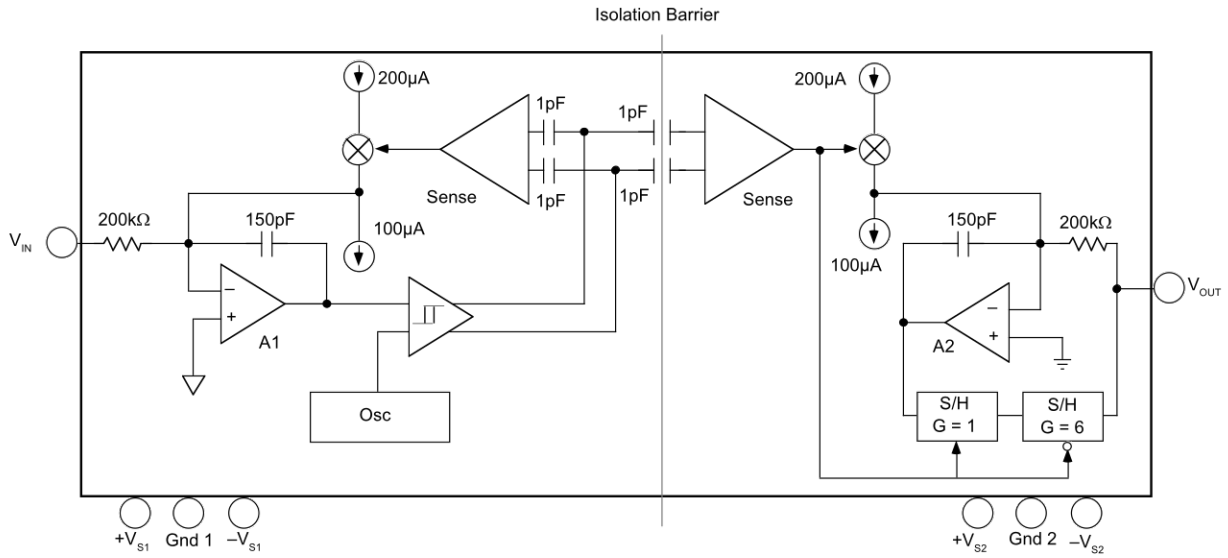
8.1.1 Modulator

An input amplifier (A1, *Functional Block Diagram*) integrates the difference between the input current (V_{IN}/200 kΩ) and a switched ±100-mA current source. This current source is implemented by a switchable 200-mA source and a fixed 100-µA current sink. To understand the basic operation of the modulator, assume that V_{IN} = 0 V. The integrator will ramp in one direction until the comparator threshold is exceeded. The comparator and sense amp will force the current source to switch; the resultant signal is a triangular waveform with a 50% duty cycle. The internal oscillator forces the current source to switch at 500 kHz. The resultant capacitor drive is a complementary duty-cycle modulation square wave.

8.1.2 Demodulator

The sense amplifier detects the signal transitions across the capacitive barrier and drives a switched current source into integrator A2. The output stage balances the duty-cycle modulated current against the feedback current through the 200 kW feedback resistor, resulting in an average value at the V_{OUT} pin equal to V_{IN}. The sample and hold amplifiers in the output feedback loop serve to remove undesired ripple voltages inherent in the demodulation process.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Isolation Amplifier

The ISO122 is a precision analog isolation amplifier. The input signal is transmitted digitally across a high-voltage differential capacitive barrier. With digital modulation the barrier characteristics do affect signal integrity, resulting in excellent reliability and high-frequency transient immunity.

8.4 Device Functional Modes

The ISO122 does not have any additional functional modes.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Carrier Frequency Considerations

The ISO122 amplifier transmits the signal across the isolation barrier by a 500kHz duty cycle modulation technique. For input signals having frequencies below 250 kHz, this system works like any linear amplifier. But for frequencies above 250 kHz, the behavior is similar to that of a sampling amplifier. The signal response to inputs greater than 250 kHz performance curve shows this behavior graphically; at input frequencies above 250 kHz the device generates an output signal component of reduced magnitude at a frequency below 250 kHz. This is the aliasing effect of sampling at frequencies less than two times the signal frequency (the Nyquist frequency). At the carrier frequency and its harmonics, both the frequency and amplitude of the aliasing go to zero.

9.1.2 Isolation Mode Voltage Induced Errors

IMV can induce errors at the output as indicated by the plots of IMV vs Frequency. It should be noted that if the IMV frequency exceeds 250 kHz, the output also will display spurious outputs (aliasing), in a manner similar to that for V_{IN} > 250 kHz and the amplifier response will be identical to that shown in the Signal Response to Inputs Greater Than 250-kHz performance curve. This occurs because IMV-induced errors behave like input-referred error signals. To predict the total error, divide the isolation voltage by the IMR shown in the IMR vs Frequency curve and compute the amplifier response to this input-referred error signal from the data given in the Signal Response to Inputs Greater than 250-kHz performance curve. For example, if a 800-kHz 1000-Vrms IMR is present, then a total of [(–60 dB) + (–30 dB)] x (1000 V) = 32-mV error signal at 200 kHz plus a 1 V, 800-kHz error signal will be present at the output.

9.1.3 High IMV dV/dt Errors

As the IMV frequency increases and the dV/dt exceeds 1000 Vμs, the sense amp may start to false trigger, and the output will display spurious errors. The common-mode current being sent across the barrier by the high slew rate is the cause of the false triggering of the sense amplifier. Lowering the power-supply voltages below ±15 V may decrease the dV/dt to 500 V/μs for typical performance.

9.1.4 High Voltage Testing

Texas Instruments has adopted a partial discharge test criterion that conforms to the German VDE0884 Optocoupler Standards. This method requires the measurement of minute current pulses (< 5 pC) while applying 2400-Vrms, 60-Hz high-voltage stress across every ISO122 isolation barrier. No partial discharge may be initiated to pass this test. This criterion confirms transient overvoltage (1.6 × 1500 Vrms) protection without damage to the ISO122. Lifetest results verify the absence of failure under continuous rated voltage and maximum temperature.

This new test method represents the "state of the art" for nondestructive high–voltage reliability testing. It is based on the effects of nonuniform fields that exist in heterogeneous dielectric material during barrier degradation. In the case of void nonuniformities, electric field stress begins to ionize the void region before bridging the entire high-voltage barrier. The transient conduction of charge during and after the ionization can be detected externally as a burst of 0.01–0.1 ms current pulses that repeat on each AC voltage cycle. The minimum AC barrier voltage that initiates partial discharge is defined as the "inception voltage." Decreasing the barrier voltage to a lower level is required before partial discharge ceases and is defined as the "extinction voltage." The

Application Information (continued)

package insulation processes have been characterized and developed to yield an inception voltage in excess of 2400 Vrms so that transient overvoltages below this level will not damage the ISO122. The extinction voltage is above 1500 Vrms so that even overvoltage induced partial discharge will cease once the barrier voltage is reduced to the 1500 Vrms (rated) level. Older high-voltage test methods relied on applying a large enough overvoltage (above rating) to break down marginal parts, but not so high as to damage good ones. Our new partial discharge testing gives us more confidence in barrier reliability than breakdown/no breakdown criteria.

9.2 Typical Application

9.2.1 Output Filter

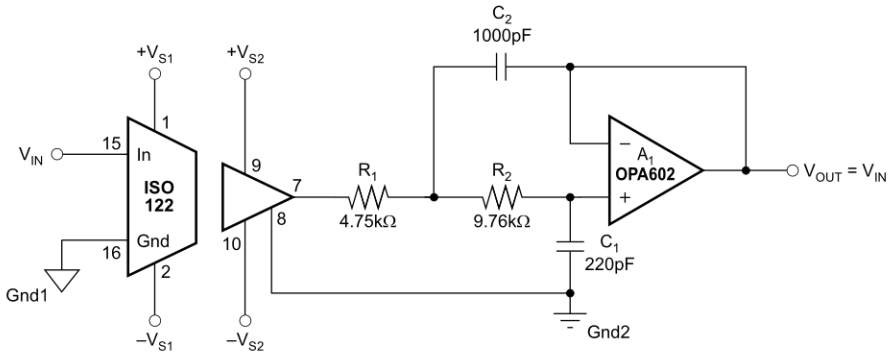


Figure 10. ISO122 With Output Filter for Improved Ripple

9.2.1.1 Design Requirements

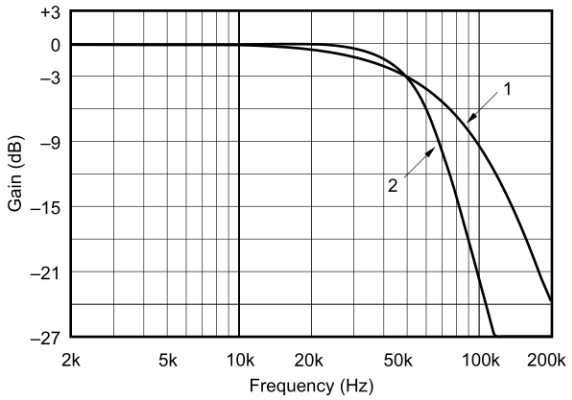
The ISO122 isolation amplifiers (ISO amps) have a small (10 to 20 mVp-p typical) residual demodulator ripple at the output. A simple filter can be added to eliminate the output ripple without decreasing the 50-kHz signal bandwidth of the ISO amp.

9.2.1.2 Detailed Design Procedure

The ISO122 is designed to have a 50-kHz single-pole (Butterworth) signal response. By cascading the ISO amp with a simple 50-kHz, Q = 1, two-pole, low-pass filter, the overall signal response becomes three-pole Butterworth. The result is a maximally flat 50-kHz magnitude response and the output ripple reduced below the noise level. Figure 10 shows the complete circuit. The two-pole filter is a unity-gain Sallen-Key type consisting of A1, R1, R2, C1, and C2. The values shown give Q = 1 and f–3-dB bandwidth = 50 kHz. Because the op amp is connected as a unity-gain follower, gain and gain accuracy of the ISO amp are unaffected. Using a precision op amp such as the OPA602 also preserves the DC accuracy of the ISO amp.

Typical Application (continued)

9.2.1.3 Application Curves



1) Standard ISO122 has 50kHz single-pole (Butterworth) response.

2) ISO122 with cascaded 50kHz, Q = 1, two-pole, low-pass filter has three-pole Butterworth response.

Figure 11. Gain vs. Frequency

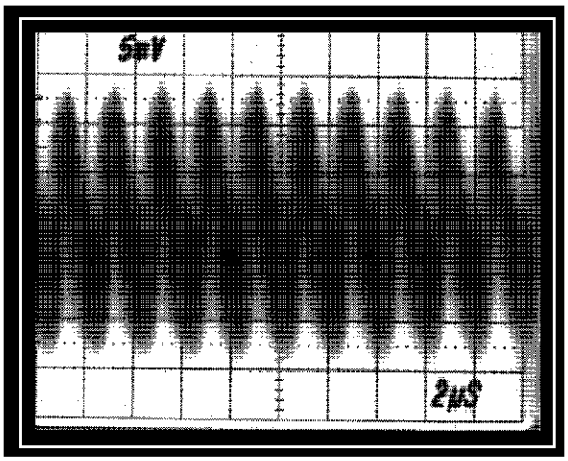


Figure 12. Standard ISO122 (Approximately 20-mVp-p Output Ripple)

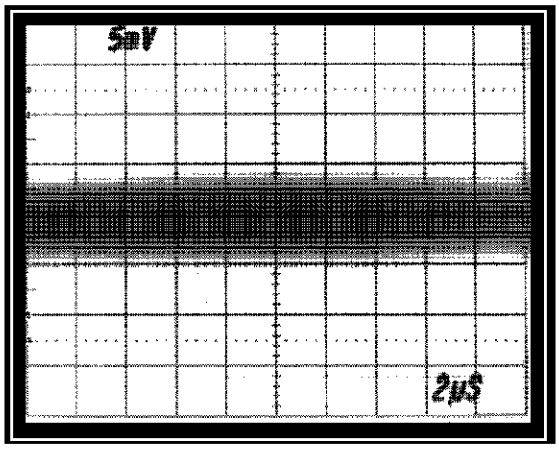


Figure 13. Filtered ISO122 (No Visible Output Ripple)

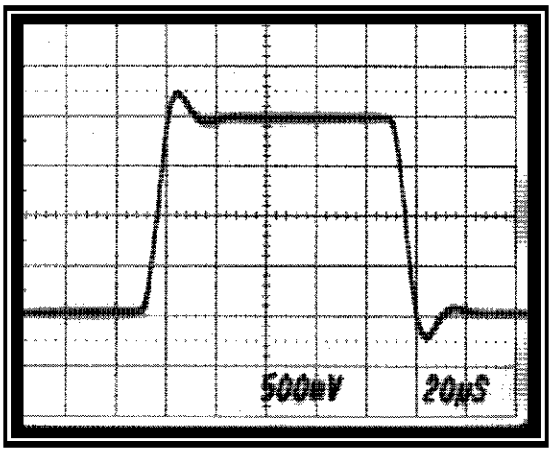


Figure 14. Step Response of Standard ISO122

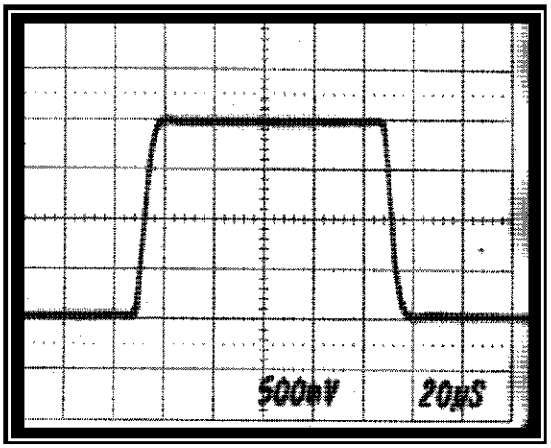


Figure 15. Step Response of ISO122 With Added Twopole Output Filter

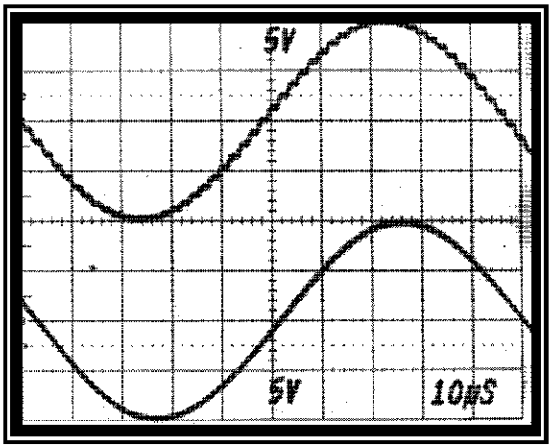


Figure 16. Large-signal, 10 kHz Sine-wave Response of ISO122 With and Without Output Filter

Typical Application (continued)

9.2.2 Battery Monitor

Figure 17 provides a means to monitor the cell voltage on a 600-V battery stack by using the battery as a power source for the isolated voltage.

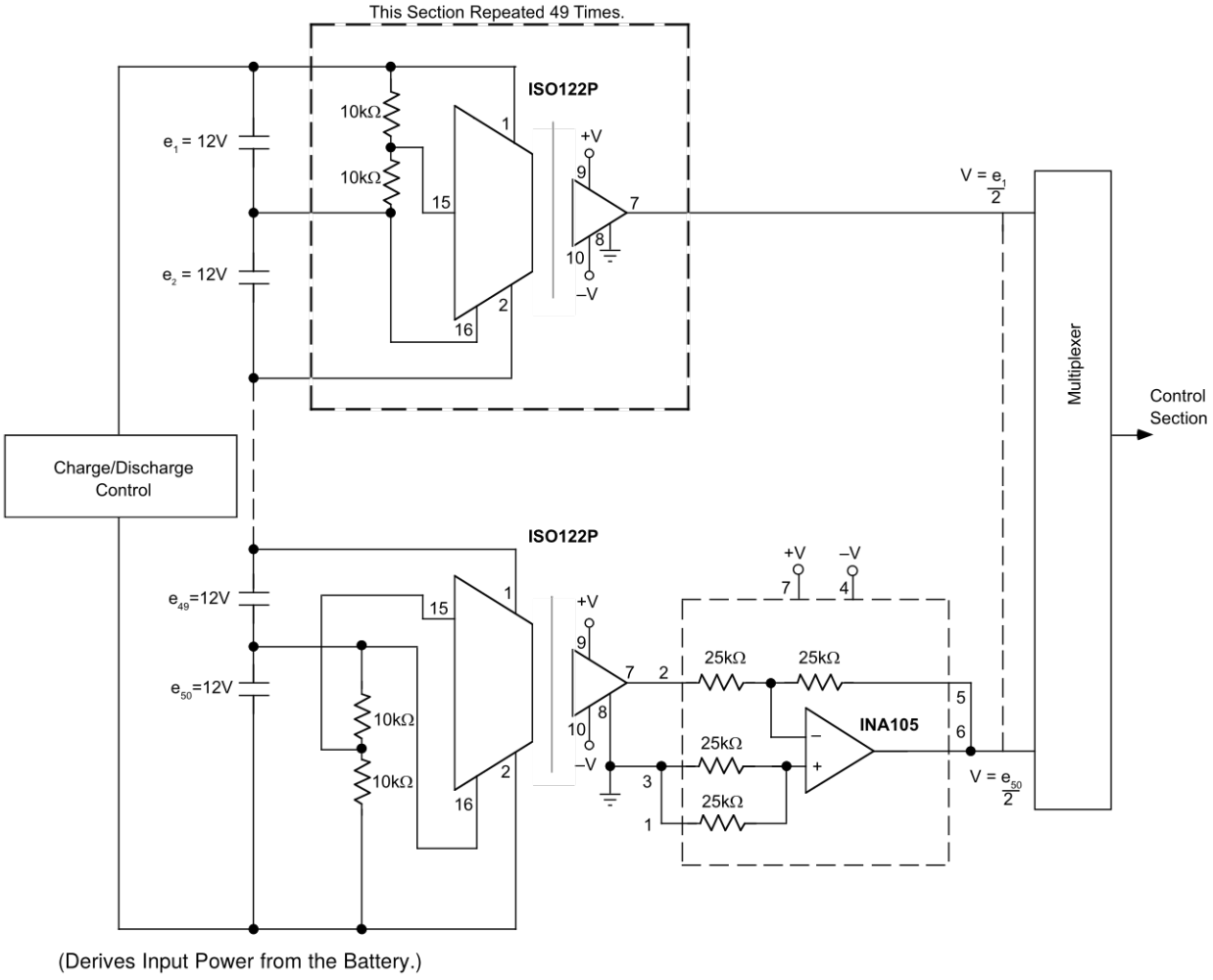


Figure 17. Battery Monitor for a 600-V Battery Power System

Typical Application (continued)

9.2.3 Programmable Gain Amplifier

In applications where variable gain configurations are required, a programmable gain amplifier like the PGA102 can be used with the ISO122. Figure 18 uses an ISO150 to provide gain pin selection options to the PGA102.

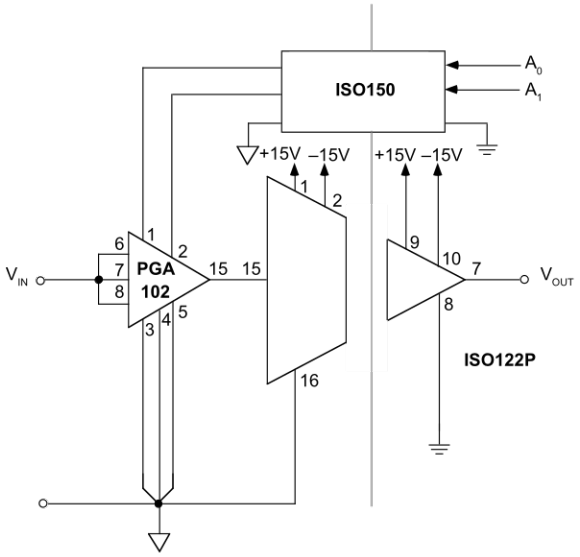
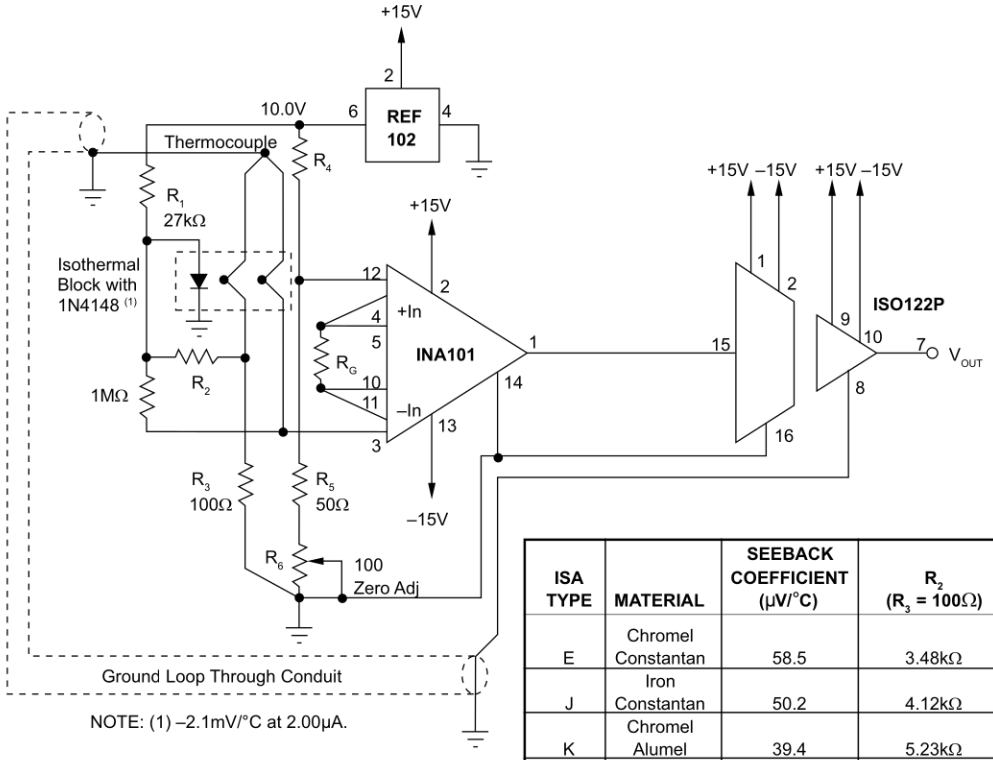


Figure 18. Programmable-Gain Isolation Channel With Gains of 1, 10, and 100

Typical Application (continued)

9.2.4 Thermocouple Amplifier

For isolated temperature measurements, Figure 19 provides an application solution using the INA101 feeding the input stage of the ISO122. The table provides suggested resistor values based on the type of thermistor used in the application.



ISA TYPE	MATERIAL	SEEBACK COEFFICIENT (µV/°C)	R_2 (R_3 = 100Ω)	R_4 (R_5 + R_6 = 100Ω)
E	Chromel Constantan	58.5	3.48kΩ	56.2kΩ
J	Iron Constantan	50.2	4.12kΩ	64.9kΩ
K	Chromel Alumel	39.4	5.23kΩ	80.6kΩ
T	Copper Constantan	38.0	5.49kΩ	84.5kΩ

Figure 19. Thermocouple Amplifier With Ground Loop Elimination, Cold Junction Compensation, and Up-scale Burn-out.

Typical Application (continued)

9.2.5 Isolated 4- to 20-mA Instrument Loop

For isolated temperature measurements in a 4- to 20-mA loop, Figure 20 provides a solution using the XTR101 and RCV420. A high-performance PT100 resistance temperature detector (RTD) provides the user with an isolated 0- to 5-V representation of the isolated temperature measurement.

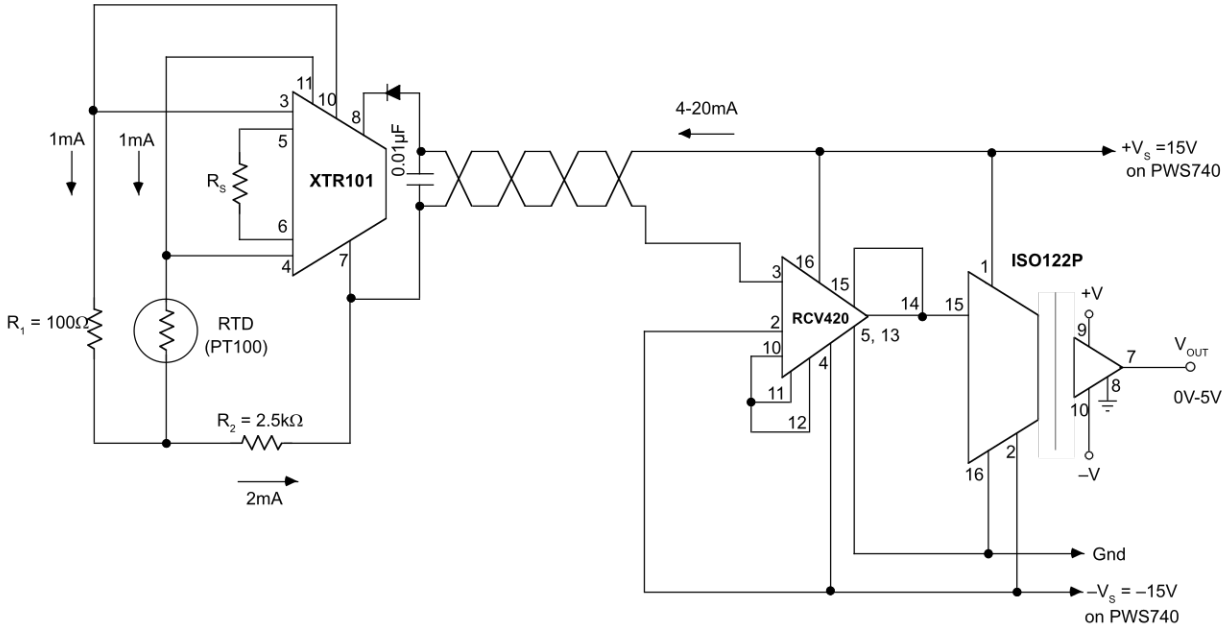
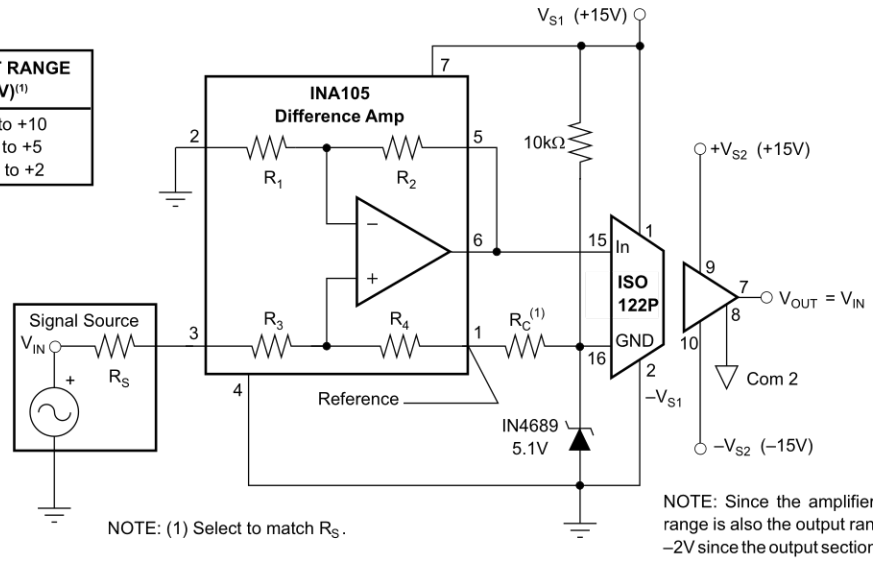


Figure 20. Isolated 4- to 200-mA Instrument Loop. (RTD shown.)

9.2.6 Single-Supply Operation of the ISO122P Isolation Amplifier

The circuit shown in Figure 21 uses a 5.1-V Zener diode to generate the negative supply for an ISO122 from a single supply on the high-voltage side of the isolation amplifier. The input measuring range will be dependent on the applied voltage as noted in the accompanying table.

V_S (V)	INPUT RANGE (V)(1)
20+	–2 to +10
15	–2 to +5
12	–2 to +2



NOTE: (1) Select to match R_S.

NOTE: Since the amplifier is unity gain, the input range is also the output range. The output can go to –2V since the output section of the ISO amp operates from dual supplies.

For additional information see SBOA004.

Figure 21. Single-Supply Operation of the ISO122P Isolation Amplifier

Typical Application (continued)

9.2.7 Input-Side Powered ISO Amp

The user side of the ISO122 can be powered from the high-voltage side using an isolated DC-DC converter as shown in Figure 22.

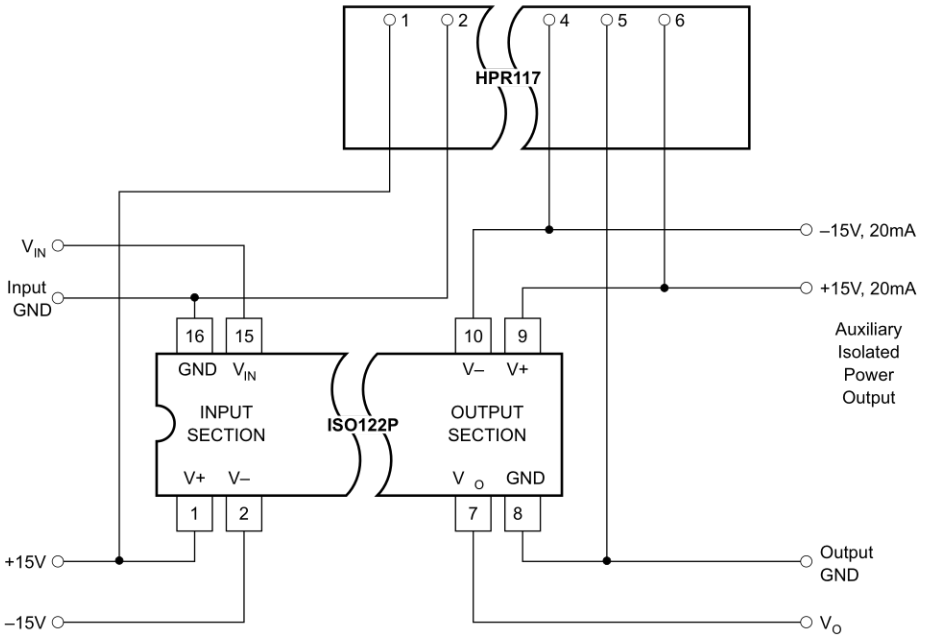


Figure 22. Input-Side Powered ISO Amp

9.2.8 Powered ISO Amp With Three-Port Isolation

Figure 23 shows an application solution that provides isolated power to both the user and high-voltage sides of the ISO122 amplifier.

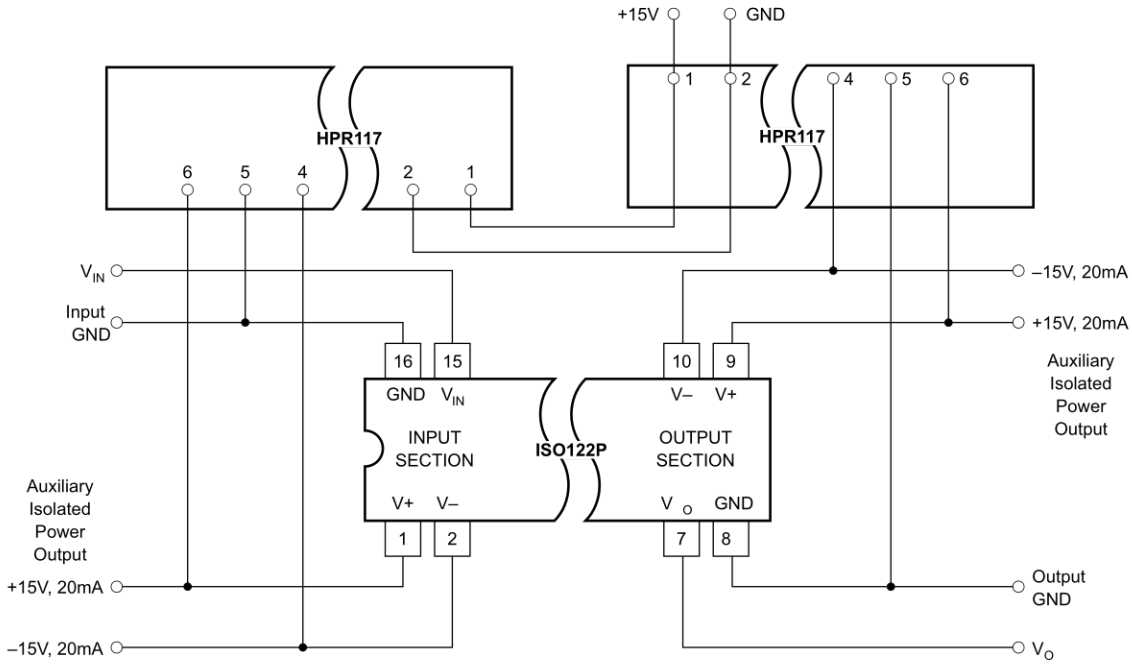


Figure 23. Powered ISO Amp With Three-Port Isolation

10 Power Supply Recommendations

10.1 Signal and Supply Connections

Each power-supply pin should be bypassed with 1-µF tantalum capacitors located as close to the amplifier as possible. The internal frequency of the modulator/demodulator is set at 500 kHz by an internal oscillator. Therefore, if it is desired to minimize any feedthrough noise (beat frequencies) from a DC-DC converter, use a π filter on the supplies (see Figure 24). The ISO122 output has a 500-kHz ripple of 20 mV, which can be removed with a simple 2-pole low-pass filter with a 100-kHz cutoff using a low-cost op amp (see Figure 10).

The input to the modulator is a current (set by the 200-kΩ integrator input resistor) that makes it possible to have an input voltage greater than the input supplies, as long as the output supply is at least ±15 V. It is therefore possible, when using an unregulated DC-DC converter, to minimize PSR related output errors with ±5-V voltage regulators on the isolated side and still get the full ±10V input and output swing.

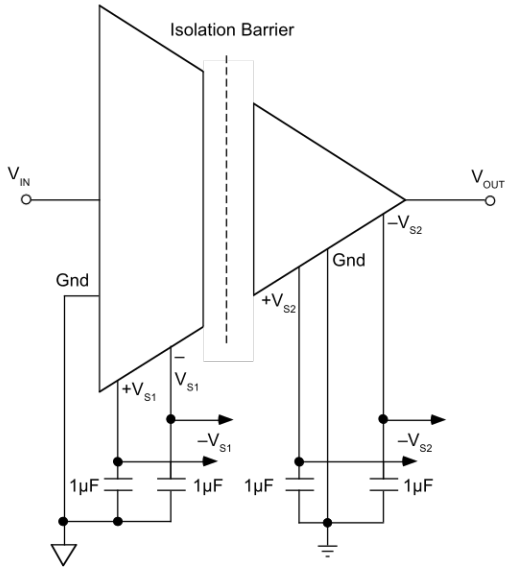


Figure 24. Basic Signal and Power Connections

11 Layout

11.1 Layout Guidelines

To maintain the isolation barrier of the device, the distance between the high-side ground (pin 16 or 28) and the low-side ground (pin 8 or 14) should be kept at maximum; that is, the entire area underneath the device should be kept free of any conducting materials.

11.2 Layout Example

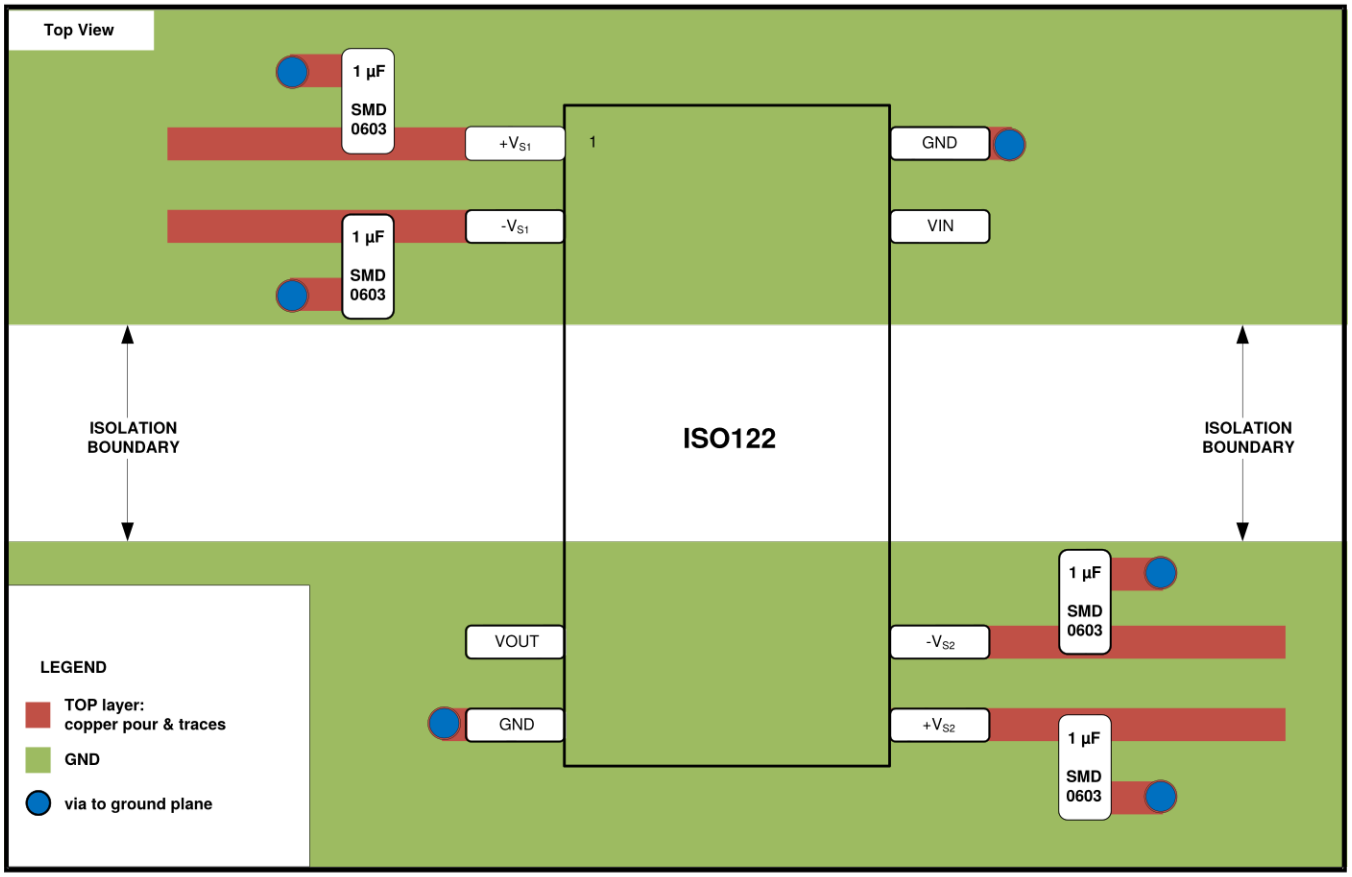


Figure 25. Typical Layout

12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO122JP	ACTIVE	PDIP	NVF	8	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-25 to 85	ISO122JP	Samples
ISO122JPE4	ACTIVE	PDIP	NVF	8	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-25 to 85	ISO122JP	Samples
ISO122JU	ACTIVE	SOIC	DVA	8	20	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-25 to 85	ISO 122JU	Samples
ISO122JU/1K	ACTIVE	SOIC	DVA	8	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-25 to 85	ISO 122JU	Samples
ISO122JUE4	ACTIVE	SOIC	DVA	8	20	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-25 to 85	ISO 122JU	Samples
ISO122P	ACTIVE	PDIP	NVF	8	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-25 to 85	ISO122P	Samples
ISO122PE4	ACTIVE	PDIP	NVF	8	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-25 to 85	ISO122P	Samples
ISO122U	ACTIVE	SOIC	DVA	8	20	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-25 to 85	ISO 122U	Samples
ISO122U/1K	ACTIVE	SOIC	DVA	8	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-25 to 85	ISO 122U	Samples
ISO122UE4	ACTIVE	SOIC	DVA	8	20	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-25 to 85	ISO 122U	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

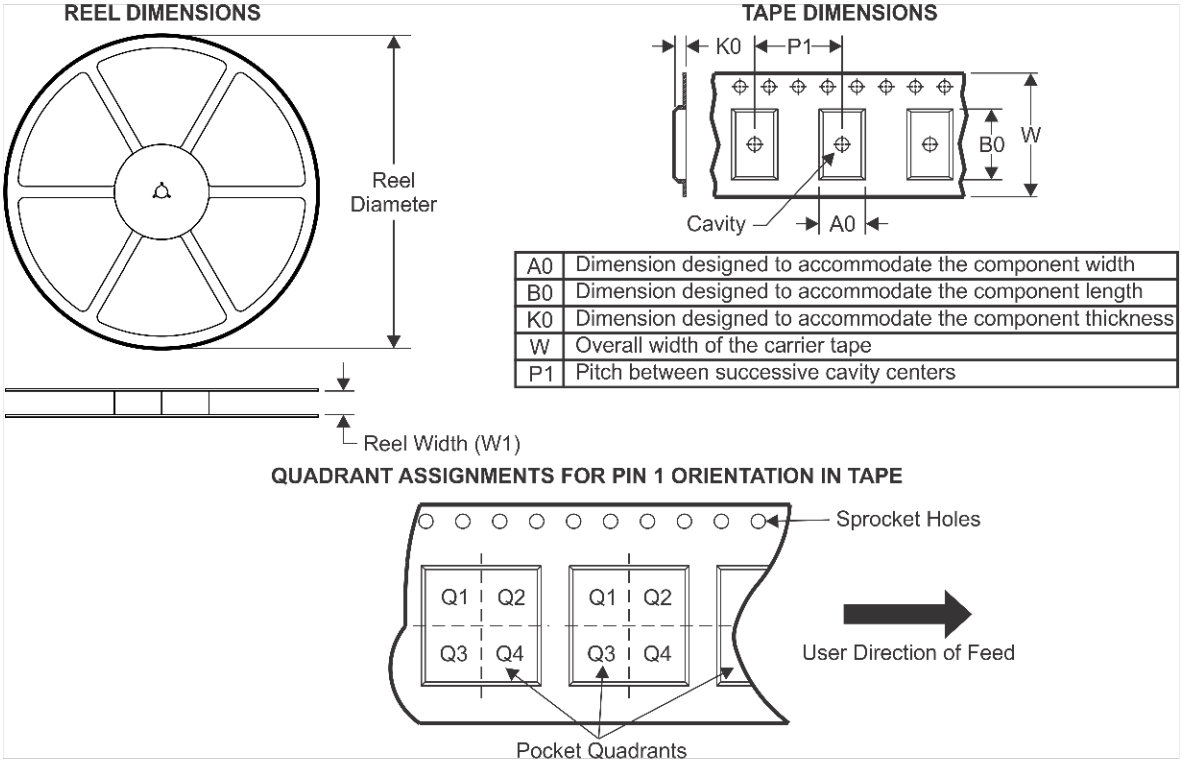
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

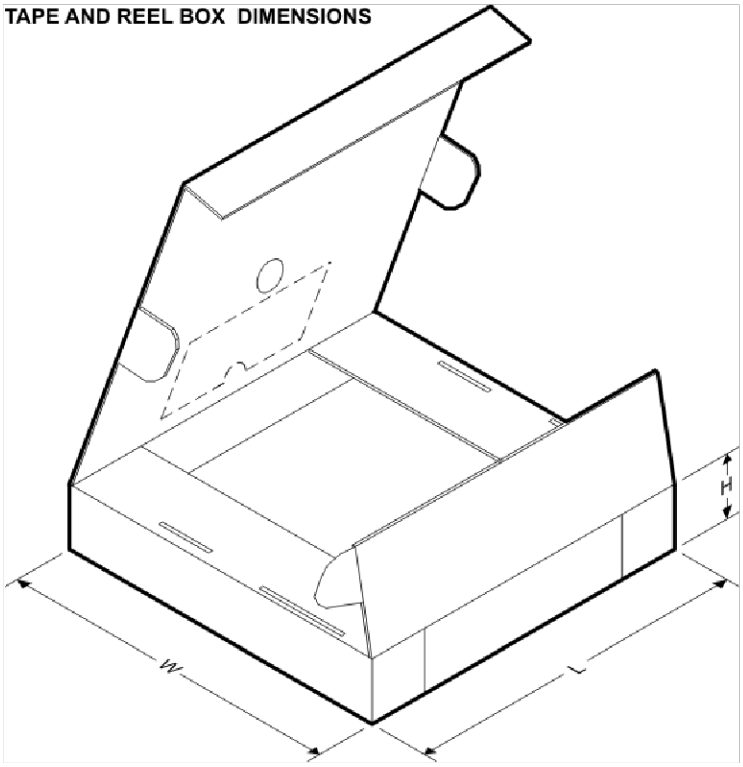


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO122JU/1K	SOIC	DVA	8	1000	330.0	24.4	10.9	18.3	3.2	12.0	24.0	Q1
ISO122U/1K	SOIC	DVA	8	1000	330.0	24.4	10.9	18.3	3.2	12.0	24.0	Q1

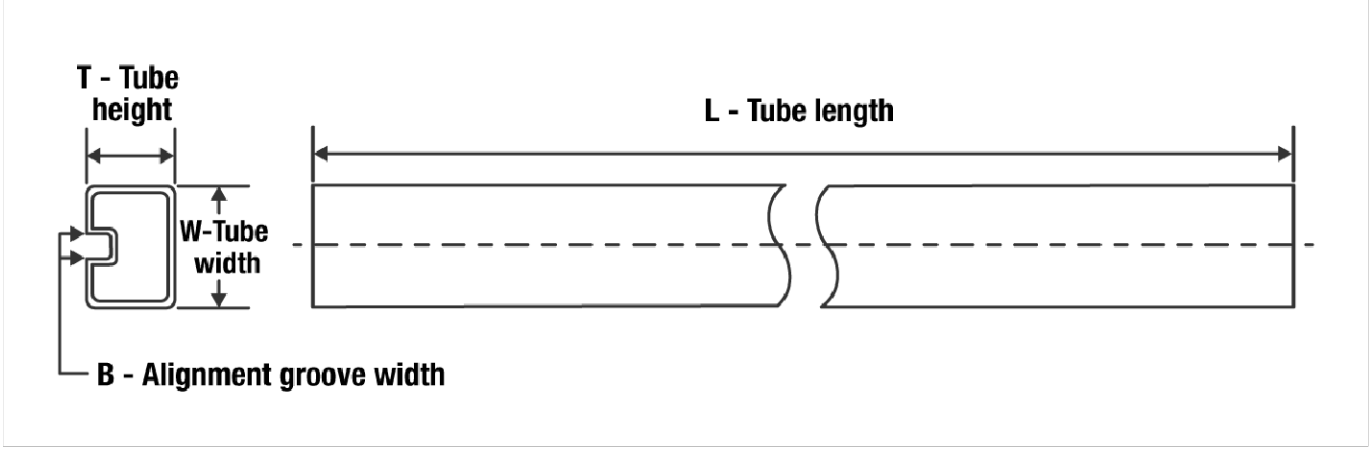
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO122JU/1K	SOIC	DVA	8	1000	367.0	367.0	45.0
ISO122U/1K	SOIC	DVA	8	1000	367.0	367.0	45.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISO122JP	NVF	PDIP	8	25	506	13.97	11230	4.32
ISO122JPE4	NVF	PDIP	8	25	506	13.97	11230	4.32
ISO122JU	DVA	SOIC	8	20	507	12.83	5080	6.6
ISO122JUE4	DVA	SOIC	8	20	507	12.83	5080	6.6
ISO122P	NVF	PDIP	8	25	506	13.97	11230	4.32
ISO122PE4	NVF	PDIP	8	25	506	13.97	11230	4.32
ISO122U	DVA	SOIC	8	20	507	12.83	5080	6.6
ISO122UE4	DVA	SOIC	8	20	507	12.83	5080	6.6

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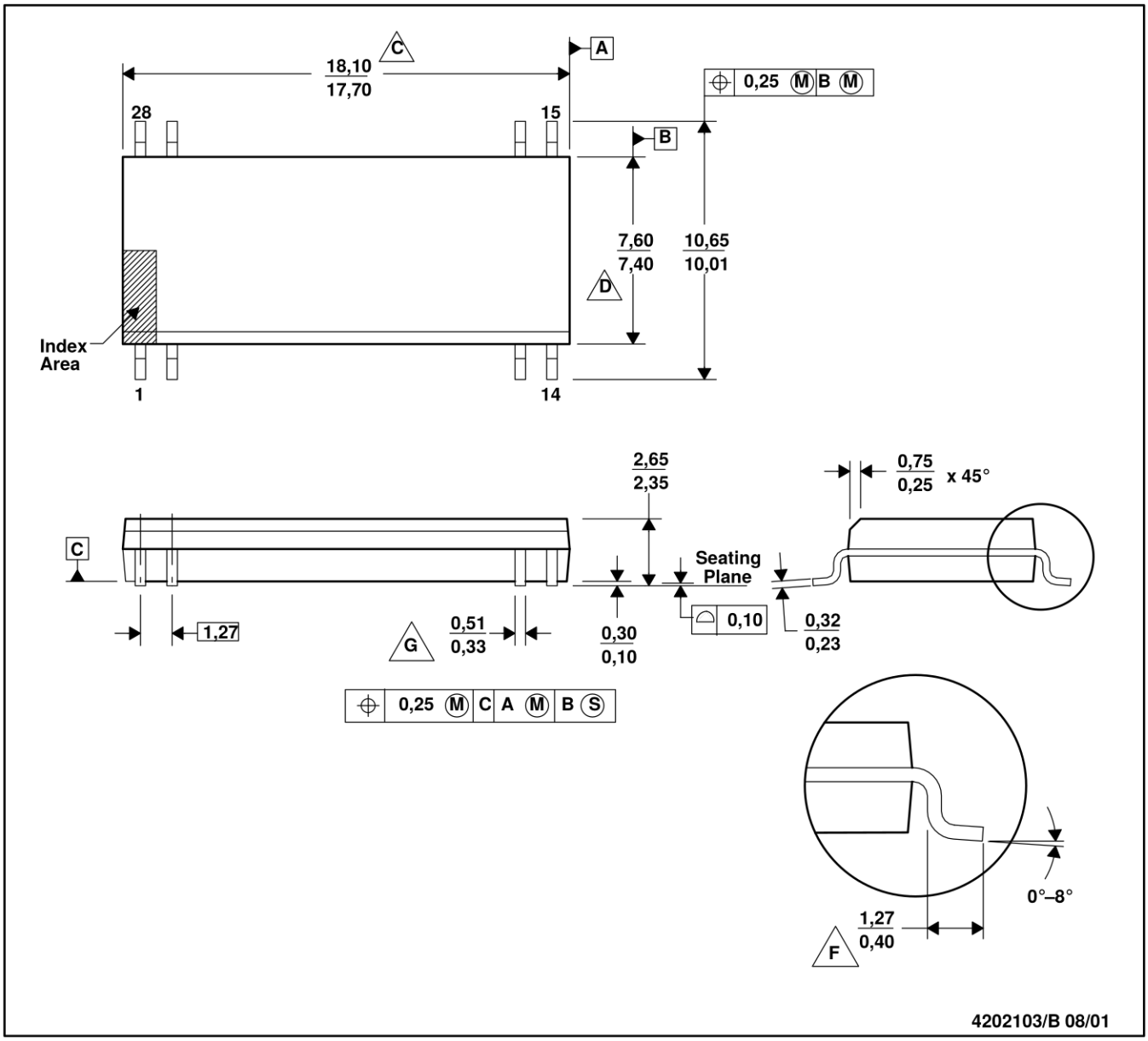
DVA (R-PDSO-G8/28) **PLASTIC SMALL-OUTLINE**



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, and gate burrs shall not exceed 0,15 mm per side.
D. Body width dimension does not include inter-lead flash or portrusions. Inter-lead flash and protrusions shall not exceed 0,25 mm per side.
E. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area.
F. Lead dimension is the length of terminal for soldering to a substrate.
G. Lead width, as measured 0,36 mm or greater above the seating plane, shall not exceed a maximum value of 0,61 mm.
H. Lead-to-lead coplanarity shall be less than 0,10 mm from seating plane.
I. Falls within JEDEC MS-013-AE with the exception of the number of leads.

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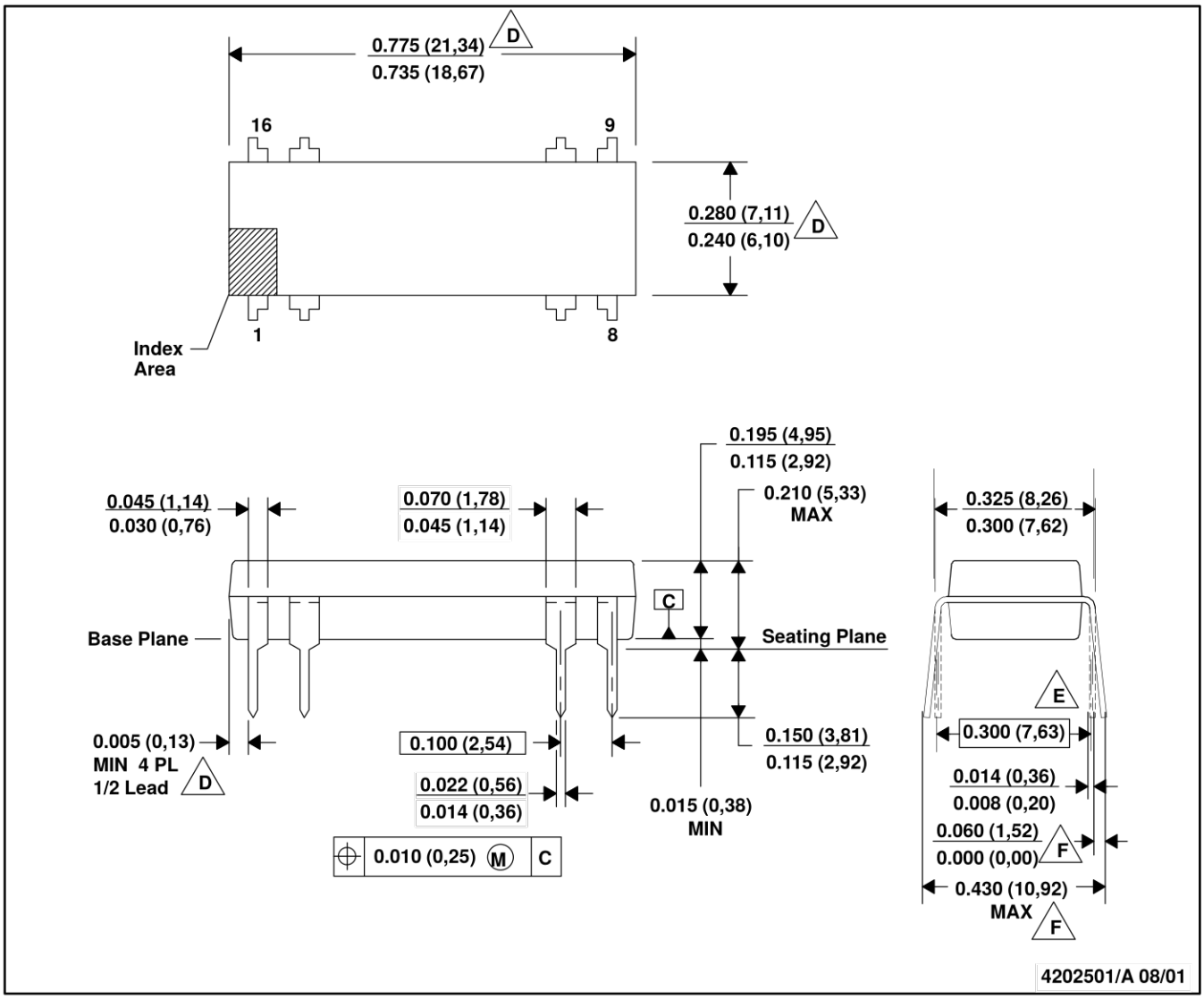
NVF (R-PDIP-T8/16) **PLASTIC DUAL-IN-LINE**



A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001-BB with the exception of lead count.
D. Dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 (0,25).
E. Dimensions measured with the leads constrained to be perpendicular to Datum C.
F. Dimensions are measured at the lead tips with the leads unconstrained.
G. A visual index feature must be located within the cross-hatched area.

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